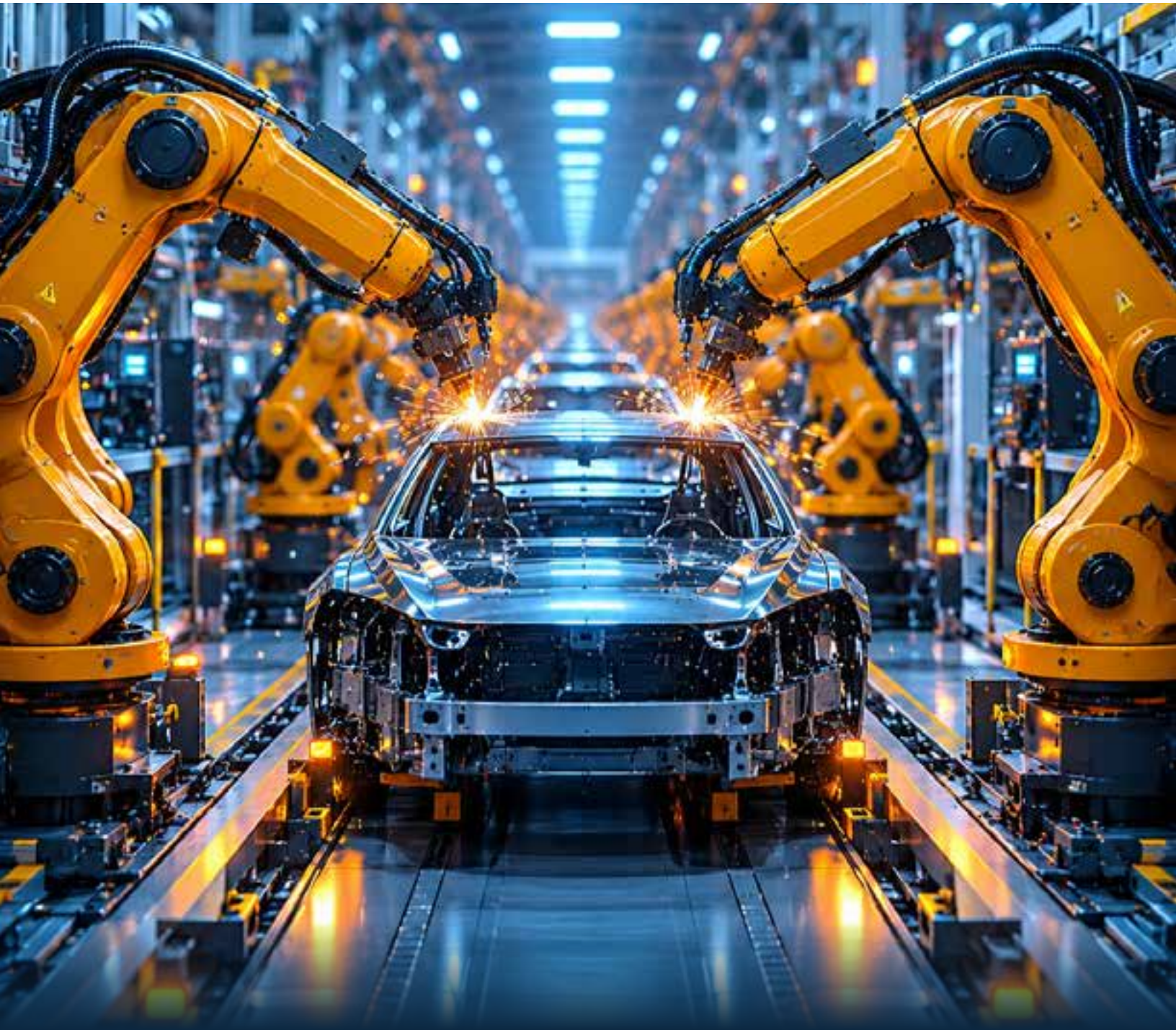
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How India's Fabless Ecosystem Can Drive Global Semiconductor Leadership

Iridium and Altair Integrate Satellite Connectivity into IoT Chipsets

India Signs ₹41 Billion Defence Deals for Satellite, Torpedoes

Bridging the Silicon Gap: Why Post-Silicon Validation Holds the Key to India's Semiconductor Ambitions



> *"Access to industry labs will help students work alongside post silicon validation engineers which allows them to learn in real time. The Government should also establish Post Silicon Center of Excellence labs across the states which will allow both students and start-ups to use them and bridge the gap."*

Banukumar M
Vice President - Test Engineering, Tessolve

India's semiconductor narrative has reached an inflection point. While domestic front-end RTL design prowess and headline-grabbing foundry investments under the India Semiconductor Mission (ISM) command global attention, the journey from cleanroom tape-out to commercial deployment hinges entirely on what happens next: testing,characterization, and packaging.

In an era dominated by heterogeneous chiplet architectures, AI-driven SoCs, and mission-critical automotive ADAS silicon, a functionally bootable chip is only the baseline. Converting initial silicon into a yield-optimized, high-reliability commercial product requires sophisticated Automated Test Equipment (ATE), rugged System-Level Test (SLT) environments, and comprehensive wafer-level screening to avert catastrophic latent failures in the field. As domestic fab and OSAT projects take root, closing the infrastructure and talent chasm in post-silicon validation is no longer optional—it is the definitive throughput determinant for the entire ecosystem.

In a recent interaction with **Rashmi Verma**, **Banukumar M**, Vice President - Test Engineering, **Tessolve**, discussed the pressing need to democratize test infrastructure for start-ups through expanded ISM policy incentives, shared engineering labs, and targeted ATE subsidies. He unpacked the rigorous engineering methodologies required to de-risk advanced multi-die packaging, shed light on evolving SLT and wafer-level reliability practices to curb silicon aging in mission-critical deployments, and outlined actionable blueprints for academia-industry partnerships to overcome acute post-silicon skill shortages. Furthermore, he articulated how Tessolve's integration of front-end ASIC design with turnkey test engineering—bolstered by strategic global acquisitions—is accelerating productization cycles and compressing client time-to-market.

While silicon design and foundry investments dominate headlines, chip testing and post-silicon validation are increasingly seen as true throughput constraints. From your perspective at Tessolve, what infrastructure and policy interventions does India need to build world-class test and characterization capabilities domestically?

India's semiconductor dream cannot be achieved only with design and foundry investments from Government initiatives. Many start-up design companies run into budget constraints by the time they tape out the chip, and they don't have enough funds left to perform the post silicon validation.

The Government and big companies have to invest in building high end characterization and engineering test labs, or have an extended partnership with companies like Tessolve which is one of the leading service providers for all post silicon validation activities. A start-up needs access to the full path from idea to product, including prototyping, fabrication, packaging, test, validation and productization. If these facilities are available within India's ecosystem, start-ups can get to market faster and at a lower cost. The current subsidy scheme under the India Semiconductor Mission (ISM) has to be extended to cover setting up post silicon validation facilities, building characterization labs, and procuring high-end ATE systems.

Also, the academia in India should upgrade the curriculum to include the topics related to post silicon validation which will enable

engineers coming out of colleges to be industry ready.

Getting first silicon to functional bring-up is only half the battle. What critical engineering gaps separate a functionally working tape-out from a commercially viable, yield-optimized product ready for mass deployment?

Tape-out marks the beginning of another critical phase, not the end of the engineering effort. A design that looks perfect in simulation does not always behave the same way in silicon. The functional bring-up of the first silicon covers only the boot sequence and some basic tests. A functionally working tape-out has major gaps in terms of full test coverage and an optimized test program with acceptable yield coverage for a product. It also does not cover the tests related to process variations in the wafers and packaged parts.

These additional tests are added to the production ATE test programs to get full test coverage. Commercially viable products for mass deployment will have full test coverage, yield optimization, test time optimization on ATE test programs and reliability tests, finally application related tests will be run at System Level Test (SLT). The engineering gap is wide and designers are now improving the design for test (DFT) to close the fault coverage gaps.

As advanced packaging (like EMIB and heterogeneous chiplet architectures) drives complexity skyward, how can chipmakers ensure zero-defect quality at scale without incurring unsustainable test costs or slipping critical launch timelines?

Advanced packaging comes with a lot of complexity in testing overall multi-die functionality using traditional end of line testing, and the main challenge is testing each die in the multi-die package. Every device must be tested before shipment, but more testing means longer manufacturing time and higher cost. The aim is to catch the failures that matter while keeping test time under control. An efficient way to ensure zero-defect quality is to test each die at wafer level for full test coverage before connecting multiple dies in a single package. Implementing strict wafer-level test flows ensures individual chiplets have near-zero defect rates before they go onto the substrate. DFT and design for manufacturability (DFM) play a major role in advanced packaging where chip designers incorporate additional routing lanes to overcome the failure of micro-bumps and also implement extensive built in self-test (BIST) at the design stage. By investing heavily in design-stage self-repair and wafer-level screening, chipmakers ensure zero-defect quality at scale without incurring unsustainable test costs or slipping critical launch timelines.

With automotive ADAS and industrial automation requiring high endurance, a chip passing day-one validation can still degrade over time. How is test engineering evolving to model latent defects, thermal stress, and long-term silicon aging before volume release?

Chips that pass day-one validation will degrade over time if proper life cycle testing is not done at the wafer level or package level. Test engineering is evolving to model and mitigate these risks by implementing on-chip monitoring to report degradation. Test engineers are moving away from traditional reliability testing to SLT based reliability testing and wafer level reliability testing. Test engineers use SLT environments to run real-world ADAS workloads at elevated voltages and temperatures. Wafer level reliability testing provides immediate feedback to foundries on the test results, so they can implement the required process improvements.

India boasts deep front-end RTL and design expertise, but advanced packaging, ATE development, and post-silicon test engineering face severe talent crunches. Where are the sharpest technical skill deficits today, and how should academia and industry bridge them?

In India, the focus has been more on design expertise, and academia has also built the education system to support design activities over the years. As we are step towards building Make in India chips, OSAT market and compete with the countries that have mastered this over the years, it is high time, academia and industry come together and revamp the engineering curriculum to address skill deficits in the post silicon validation. Academia should have a close partnership with semiconductor product companies and service companies like Tessolve to understand the gap and exact industry needs. Based on this, academia should come up with a program to teach the concepts of advanced packaging and post silicon validation techniques as part of its curriculum. Industry should help by providing access to the post silicon validation labs as setting up these labs is expensive. At Tessolve, we have set up semiconductor labs with universities, trained more than 7,000 semiconductor engineers and work closely with faculty to bring industry knowledge into the classroom.

Access to industry labs will help students work alongside post silicon validation engineers which allows them to learn in real time. The Government should also establish Post Silicon Center of Excellence labs across the states which will allow both students and start-ups to use them and bridge the gap.

With recent strategic milestones - including the Dream Chip acquisition, TPG/Vector Line backing, and collaboration on advanced packaging - how is Tessolve integrating front-end AI SoC design directly with end-to-end test engineering to shorten client time-to-market?

As Tessolve is a one stop end-to-end solution provider, the recent acquisition of Dream Chip Technologies has strengthened Tessolve's capacity to execute complex, leading-edge Application-Specific Integrated Circuit (ASIC) design projects and accelerate time-to-market for global customers. The TPG/Vector Line Capital backing helps accelerate planned acquisitions in the US and India to broaden engineering capabilities in AI and high-performance computing. With design expertise in-house, our test engineers work closely with the design team right from the initial stage and provide the required inputs from the test engineering side that help cover all possible tests at the design stage.

When the chip is taped out, we have full test coverage and our test engineers know exactly what is taken care of in the design and what tests need to be performed at the post silicon validation stage. As our test engineers are involved in the entire life cycle from the design stage, through package and assembly to test development at wafer level and package level, the time to market for the chip is shortened, which helps customers meet their targets.