

Verification & Semiconductors Futures Conference 2026



Tuesday,
6 October 2026



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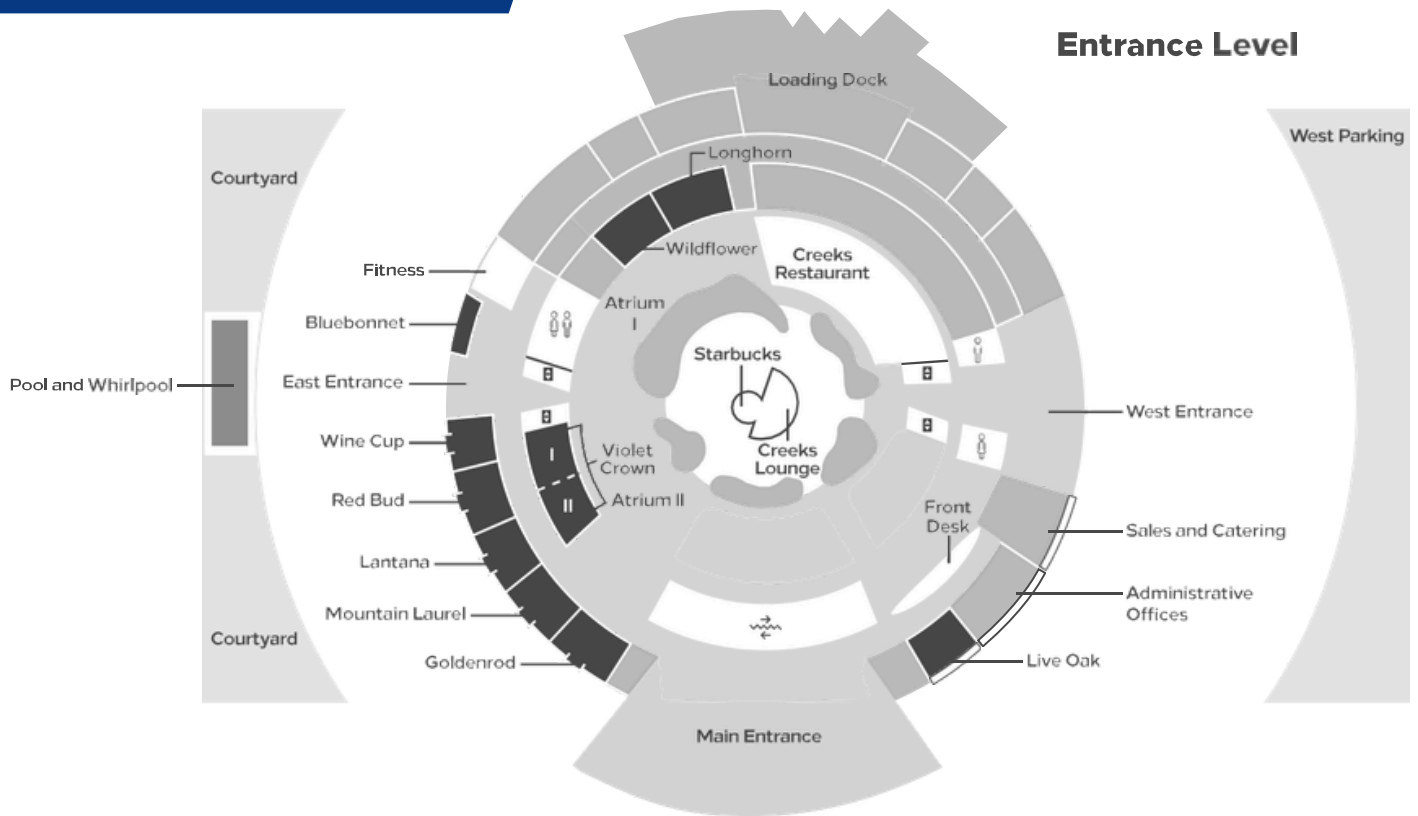


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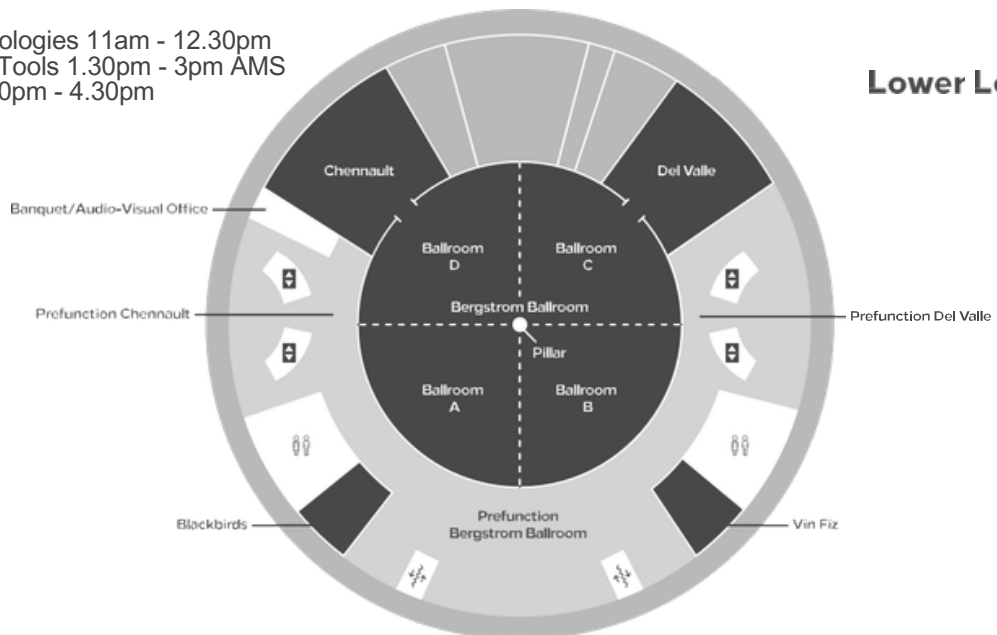


Index

	Track	Page Number	Venue
1.	Floor Plan	4	
2.	Agenda	5-6	
3.	Welcome Message by Tessolve	7	Ballroom A&B
4.	Opening Keynote	8	Ballroom A&B
5.	Industry Keynote	9	Ballroom A&B
6.	Formal Verification and AI	10-13	Ballroom A&B
7.	Emerging Hardware Technologies	14-17	Chennault
8.	Using AI in VLSI and DV	18-21	Ballroom A&B
9.	Open Source EDA design Tools	22-25	Chennault
10.	Using AI in DV	26-28	Ballroom A&B
11.	AMS Design and Verification	29-30	Chennault
12.	Feedback Form	39	



Chennault
Emerging Hardware Technologies 11am - 12.30pm
Open Source EDA Design Tools 1.30pm - 3pm
AMS Design and Verification 3.30pm - 4.30pm



Ballroom AB
Key Note 9.25am - 10.30am
Formal Verification and AI - 11am - 12.30pm
Using AI in VLSI and DV 1.30pm - 3pm
Using AI in DV 3.30pm - 4.30pm

FLOOR MAP KEY

- Meeting/Conference Rooms
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- Outdoor Space

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 **DOULOS**

Tuesday, 6 October 2026 (Morning)

- 08:30 AM** | **Registration, Breakfast & Networking**
- 09:25 AM** | **Welcome Note – Tessolve**
- 09:30 AM** | **Opening Keynote – Irene Deng, NXP**
Power Is the New Compute: How Energy Intelligence Will Define the Next Era of Semiconductors
- 10:00 AM** | **Industry Keynote – Nandan Nayampally, Baya Systems**
Correct by Construction, Accelerated by AI : A New Contract for Chiplet Verification

10:30 AM |  **Break**

Formal Verification and AI

11:00 AM | **Tobias Ludwig, Lubis EDA**
From Craft to System: A Platform Approach to Structured and Automated Formal Verification

11:30 AM | **David Landoll, Siemens**
The Future of Formal Verification: Scaling Proof, Productivity, and Adoption with AI

11:50 AM | **Paul Graykowski, Cadence**
Agentic AI in Verification: Introducing the ChipStack Super Agent

12:10 PM | **Shankar Channabasappa, Tessolve**
System Verilog RTL generation using NL Specification with AI tools

12:30 PM |  **Lunch Break**

Emerging Hardware Technologies

11:00 AM | **Gurpreet S. Kalsi, Intel**
BlFrost: A Composable, Resilient Interconnect Network Architecture for Scalable AI Systems

11:30 AM | **Ranjit Loboprabhu, Johns Hopkins University – APL**
Hybrid ASIC Automation Flows using Agentic AI

11:50 AM | **Jagadish Rongali, NXP Semiconductors**
DMA: The Hidden Engine Behind the AI performance : Architecture, Bottlenecks and Verification

12:10 PM | **Praveen Vagala**
A Reusable Three Layer Configuration Framework for FSDB to Module Level Stimulus Replay

Using AI in VLSI and DV

13:30 PM

Sunil Sahoo, Siemens

Breaking the Design-Verification Barrier with Agentic AI

14:00 PM

Shelly Henry, Moores Lab AI

The Verification Gap: What AI Produces vs. What Silicon Demands

14:20 PM

Vikash Kumar, ARM

Trustworthy Shift-Left Integration Strategies Using AI to Accelerate SoC Verification

14:40 PM

Tom Henige, MathWorks

From Algorithm to Verified Silicon: Accelerating Semiconductor Design with Model-Based Design, Shift-Left Verification, and AI

15:00 PM

 **Refreshment Break & Networking**

Using AI in DV

15:30 PM

Sasa Stamenkovic, Pure Silicon Solutions

Holistic Verification in the AI Era: Scaling Formal and Empowering Engineers

15:50 PM

Vinoth Selvan, NVIDIA

Agentic RCA for Performance Verification: Unifying RTL, Full-Chip, and Silicon Debug

16:10 PM

Frank Schirrmeister, Synopsys

The Next Era of Hardware-Assisted Verification for AI Systems: Modular, Software-Defined, and Hybrid

16:30 PM

Conference Close

Open Source EDA design Tools

13:30 PM

Andy Bond, Olix

AVL - Where's the Catch? Open Source, Feature Rich, and AI ready

14:00 PM

Amit Kumar, Tenstorrent

From Test Generator to Golden Model: Open-Source RISC-V Design Verification Building Blocks

14:20 PM

Abinaya Senthil, NXP Semiconductors

From Prompt to Passing Regression: LLM-Assisted UVM Testbench Bring-Up on an Open-Source RISC-V Core

14:40 PM

Madhukar Kadige (Remote)

How AI & Open-source can reshape VLSI industry

AMS Design and Verification

15:30 PM

Daniel Cross, Cadence Design Systems

Beyond Circuits: Modeling Arbitrary Physics in Digital Verification

15:50 PM

Daniel Cross, Cadence Design Systems

Beyond Circuits: Modeling Arbitrary Physics in Digital Verification

16:10 PM

Efrain Gaxiola, Silicon Labs

The Art of Silicon RF Validation: Measuring What a Radio Actually Does

Mike Bartley

CEO, Alpinum Consulting

Biography:

Mike has been involved in software testing and hardware verification since 1988 after completing a PhD in Math. He started his career in testing military software and safety-related aerospace applications using formal mathematical methods before moving into commercial software testing. Mike moved to semiconductor Design Verification (DV) in 1994 and has verified complex hardware products (on Silicon and FPGA) going into commercial and safety-related sectors such as mobile phones, avionics, automotive, comms, cloud/data servers, and, more recently, Artificial Intelligence. Mike built and managed state-of-the-art DV teams inside several companies (including STMicroelectronics, Infineon, Panasonic, and the start-up ClearSpeed), specialising in CPU verification and verifying over 15 different CPUs. Mike was invited to speak at many international conferences, helping him to become a well-known, global DV leader.

Mike founded and grew a DV services company to 450+ engineers globally, successfully delivering services and solutions to over 50+ clients on multiple continents and spanning the top 10 semiconductor companies through to start-ups, in various technologies and industries. He also advised several companies (ARM, NXP, and multiple start-ups) on organisational DV strategies. The company was acquired by Tessolve Semiconductors in 2020 and Mike worked at Tessolve as SVP in VLSI, managing the Centre of Excellence (CoE) for building new products and services across all Tessolve business units (VLSI, Test, PCB, and embedded SW) and developing AI capabilities and expertise across Tessolve. Mike is now running an AI and RTL to GDS VLSI services company Alpinum Consulting (www.alpinumconsulting.com) offering time-and-materials, fixed-price delivery-based, and full fixed-price turn-Key ASIC business models. Offices are both offshore and nearshore with development centres in Vietnam, India, Egypt, Eastern Europe, Mexico and Costa Rica.

Irene Deng

EVP/General Manager (Power & Energy), NXP Semiconductors

Presentation Title:

Power is the New Compute: How energy intelligence will define the next era of semiconductors

Abstract:

For decades, our semiconductor industry measured progress by Moore's law, transistor density, compute performance, software capabilities. The next decade is increasingly constrained by available energy, power delivery, thermal limits, battery life, and system efficiency.

The fundamental question is no longer "How much compute can we build?", but "How intelligently can we manage, convert, distribute, and optimize energy to unlock that compute?" This is an era where Power & Energy becomes a form of intelligence.

Why it is highly correlated to verification innovation:

1. The future challenges will be about verifying whether an intelligent system makes the right energy decisions under different operating conditions, not just verifying functionality and performance matrix.
2. Interaction between the compute and power becomes a critical system verification challenge. AI is uniquely valuable here.

Speaker Biography:

Irene Deng is executive vice president and general manager of Power and Energy at NXP Semiconductors. In this role, she is responsible for overseeing strategy, product innovation and execution, technology leadership, and financial performance for the business. With more than 20 years of experience in the semiconductor and technology industries, Irene has driven transformative growth and innovation across global businesses, delivered revenue growth and profitability, shaped investment strategies that strengthen market leadership, and built alignment across cross-functional teams.



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Nandan Nayampally

Chief Commercial Officer, Baya Systems

Presentation Title:

Correct by Construction, Accelerated by AI: A New Contract for Chiplet Verification

Abstract:

AI and chiplet systems are no longer limited by compute. They are limited by how efficiently and correctly data moves across dies, caches and memory. Yet verification still treats the interconnect as plumbing: generated late, stitched by hand, then chased with months of simulation for deadlocks, coherency escapes and QoS misses that were designed in from day one. AI agents now promise dramatic speedups, but without a trusted spec they risk finding the same problems faster, not fewer of them.

This keynote outlines a new contract between architecture and verification: principles we have embraced at Baya Systems'. Define intent once, in a machine-readable source of truth, with every change monitored and re-verified. Construct it right, with fabrics that are correct by construction, chiplet ready and checked by early static analysis. Prove it, with formal methods for protocol, coherency and deadlock properties, and workload-driven models for function and performance. Carry those models from concept to post-silicon. Then accelerate with AI, letting agents generate tests, close coverage and triage debug against a spec and proofs they can trust.

Attendees will leave with a practical framework for moving effort from bug-hunting to intent-proving, and eight questions to ask of any fabric, IP, flow or AI agent before it enters their next chiplet program.

Speaker Biography:

Nandan Nayampally is a semiconductor executive with nearly three decades of experience in engineering, product and business roles. With an extensive background in processing, systems, software and IP, he began on AMD's Athlon processor team. He spent 16 years at Arm building processor, fabric and vertical product businesses, serving as General Manager of the CPU business and the first GM of the Client business. He led Amazon's third-party Alexa effort and held roles at Denali and BrainChip.

Nandan has an M.A. in Computer Science from the University of Texas at Austin and a B.Tech. from the Indian Institute of Technology, Mumbai.



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Tobias Ludwig

CEO, LUBIS EDA

Presentation Title:

From Craft to System: A Platform Approach to Structured and Automated Formal Verification

Abstract:

Demand for new chips is outpacing the industry's capacity to verify them. Formal verification is a powerful guard against costly bug escapes, yet it remains a major effort sink, and projects still slip unpredictably toward sign-off. A closer look reveals why: alongside the expert work only domain specialists can do, sits a persistent layer of orchestration overhead, from extracting design information to updating verification plans and maintaining tool-specific scripts. This overhead is well-scoped and low-risk, precisely where AI can deliver value safely. But naive adoption fails, because formal verification demands the determinism and consistency that unguarded AI agents undermine.

The answer is a platform approach. This talk presents an AI-first platform built at LUBIS EDA that grounds automation within well-defined guardrails, making process discipline the default rather than a deliberate investment. The platform acts as a central cockpit for AI- and tool-based automations. It loads the design into the formal environment, extracts key I/Os and behaviors with generated descriptions, populates the verification plan, and maintains the scripts formal checks depend on, all feeding an integrated project view with no manual reporting overhead. The result is a clean separation of concerns: engineers focus on the work only they can do, while the platform owns everything else.

Speaker Biography:

Dr. Tobias Ludwig is CEO and co-founder of LUBIS EDA, where he leads the company's formal verification methodology and the development of the FormalOS infrastructure. A recognized expert in formal verification, Tobias is dedicated to helping semiconductor companies achieve more practical, predictable, scalable verification for today's most complex chip designs.



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David Landoll

Product Manager, Questa Static & Formal Solutions , Siemens

Presentation Title:

The Future of Formal Verification: Scaling Proof, Productivity, and Adoption with AI

Abstract:

As design complexity continues to accelerate, verification teams are under increasing pressure to find bugs earlier, close coverage faster, and improve productivity. Formal verification is increasingly being deployed beyond traditional property checking to address connectivity, security, coverage closure, processor verification, and signoff challenges. At the same time, automation and AI-assisted workflows are lowering adoption barriers and enabling wider use across engineering teams. This presentation examines the evolution of formal verification, shares lessons from real-world deployments, explores the opportunities and limitations of AI-assisted verification, and discusses how formal methodologies may continue to evolve in the years ahead.

Speaker Biography:

David Landoll is a Product Manager within Siemens EDA focused on formal and static verification technologies, including formal verification, static analysis, CDC, and AI-assisted verification solutions. With more than 30 years of experience in semiconductor verification, David has helped develop and deploy advanced verification methodologies used by many of the industry's leading semiconductor companies. His work spans formal verification, safety and security verification, design signoff, and the application of AI to improve verification productivity. David is a frequent speaker at industry conferences and technical events and serves on the DVCon Technical Program Committee.



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Paul Graykowski

Product Marketing Director, Cadence

Presentation Title:

Agentic AI in Verification: Introducing the ChipStack Super Agent

Abstract:

Semiconductor design complexity is outpacing traditional engineering capacity, driving EDA tools past point solutions toward agentic, AI-driven optimization. Cadence answers this shift with a family of AI agent stacks integrated directly into its tools to work alongside engineers. ChipStack™ Super Agent is the stack purpose-built for design verification: specialized agents that assist with test planning and coverage closure, formal testbench generation and debug, and regression debugging with auto-fix. ChipStack embeds within the engineer's existing verification flow, coordinating tools and methodologies to accelerate each stage while keeping the engineer in control.

Speaker Biography:

Paul Graykowski is a Product Marketing Director in the System Verification Group at Cadence, focused on Verification IP (VIP). With over 25 years of experience designing and verifying System on Chip (SoC) solutions, he has worked across simulation, mixed-signal verification, UVM, and verification methodology. More recently, Paul has been involved in sharing Cadence's work on verification optimization and agentic AI. He previously held marketing and application engineering roles at Arteris and Synopsys, and worked in design and verification at Cirrus Logic, Compaq, and Intel. He received his BSEE from Texas A&M University.



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Shankar Channabasappa

AVP Custom Silicon, Tessolve Semiconductor Inc

Presentation Title:

System Verilog RTL generation using NL Specification with AI tools

Abstract:

How to generate System Verilog RTL using NL Specifications? It is possible now with AI tools such as Claude, Cadence ChipStack AI Super Agent, Alpha Design AI ChipAgents, and Synopsys.ai Copilot. These tools are transforming front-end semiconductor design by converting specifications, microarchitecture documents, interface definitions, and register maps into draft SystemVerilog RTL, assertions, and verification collateral.

ChipStack and ChipAgents use multi-agent workflows with design-intent awareness, while Claude and other LLMs provide prompt-driven RTL generation and design assistance. These tools can significantly accelerate RTL development, verification planning, and debug activities.

However, generated RTL still requires expert review, simulation, linting, CDC/RDC analysis, formal verification, and signoff before production use.

Speaker Biography:

Shankar Channabasappa is a seasoned semiconductor technology leader with over two decades of experience spanning the complete ASIC development lifecycle, from architecture and specification through RTL design, verification, physical implementation, and GDSII signoff. He holds an M.S. in Electrical Engineering from the Indian Institute of Science (IISc), Bangalore, and has successfully built and led high-performance engineering teams across the United States and India.

His expertise includes high-performance networking and AI/ML SoCs, PCIe Gen5/Gen6, DDR memory subsystems, high-speed Ethernet, 200G SerDes, Interlaken, and ARM-based SoC architectures. He has led the development of silicon-proven products in advanced technologies, including TSMC N3P, enabling industry-leading performance, power efficiency, and area optimization for cloud, AI, and data center applications.



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Gurpreet Singh Kalsi

Principal Engineer, Intel

Presentation Title:

BiFrost: A Composable, Resilient Interconnect Network Architecture for Scalable AI Systems

Abstract:

AI scaling is increasingly limited by communication, memory, and system complexity. BiFrost is a composable interconnect architecture that unifies communication across chiplets, packages, and large-scale systems. A scalable FatTree fabric, shared address space, and packet-address compute engine enable software-transparent resource composition, while adaptive routing and dynamic remapping provide resilience under failures. BiFrost demonstrates how a unified fabric can simplify AI system design, improve scalability and programmability, and enable the next generation of composable AI infrastructure.

Speaker Biography:

Gurpreet Singh Kalsi is a Principal Engineer in Intel's Datacenter Group, specializing in large-scale system architecture, AI infrastructure, and hardware-software co-design. Over two decades at Intel, he has contributed to more than 10 revenue-generating silicon programs and led innovations spanning AI accelerators, GPU architectures, memory systems, and high-performance networking. He has held technical leadership roles across Intel and U.S. Government research programs, enabling scalable system connectivity through silicon photonics and co-packaged optics technologies. Gurpreet holds over 50 issued or submitted patents, has published more than 20 papers in leading IEEE venues, and is the lead author of BiFrost, a composable interconnect architecture for scalable AI systems.



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Ranjit LoboPrabhu

Sr. Staff 2, Johns Hopkins Univ – Applied Physics Lab

Presentation Title:

Hybrid ASIC Automation Flows using Agentic AI

Abstract:

This work presents three practical uses of automation and AI in ASIC design. First, agentic AI is used to trace scan-chain failures, find the first bad stage, and identify timing problems. Second, a hybrid Aprisa, Virtuoso, and Calibre flow supports custom routing while keeping implementation and signoff controlled. Third, pad-ring creation is automated from a structured pad list, generating both RTL and physical placement data. Together, these methods reduce manual effort, improve consistency, and make complex design flows easier to repeat, review, debug, and verify.

Speaker Biography:

Ranjit is an implementation expert and has worked on 45+ chip designs in startups and large companies across AI/CPU/Networking/Communications sectors.



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Jagadish Rongali

Senior Principal Engineer, NXP Semiconductors Inc

Presentation Title:

DMA: The Hidden Engine Behind the AI performance – Architecture, Bottlenecks and Verification

Abstract:

DMA is becoming a key bottleneck in modern AI SoCs as compute scales. This talk outlines a generic DMA architecture and a verification approach combining UVM/SVA simulation, formal property verification, and emulation. It highlights deadlock/starvation-proof design, formal methods for liveness and functional safety (ISO26262), and the role of emulation for full-workload stress testing. It also describes running simulation, formal, and emulation in parallel to accelerate schedules, and briefly explores a cost-conscious RAG-based workflow to support debug and triage.

Speaker Biography:

Jagadish Rongali is a Senior Principal Engineer with 18+ years of experience delivering silicon-proven SoC solutions across automotive, wireless, mobile, healthcare, and secure-payment domains. He specializes in SoC/IP verification, FPGA prototyping, system-level emulation, formal verification, low-power verification, and RNM modeling. Jagadish has led complex verification programs at NXP and Goodix, improving coverage, quality, and silicon success. His work spans secure-boot engines, DMA IP, RF-digital interfaces, SerDes/DDR, and mixed-signal subsystems. An active contributor to patents, publications, and industry forums, he also mentors engineers and drives automation initiatives that accelerate hardware bring-up and reduce re-spins.



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Praveen Kumar Vagala

Design Verification Engineer, Independent Researcher

Presentation Title:

A Reusable Three-Layer Configuration Framework for FSDB-to-Module-Level Stimulus Replay

Abstract:

Verification teams often need to reproduce chip- or subsystem-level simulation failures at the IP level, where debugging is faster. Manual waveform extraction and stimulus formatting are slow, error-prone, and repeated for each IP. This talk presents CDSR (Configuration-Driven Stimulus Reconstruction), which separates signal probing, protocol-semantic reconstruction, and replay-target mapping into declarative YAML layers interpreted by a single reusable engine. CDSR reconstructs stimulus once for replay in compatible testbenches. Validation across OpenTitan AES and OTBN and OpenHW CV32E40P, spanning two protocol families, completed in under 35 seconds and achieved 100% byte-exact fidelity against the original binaries

Speaker Biography:

Praveen Kumar Vagala is an independent researcher and design verification professional in the semiconductor industry, with over 16 years of experience across GPU, SoC, FPGA, and complex reusable IP verification. His professional work includes architecting advanced verification methodologies, reusable testbench environments, coverage-closure, formal verification flows, AMS, and AI/LLM-assisted automation frameworks for complex hardware systems. Alongside his semiconductor engineering career, he contributes to the broader research and technology community as a technical author and scholarly peer reviewer, evaluating technical manuscripts and research contributions in his field. His research focuses on design verification automation, embedded systems, coverage closure, AI-assisted verification methodologies, and scalable verification infrastructure for modern chip-development programs.



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Sunil Sahoo

Product Manager, Siemens EDA

Presentation Title:

Breaking the Design-Verification Barrier with Agentic AI

Abstract:

Modern SoC design complexity has outpaced traditional methodologies, while the persistent divide between design and verification has deepened the challenge. Agentic AI addresses this by enabling autonomous systems that reason, plan, and adapt across the chip development lifecycle. Rather than simply accelerating workflows, it helps dissolve boundaries between creation and validation. Semantic layers connect isolated EDA tools, turning them into collaborative, context-aware elements of an orchestrated ecosystem. These intelligent tools coordinate design, verification, analysis, and signoff across the full flow, supporting trusted RTL signoff with greater speed and confidence. The era of siloed tools is ending; orchestrated intelligence is beginning.

Speaker Biography:

Sunil Sahoo is a Product Manager for simulation tools at Siemens Digital Industries Software, focused on advancing functional verification solutions for modern SoC development. With over 14 years of EDA experience spanning digital design, verification, and applications engineering, he brings practical insight into the challenges of complex chip development and RTL signoff. Sunil works with customers exploring verification methodologies and emerging approaches such as AI-driven, orchestrated tool flows that connect design, verification, analysis, and signoff. He holds a B.S. in Electronics and Communications Engineering from VIT University, India, and an M.S. in Computer Engineering from Villanova University.



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Shelly Henry

CEO | Founder, Moores Lab AI

Presentation Title:

The Verification Gap: What AI Produces vs. What Silicon Demands

Abstract:

Every chip team has tried it: paste your spec into an LLM, watch a UVM testbench appear in seconds. The output looks plausible — monitors, drivers, a scoreboard, cover groups. Then a DV engineer looks at it. The testplan misses corner cases. The monitor doesn't handle back pressure. The scoreboard assumes in-order transactions. SVA properties are syntactically correct but semantically wrong. The coverage model samples signals instead of closing design intent. This talk walks each artifact — testplan, testbench components, testcases, SVA, and functional coverage — showing where AI falls short today, what production DV requires, and what it takes to close the gap.

Speaker Biography:

Shelly Henry is CEO and Co-Founder of Moores Lab AI, where he is transforming semiconductor design and verification through agentic AI. With more than 20 years of experience in silicon engineering and AI, Shelly has led teams at Microsoft and ARM and contributed to more than 20 chip programs spanning Xbox, HoloLens, smartphones, cloud, and AI infrastructure. His deep expertise spans processor architecture, hardware engineering, and the end-to-end challenges of modern chip development. Shelly holds a Bachelor's degree from IIT Madras and a Master's degree from the University of Illinois Urbana-Champaign. He is focused on making advanced silicon innovation faster, more accessible, and dramatically more scalable.



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Vikash Kumar

Senior Verification Architect, Arm

Presentation Title:

Trustworthy Shift-Left Integration Strategies Using AI to Accelerate SoC Verification

Abstract:

A VEGA Framework approach to governed, evidence-based AI verification Shift-left stalls because the verification environment lands too late. AI can collapse that timeline, generating the driver, monitor, scoreboard, sequences, and coverage from the spec in hours. But early and fast is worthless if the generated environment is hollow, because that just shifts false confidence left. This talk shows a VEGA-framework approach. AI generation is anchored to machine-readable intent, then a tool-agnostic metric set scores stimulus quality, checking integrity, and observability before the environment is trusted. Calibrated against a hand-built environment on the same block, the metrics become something you can actually gate a shift-left flow on.

Speaker Biography:

Vikash Kumar is a Senior Verification Architect at Arm and an IEEE Senior Member with over 15 years in the semiconductor industry, specializing in the verification of complex designs across IP, subsystem, and full SoC levels using SystemVerilog and UVM. He is the author of the forthcoming Springer book AI-Assisted Hardware Verification: Cognitive Verification Architecture with the VEGA Framework. His work focuses on large-scale SoC integration and verification closure, with deep experience in AMBA, CHI, PCIe, and UCIe. Prior to Arm, he held roles at Intel, contributing to silicon programs including the Intel Data Streaming and Analytics Accelerators.



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Tom Henige

Application Engineer, MathWorks, Inc.

Presentation Title:

From Algorithm to Verified Silicon: Accelerating Semiconductor Design with Model-Based Design, Shift-Left Verification, and AI

Abstract:

As semiconductor devices grow in complexity, engineering teams face increasing pressure to meet ambitious performance, power, schedule, and quality objectives. This presentation explores how Model-Based Design and shift-left verification methodologies help teams identify and resolve issues earlier in the development process.

Attendees will learn how Model-Based Design supports workflows spanning algorithm development, architectural exploration, HDL generation, high-level synthesis (HLS), and verification. The session also examines the emerging role of agentic AI and highlights real-life case studies demonstrating improved productivity, design quality, and time to silicon.

Speaker Biography:

Tom Henige, Application Engineer at Mathworks

Tom supports customers using Mathworks' HDL code generation and verification products. He has over 20 years of experience in FPGA design and verification. His previous work includes next-gen wireless systems at Samsung Research America, communications and telemetry for aerospace at Southwest Research Institute, and data acquisition systems at Texas Instruments. He holds a Bachelors Degree in Electrical Engineering from Texas A&M University, and several patents in channel coding hardware implementations.

Andy Bond

Director RTL and Verification, OLIX

Presentation Title:

AVL – Where’s the Catch?. Open Source, Feature Rich and AI ready

Abstract:

AVL – The Apheleia Verification Library was released in 2025, an open-source Python based verification library with VIP and full simulator support. One year on, what has changed and what have we learnt.

Primarily we’ve learnt to support the community. Through them we’ve seen significant performance improvements, user focused VIP development and the efficiency advantages of running testbenches tightly integrated with AI.

Speaker Biography:

Andy Bond has over 25 years industry experience as a design and verification engineer, manager and leader.

He developed AVL to combine the advantages of UVM, CocoTB and Python together in a completely free and open-source environment. By enabling commercial grade verification to anyone with a laptop, without the overhead of bloated methodologies, we can bring cutting-edge verification to universities, start-ups and multi-nationals.

In his role as Director of RTL and Verification at OLIX he’s working with some of the best minds in the industry to solve the most consequential problem in the development of frontier AI.



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Amit Kumar

Principal Engineer, Tenstorrent

Presentation Title:

From Test Generator to Golden Model: Open-Source RISC-V Design Verification Building Blocks

Abstract:

Every RISC-V DV team builds the same four layers around its RTL: stimulus, reference model, testbench environment and checking. Tenstorrent has open-sourced all four as separable, production-grade components: RiescueD/RiescueC/CTK for directed and compliance test generation, Whisper as a steppable golden model, rv_tester as a lockstep core testbench with platform models, and CoreArchCoverage for ISA coverage derived from the model. This talk walks the stack end to end, shows it running on CVA6 and OpenC910, then scopes the same four roles down to a unit-level MMU environment. Attendees leave knowing which piece to adapt first.

Speaker Biography:

Amit Kumar is a Principal Engineer in RISC-V Design Verification at Tenstorrent, based in Austin, Texas. His work focuses on verifying high-performance RISC-V cores, with particular emphasis on memory-management units, functional coverage, and scalable verification infrastructure. He leads development of reusable verification frameworks that combine UVM, RiESCUE, and Whisper, and actively drives open-source collaboration and tool adoption, including Verilator. Amit also contributes to verification of non-coherent atomics, vector extensions, and functional-safety features. Passionate about rigorous, evidence-driven engineering, he enjoys turning complex verification challenges into practical methodologies that improve confidence, productivity, and adoption across the broader RISC-V engineering community and beyond.



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Abinaya Senthil

Design Verification Engineer, NXP Semiconductors

Presentation Title:

From Prompt to Passing Regression: LLM-Assisted UVM Testbench Bring-Up on an Open-Source RISC-V Core

Abstract:

Most AI-in-verification talks stop at the demo. This one starts after it. Using an open-source RISC-V core, this session walks through bringing up a UVM testbench with LLM assistance end to end: generating agents, sequences and scoreboard scaffolding, then closing the gap between code that compiles and code that catches bugs. It covers where the model saved real days, where it quietly cost time through hallucinated APIs and plausible-but-wrong assertions, and the review discipline that separates the two. Attendees leave with a workflow they can try on their own testbench and an honest accounting of its limits.

Speaker Biography:

Abinaya is a Design Verification Engineer at NXP Semiconductors in Austin, Texas, working on UVM-based IP verification, CDC verification, and functional safety for automotive SoCs. Her work on AI-assisted regression optimization in UVM-based verification was presented at CSTIC 2026 and indexed in IEEE Xplore, and her current research focuses on LLM-assisted UVM testbench generation for RISC-V processors. She founded SiliconDV, an education platform for design verification engineers with an audience of over 10,000 and more than 50 engineers mentored. She holds a master's from Boston University and a bachelor's in Electronics and Communication Engineering from CEG, Anna University.



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Madhukar Kadige

Senior design and verification engineer, Beammwave AB

Presentation Title:

How AI & open-source can reshape VLSI industry

Abstract:

As AI & ML usage is predominantly increasing in the modern world, many industries started adopting it for productivity & other purposes. No doubt AI & ML take over old boring processes and eventually increase productivity. On the other hand opensource technologies are attracting enthusiasts/researchers/academicians and triggering to think in a different dimension.

For time to market, industries rely on quick and pre-existing solutions. By combining opensource technologies with AI/ML, it is possible to reshape the VLSI tools and processes. It is also possible to think about low cost EDA solutions instead of expensive commercial EDA solutions.

Speaker Biography:

Madhukar Kadige, having close to 20 years of experience in VLSI industry. Performed many roles as an engineering college assistant professor, field application engineer, academic project consultant, design and verification engineer etc., in various domains starting with mobile communications, fiberchannel and ethernet. Built IP/subsystem/SoC verification environments and executed UVM/C-testcases.

Integration and deployment of various EDA tools and flows. DV technical lead for a 30+ member team. Like start-up models where team-work and independent-work are the key growth factors for both engineers and the company.



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Sasa Stamenkovic

Principal Engineer, Formal Verification, Pure Silicon Solutions

Presentation Title:

Holistic Verification in the AI Era: Scaling Formal and Empowering Engineers

Abstract:

Modern SoC verification demands more than a single methodology. This presentation explores a holistic approach that combines targeted formal verification, scalable simulation, deep collaboration between verification and design teams, and guided AI acceleration. Through practical examples, we examine how decomposition and sound abstraction make formal verification effective on complex designs, while dual-runable environments help connect formal and simulation. We then explore how AI agents can act as supervised “junior engineers,” accelerating testbench development, environment bring-up, and counterexample triage. The result is a verification strategy that scales engineering capacity while keeping human expertise and design intent at its core.

Speaker Biography:

Sasa Stamenkovic is a Principal Engineer and Formal Verification Leader at Pure Silicon Solutions, with 15 years of experience in hardware design verification and formal verification. Since graduating with an MS in VLSI Engineering from the University of Novi Sad in 2010, he has focused his career on formal methods, continuously adopting and developing new verification methodologies and techniques.

Before joining Pure Silicon Solutions, Saša spent more than a decade at OneSpin Solutions and Siemens, working with semiconductor companies and engineering teams to apply formal verification to complex hardware designs. His experience spans a broad range of designs and verification challenges, with a particular focus on developing practical formal verification solutions that help teams achieve confidence and convergence on complex designs.



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Vinoth Selvan

Senior Design Verification Engineer, NVIDIA Corporation

Presentation Title:

Agentic RCA for Performance Verification: Unifying RTL, Full-Chip, and Silicon Debug

Abstract:

Performance root-cause analysis becomes harder as designs move from RTL to full-chip validation and silicon, where evidence sources, observability, and debug workflows differ. This talk presents an agentic RCA methodology for performance verification that uses AI to orchestrate a controlled evidence loop across trusted tools and reusable debug procedures. MCP tools provide structured access to platform-specific measurements, while Skills capture expert playbooks for bandwidth analysis, latency investigation, clock/configuration checks, and bottleneck isolation. The flow produces a reproducible RCA report with supporting evidence, confidence basis, and the next decisive action, enabling faster, more consistent performance debug across platforms.

Speaker Biography:

Vinoth Selvan is a Senior Design Verification Engineer at NVIDIA, leading pre-silicon performance verification and silicon-correlated validation for high-speed interconnect architectures. With 15 years of semiconductor design verification experience, including a decade at NVIDIA and earlier roles at Intel and Qualcomm, he has worked across clocks and reset, error resiliency, power management, performance verification, and silicon bring-up/debug for complex workload-driven performance issues. His recent work focuses on agentic AI, MCP-based debug infrastructure, reusable verification Skills, and evidence-driven RCA workflows that improve performance analysis from RTL through silicon. Vinoth holds an M.S. in Electrical Engineering from the University of Minnesota, Twin Cities.



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Frank Schirrmeister

Executive Director, Strategic Programs, Synopsys

Presentation Title:

The Next Era of Hardware-Assisted Verification for AI Systems: Modular, Software-Defined, and Hybrid

Abstract:

The rapid rise of AI-driven systems is transforming both semiconductor design and verification. AI accelerators, chiplet-based architectures, and software-defined products are driving unprecedented verification complexity, while the hardware-assisted verification (HAV) market requirements are bifurcating between large-scale data center AI workloads and software-centric edge, mobile, and physical AI applications. This presentation examines the shift toward modular HAV architectures that enable scalable capacity, IP-centric validation, and seamless progression from emulation to prototyping. It also explores AI-assisted workflows, hybrid verification, and low-power validation techniques that combine virtual platforms with RTL-accurate emulation to accelerate software development and expose system-level issues before silicon availability

Speaker Biography:

Frank Schirrmeister is Executive Director, Strategic Programs, System Solutions in Synopsys' Market and Products Group. He leads strategic activities across system software and hardware assisted development for industries like automotive, data center and 5G/6G communications, as well as for horizontals like Artificial Intelligence / Machine Learning. Prior to Synopsys, Frank held various senior leadership positions at Arteris, Cadence Design Systems, Imperas, Chipvision, and SICAN Microelectronics, focusing on product marketing and management, solutions, strategic ecosystem partner initiatives, and customer engagement. He holds an MSEE from the Technical University of Berlin and actively participates in cross-industry initiatives as Panel Chair of the Design Automation Conference.



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Daniel Cross

Solutions Architect, Cadence Design Systems

Presentation Title:

Beyond Circuits: Modeling Arbitrary Physics in Digital Verification

Abstract:

Most systems include some non-circuit elements. Complete verification of these systems requires including important behaviors of the non-circuit elements within digital verification simulations. This work reviews SystemVerilog behavioral modeling techniques that can be used to simulate a variety of non-circuit system elements. It includes relevant examples demonstrating the use of these modeling techniques.

Speaker Biography:

Daniel Cross holds MSECE and BSEE degrees from the University of Miami. He has been applying behavioral modeling and mixed signal simulation to verification problems for over 20 years. He joined Cadence in 2019 and has championed the use of Real Modeling and advanced verification methodologies for mixed signal designs. He is a Senior Member of the IEEE and participates in several IEEE standards working groups.



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Efraín Gaxiola

Associate Staff Engineer, Silicon Labs

Presentation Title:

The Art of Silicon RF Validation: Measuring What a Radio Actually Does

Abstract:

Validating a wireless system-on-chip is not simply connecting an instrument and recording a number. At RF frequencies, cables, fixtures, interference, instrument limits, and software can become part of the result. This presentation explores how engineers separate true silicon behavior from measurement artifacts while evaluating figures of merit such as noise figure, receiver sensitivity, transmit power, modulation quality, unwanted emissions, interference susceptibility, and radiated performance. Attendees will learn how shielding, calibration, filtering, automation, temperature testing, repeatability, and correlation transform difficult measurements into trustworthy engineering conclusions—and why RF validation remains both an art and a science in practice.

Speaker Biography:

Efraín Gaxiola is an associate engineer on Silicon Labs technical staff, where he leads development of RF validation infrastructure and automated testing for next-generation Internet of Things systems-on-chip. He has held technical leadership roles in wireless, automotive, television, and radio tuners, and previously worked at Texas Instruments and Biotronik. Efraín holds a PhD in Electrical Engineering from Texas A&M University and a bachelor's degree in Electronic Engineering from Instituto Tecnológico de Mérida. He received Yucatán's State Youth Prize in Academia, has published in peer-reviewed journals, earned multiple Silicon Labs Technical Symposium awards, and holds an automotive patent.



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02

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03

Prepare

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04

Execute

Develop and refine verification evidence

05

Sign Off

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FORMAL VERIFICATION
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100%

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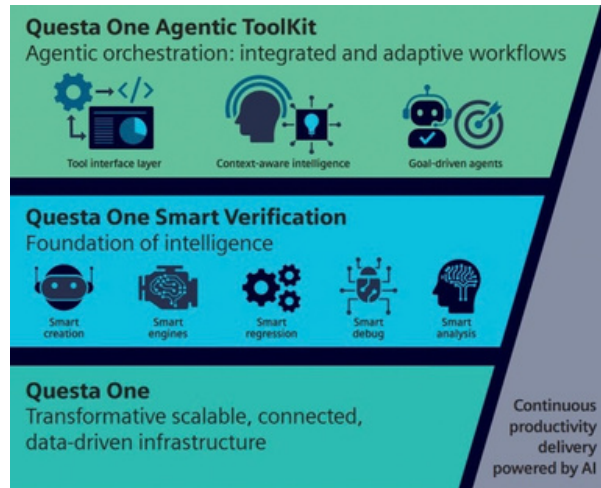


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- Flexible integration preserves current investments with optimized performance and comprehensive verification in an open ecosystem
- Delivers Agentic AI autonomous workflows that operate within the verification domain under customer-defined governance boundaries with autonomous goal decomposition, adaptive cross-run strategies and persistent expertise building

Partner and customer experiences

*"The increasing complexity of modern chip design and verification requires a new generation of intelligent, agentic workflows that can reason through intricate tasks while maintaining the highest levels of precision," said **Tim Costa, general manager of Industrial and Computational Engineering, NVIDIA**. "By leveraging NVIDIA NIM and Nemotron reasoning models, Siemens is providing engineers with a powerful, AI-driven foundation to accelerate the development of the world's most advanced electronic systems."*

*"The productivity gains delivered by the Questa One Agentic Toolkit were both immediate and significant," said **Akshay Aggarwal, senior director of Engineering, MediaTek**. "Our engineers were able to become proficient within hours, despite limited prior exposure to the tool - completing tasks that typically require days, and mastering workflows that would usually take weeks of training. In combination with MediaTek's existing advanced in-house verification methodology, the Questa One Agentic Toolkit not only bridged the knowledge gap but fundamentally accelerated our operational processes."*

*"Combining AI and verification, Questa One enabled our team to quickly adopt full agentic Formal Property Verification, and auto-fix issues with Lint Agent," said **Shalesh Thusoo, founder and chief executive officer, Tsavorite Scalable Intelligence**. "With the Agentic Toolkit, we leverage these capabilities and their productivity gains at the optimal point in our development flow."*

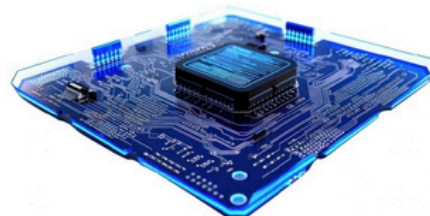
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Holistic verification for the AI era

Scaling Formal and Empowering Engineers



Pure Silicon helps semiconductor teams find the deep, corner-case failures that threaten schedules, re-spins, and first-silicon success. We combine formal rigor, simulation scale, and expert-guided AI to strengthen signoff confidence.

THE VERIFICATION PRESSURE

14% A0 success rate in 2024

Compressed design cycles and familiar verification flows leave rare states, configuration interactions, and complex control paths exposed.

THE AI-GENERATED RTL BOOM

More RTL. New escape risks.

Generated code can look structurally clean while masking deep logic errors. Independent expert verification provides the essential guardrail before tape-out.

THE VERIFICATION SWEET SPOT

Formal depth where simulation struggles. Dynamic scale where full-chip behavior matters. Human judgment across both.

TARGETED FORMAL RIGOR

Exhaustive proofs for high-risk control logic, deadlock, security, coherence, SEC, CDC, and hidden configurations. Optimal for early bug discovery.

DYNAMIC VERIFICATION

SV/UVM environments, verification planning, regressions, debug, and meaningful coverage closure at IP and SoC scale.

GUIDED AI ACCELERATION

AI-assisted analysis, assertion development, and triage with expert review, traceability, and signoff discipline.

PREDICTABLE TAPE-OUT

Eliminate bug escapes that cause schedule slips, costly re-spins, and post-silicon failures.

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skilled experts

10+ yrs

average experience

20+

successful projects

6

Fortune 100 clients

ISO

9001 + 27001

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Create robust design.



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Catch issues early.



DebugAgent

Find issues faster.
Resolve with precision.



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Maximize coverage.
Justify exclusions.

FOUNDATION PACKAGES

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Curated Verification Expertise

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Works with leading AI platforms



Pre- Built Components & IP

High-quality, reusable verification assets



Standards Aligned

Built to industry and tool standards



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Industry- proven approaches that work



Proven & Production Ready

Used in real-world designs at scale



Scalable & Flexible

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Verified & Reliable

Quality you can trust, results you can rely on

Built on a strong foundation. Powered by intelligent agents.



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- » AMD FPGA Flows » Signal & Power Integrity

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- SOC Verification
- CPU/GPU Verification
- DFX Validation
- Low-power RTL and Netlist verification
- Gate Level Simulations

Scale

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- IP
- SS/SOC
- GLS
- DFX

Methodologies

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- Formal Verification
- PSS – Portable Stimulus standards
- Adaptation of AI/ML methodologies

Low-speed peripherals

- SPI/QSPI
- I2C/I3C
- I2S
- UART
- CAN 1.0/2.0
- SPDIF

Memory interfaces

- SD Card 3.0
- ONFI 3.2
- LPDDR/DDR 3/4/5
- UFS
- NVMe

MIPI

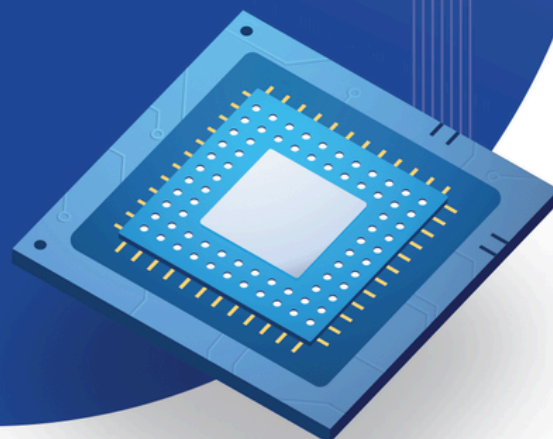
- RFFE
- DSI
- CSI
- D-PHY
- C-PHY

CPU Core & Infra

- ARM Cortex M*, A*
- RISC-V
- Tensilica

HSIO

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- PCIe GEN 3/4/5/6
- UCIe 1.0/1.1
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- SPI 4.2
- DP 1.2



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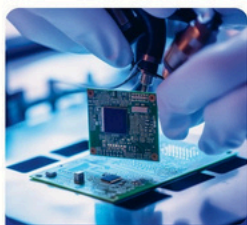
Scaled To Your Unique Needs

Balancing Timeline & Costs

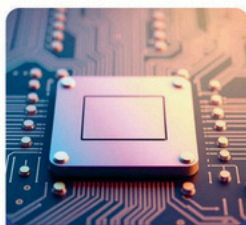
Results in Delivering Products Faster

Committed to Project Milestones

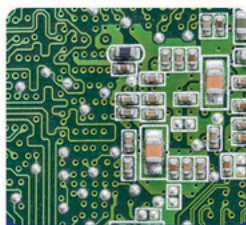
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Silicon Testing (ATE/Bench Lab)



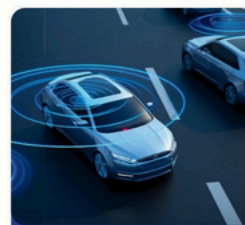
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