

Verification & Semiconductors Futures Conference 2026



Thursday,
8 October 2026



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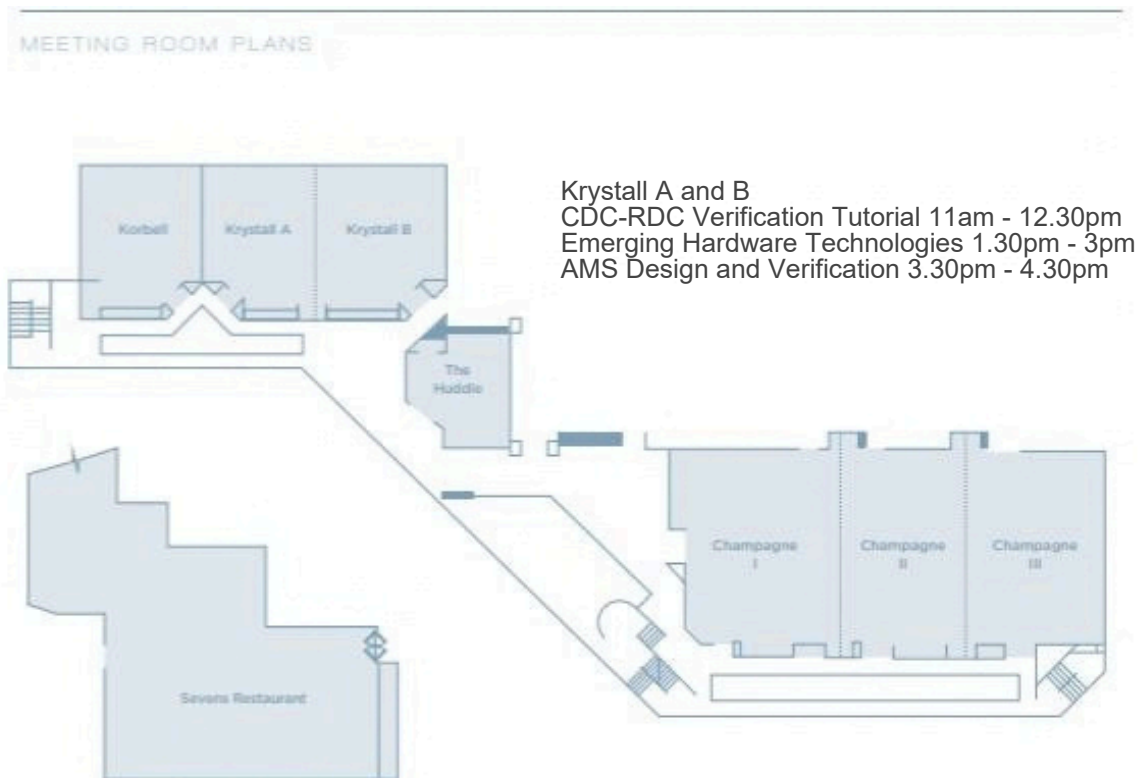
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San Jose Floor Plan



Krystall A and B
CDC-RDC Verification Tutorial 11am - 12.30pm
Emerging Hardware Technologies 1.30pm - 3pm
AMS Design and Verification 3.30pm - 4.30pm

Champagne I, II and III
Key Note 10.15am - 11am
Formal Verification and AI 11am - 12.30pm
Using AI in VLSI and DV 1.30pm - 3pm
Verifying Complex Systems 3.30pm - 4.30pm

Verification & Semiconductor Futures San Jose 2026



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Thursday, 8 October 2026 (Morning)

09:30 AM | Registration, Breakfast & Networking

10:15 AM | Welcome Note – Mike Bartley, Alpinum Consulting

10:20 AM | Pre-Keynote – Tessolve

10:30 AM | Opening Keynote – Sean Safarpour, AMD
Game Changer : AI Makes Verification Formal

Formal Verification and AI

11:00 AM | Tobias Ludwig, Lubis EDA
From Craft to System: A Platform Approach to
Structured and Automated Formal Verification

11:30 AM | Shankar Channabasappa,
Tessolve
System Verilog RTL generation using NL
Specification with AI tools

11:50 AM | Nayab Hossain, Chipster
Formal Verification via Data Generation &
Bi-directional Data Synthesis

12:10 PM | Ankit Kumar Garg, NVIDIA
Forward Progress: Formal Verification
beyond Function testing

12:30 PM |  Lunch Break

CDC-RDC Verification Tutorial

11:00 AM

**Bill Gascoyne,
Blue Pearl Solutions
&
Dammy Olopade, Google**

CDC-RDC Verification Standard 1.0
for Interoperable Abstract Model

Using AI in VLSI and DV

13:30 PM

Andy Bond, Olix

AVL - Where's the Catch?. Open Source, Feature Rich and AI ready

14:00 PM

Sasa Stamenkovic, Pure Silicon Solutions

Holistic Verification in the AI Era: Scaling Formal and Empowering Engineers

14:20 PM

Suraj Chakravarthi Raja, MathWorks

From Algorithm to Verified Silicon: Accelerating Semiconductor Design with Model-Based Design

14:40 PM

Oscar Gustafsson (Remote) Linköping University

Surfer - debugging digital waveforms on most platforms

15:00 PM

 **Refreshment Break & Networking**

Verifying Complex Systems

15:30 PM

Chiranjeevi Sirandas, NVIDIA

A UVM RAL Flow for Registers Protected Behind Access Control: Explicit Prediction, Extensions, Solved Identities

15:50 PM

Sivaharan Janahan, WRAXX Corp.

Your RTL Changed - Which Evidence Is Still Valid?

16:10 PM

Krupa Shah, Cisco Systems

When 100% Coverage Isn't Enough: Verifying Multi-Chiplet GenAI Platforms

16:30 PM

Conference Close

Emerging Hardware Technologies

13:30 PM

Gurpreet S. Kalsi, Intel

BiFrost: A Composable, Resilient Interconnect Network Architecture for Scalable AI Systems

14:00 PM

Frank Schirrmeister, Synopsys

Verifying Physical AI Systems: The Evolution of Software-Defined Hardware-Assisted Verification

14:20 PM

Allen Nejah, SunMan Engineering

From Silicon to Care: Engineering an AI Care Platform for Real-World Applications

14:40 PM

Abyarthana Bisoyi (Remote) Odisha University of Technology and Research

Co-Design and Verification of FPGA-Efficient CNNs and Next-Generation Deep Video Codecs

AMS Design and Verification

15:30 PM

Leon King, Cadence Design Systems

Beyond Circuits: Modeling Arbitrary Physics in Digital Verification

16:10 PM

Sandeep Sharma, Meta

AI-Assisted UVM-Based AMS Co-Simulation and Verification Methodology for Mixed-Signal Designs

Mike Bartley

CEO, Alpinum Consulting

Welcome Message :

Welcome to the Verification Futures Conference Austin 2025, which will be chaired by Mike Bartley from Alpinum Consulting.

Biography:

Mike has been involved in software testing and hardware verification since 1988 after completing a PhD in Math. He started his career in testing military software and safety-related aerospace applications using formal mathematical methods before moving into commercial software testing. Mike moved to semiconductor Design Verification (DV) in 1994 and has verified complex hardware products (on Silicon and FPGA) going into commercial and safety-related sectors such as mobile phones, avionics, automotive, comms, cloud/data servers, and, more recently, Artificial Intelligence. Mike built and managed state-of-the-art DV teams inside several companies (including STMicroelectronics, Infineon, Panasonic, and the start-up ClearSpeed), specialising in CPU verification and verifying over 15 different CPUs. Mike was invited to speak at many international conferences, helping him to become a well-known, global DV leader.

Mike founded and grew a DV services company to 450+ engineers globally, successfully delivering services and solutions to over 50+ clients on multiple continents and spanning the top 10 semiconductor companies through to start-ups, in various technologies and industries. He also advised several companies (ARM, NXP, and multiple start-ups) on organisational DV strategies. The company was acquired by Tessolve Semiconductors in 2020 and Mike worked at Tessolve as SVP in VLSI, managing the Centre of Excellence (CoE) for building new products and services across all Tessolve business units (VLSI, Test, PCB, and embedded SW) and developing AI capabilities and expertise across Tessolve. Mike is now running an AI and RTL to GDS VLSI services company Alpinum Consulting (www.alpinumconsulting.com) offering time-and-materials, fixed-price delivery-based, and full fixed-price turn-Key ASIC business models. Offices are both offshore and nearshore with development centres in Vietnam, India, Egypt, Eastern Europe, Mexico and Costa Rica.

Sean Safarpour

Fellow, AMD

Presentation Title:

Game Changer: AI Makes Verification Formal

Abstract:

On November 30th 2022, ChatGPT was publicly released. In 4 short years, we have seen our technical working world get transformed. AI-generated code now accounts for 70-90% of all new code at some companies. Token usage has increased 330X in the last two years alone, as people realize the benefits and impact of using AI in their daily tasks. This trend includes all aspects of hardware design and verification. In this talk I make the case that AI is the dream technology Formal Verification has been missing for decades. AI allows every formal barrier to be reduced to such an extent to drive tremendous deployment of formal verification. In a world where first-time silicon continues to be a challenge and verification cost/effort increases relentlessly³, Formal Verification will become the main verification approach in 5 years.

Speaker Biography:

Sean Safarpour is a Fellow at AMD, leading efforts in formal verification deployment, scaling, and innovation. Prior to AMD, he led the formal verification R&D team at Synopsys as Executive Director for four years, after six years as Director of Product and Application Engineering. He previously held director roles at Atrenta and was co-founder and VP at Vennsa. Sean received his PhD and Master's degrees from the University of Toronto and his Bachelor's from the University of British Columbia. He has 35+ papers, 5 patents, and 2 books to his name.



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Tobias Ludwig

CEO, LUBIS EDA

Presentation Title:

From Craft to System: A Platform Approach to Structured and Automated Formal Verification

Abstract:

Demand for new chips is outpacing the industry's capacity to verify them. Formal verification is a powerful guard against costly bug escapes, yet it remains a major effort sink, and projects still slip unpredictably toward sign-off. A closer look reveals why: alongside the expert work only domain specialists can do, sits a persistent layer of orchestration overhead, from extracting design information to updating verification plans and maintaining tool-specific scripts. This overhead is well-scoped and low-risk, precisely where AI can deliver value safely. But naive adoption fails, because formal verification demands the determinism and consistency that unguarded AI agents undermine.

The answer is a platform approach. This talk presents an AI-first platform built at LUBIS EDA that grounds automation within well-defined guardrails, making process discipline the default rather than a deliberate investment. The platform acts as a central cockpit for AI- and tool-based automations. It loads the design into the formal environment, extracts key I/Os and behaviors with generated descriptions, populates the verification plan, and maintains the scripts formal checks depend on, all feeding an integrated project view with no manual reporting overhead. The result is a clean separation of concerns: engineers focus on the work only they can do, while the platform owns everything else.

Speaker Biography:

Dr. Tobias Ludwig is CEO and co-founder of LUBIS EDA, where he leads the company's formal verification methodology and the development of the FormalOS infrastructure. A recognized expert in formal verification, Tobias is dedicated to helping semiconductor companies achieve more practical, predictable, scalable verification for today's most complex chip designs.



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Shankar Channabasappa

AVP Custom Silicon, Tessolve Semiconductor Inc

Presentation Title:

System Verilog RTL generation using NL Specification with AI tools

Abstract:

How to generate System Verilog RTL using NL Specifications? It is possible now with AI tools such as Claude, Cadence ChipStack AI Super Agent, Alpha Design AI ChipAgents, and Synopsys.ai Copilot. These tools are transforming front-end semiconductor design by converting specifications, microarchitecture documents, interface definitions, and register maps into draft SystemVerilog RTL, assertions, and verification collateral.

ChipStack and ChipAgents use multi-agent workflows with design-intent awareness, while Claude and other LLMs provide prompt-driven RTL generation and design assistance. These tools can significantly accelerate RTL development, verification planning, and debug activities.

However, generated RTL still requires expert review, simulation, linting, CDC/RDC analysis, formal verification, and signoff before production use.

Speaker Biography:

Shankar Channabasappa is a seasoned semiconductor technology leader with over two decades of experience spanning the complete ASIC development lifecycle, from architecture and specification through RTL design, verification, physical implementation, and GDSII signoff. He holds an M.S. in Electrical Engineering from the Indian Institute of Science (IISc), Bangalore, and has successfully built and led high-performance engineering teams across the United States and India.

His expertise includes high-performance networking and AI/ML SoCs, PCIe Gen5/Gen6, DDR memory subsystems, high-speed Ethernet, 200G SerDes, Interlaken, and ARM-based SoC architectures. He has led the development of silicon-proven products in advanced technologies, including TSMC N3P, enabling industry-leading performance, power efficiency, and area optimization for cloud, AI, and data center applications.



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Nayab Hossain

CEO, Chipster

Presentation Title:

Formal Verification via Data Generation & Bi-directional Data Synthesis

Abstract:

Formal verification is difficult to scale with AI because high-quality assertion and proof data remains scarce. This talk presents an approach to generating stronger verification data through automated formal feedback and bi-directional data synthesis. Using RTL, natural language specifications, SystemVerilog Assertions, proof results, counterexamples, non-vacuity checks, and coverage signals, the workflow creates iterative training and evaluation data for LLM- assisted verification. The presentation will discuss the architecture, data-generation process, experimental results, and the challenges involved in building more reliable autonomous formal-verification systems.

Speaker Biography:

Nayab Hossain is a Computer Engineering student at San José State University working on Chipster, an autonomous formal verification system for ASIC and SoC RTL designs. His work focuses on AI assisted assertion generation, formal proof, non-vacuity analysis, and verification automation. He is also in Plug and Play's accelerator program and has earned 10+ awards through engineering competitions and hackathons



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Ankit Kumar Garg

Senior Manager, Formal Verification, Nvidia

Presentation Title:

Forward Progress: Formal Verification beyond Function testing

Abstract:

This presentation talks about how formal verification can systematically find deadlock, livelock, and starvation bugs that escape simulation-based corner, random, and stress tests. Using real case studies, we also compare safety vs liveness assertions for forward-progress properties, explain when to use each, and share convergence techniques and RTL design guidelines. Formal liveness checks uncover substantially more forward-progress issues than safety-only approaches, highlighting why forward progress must be treated as a first-class verification goal, not a side effect of functional testing.

Speaker Biography:

Ankit Garg is Senior Formal Verification Manager at NVIDIA in Santa Clara, with over 18 years of semiconductor experience. He has held roles in RTL design, ASIC verification at Qualcomm, and formal applications engineering at Synopsys, and now leads a formal verification team working on CPU, GPU, and high-performance computing designs at NVIDIA.



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Bill Gascoyne

CDC-RDC Verification expert, Blue Pearl Solutions

Presentation Title:

CDC-RDC Verification Standard 1.0 for Interoperable Abstract Model

Abstract:

The Accellera CDC Working-Group aims to define a standard CDC-RDC IP-XACT/TCL model to be portable and reusable regardless of the involved verification tool. CDC-RDC analysis has evolved as an inevitable stage in RTL quality signoff in the last two decades. As the design sizes increased in every generation, the EDA tools could not handle running flatly and the only way of handling design complexity was through hierarchical CDC-RDC analysis consuming abstracts. Even with all this significant progress in capabilities of EDA tools the major bottleneck in CDC-RDC analysis of complex SOC's and Chiplets is consuming abstracts generated by different vendor tools.

Speaker Biography:

Currently works at Blue Pearl Solutions in documentation, training, and software QA
Previously worked as an AE and in technical training at LSI Logic, and in technical training at Magma Design Automation



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Dammy Olopade

Team Lead , Google

Presentation Title:

CDC-RDC Verification Tutorial

Abstract:

The Accellera CDC Working-Group aims to define a standard CDC-RDC IP-XACT/TCL model to be portable and reusable regardless of the involved verification tool. CDC-RDC analysis has evolved as an inevitable stage in RTL quality signoff in the last two decades. As the design sizes increased in every generation, the EDA tools could not handle running flatly and the only way of handling design complexity was through hierarchical CDC-RDC analysis consuming abstracts. Even with all this significant progress in capabilities of EDA tools the major bottleneck in CDC-RDC analysis of complex SOC's and Chiplets is consuming abstracts generated by different vendor tools.

Speaker Biography:

Dammy is a Technical Lead at Google, where he leads Quality and Innovation in building AI platforms. Previously at Intel, he built, managed and led teams as a technical contributor. His Quality work focused on the prevention of metastability issues, innovated new tools/solutions with leading EDA companies for CDC, RDC etc. His multi-disciplinary expertise has been essential in tackling complex challenges. His Innovation work centered on taking key technologies from incubation to products, making sure the culture/environment supported the nurturing of creative ideas, and the corporation appropriately invested in the future, as it focused on executing on the flagship projects. He is an avid mentor who prioritizes relationships (faith, family, friends)



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Andy Bond

Director RTL and Verification, OLIX

Presentation Title:

AVL – Where’s the Catch?. Open Source, Feature Rich and AI ready

Abstract:

AVL – The Apheleia Verification Library was released in 2025, an open-source Python based verification library with VIP and full simulator support. One year on, what has changed and what have we learnt.

Primarily we’ve learnt to support the community. Through them we’ve seen significant performance improvements, user focused VIP development and the efficiency advantages of running testbenches tightly integrated with AI.

Speaker Biography:

Andy Bond has over 25 years industry experience as a design and verification engineer, manager and leader.

He developed AVL to combine the advantages of UVM, CocoTB and Python together in a completely free and open-source environment. By enabling commercial grade verification to anyone with a laptop, without the overhead of bloated methodologies, we can bring cutting-edge verification to universities, start-ups and multi-nationals.

In his role as Director of RTL and Verification at OLIX he’s working with some of the best minds in the industry to solve the most consequential problem in the development of frontier AI.



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Sasa Stamenkovic

Principal Engineer, Formal Verification, Pure Silicon Solutions

Presentation Title:

Holistic Verification in the AI Era: Scaling Formal and Empowering Engineers

Abstract:

Modern SoC verification demands more than a single methodology. This presentation explores a holistic approach that combines targeted formal verification, scalable simulation, deep collaboration between verification and design teams, and guided AI acceleration. Through practical examples, we examine how decomposition and sound abstraction make formal verification effective on complex designs, while dual-runnable environments help connect formal and simulation. We then explore how AI agents can act as supervised “junior engineers,” accelerating testbench development, environment bring-up, and counterexample triage. The result is a verification strategy that scales engineering capacity while keeping human expertise and design intent at its core.

Speaker Biography:

Sasa Stamenkovic is a Principal Engineer and Formal Verification Leader at Pure Silicon Solutions, with 15 years of experience in hardware design verification and formal verification. Since graduating with an MS in VLSI Engineering from the University of Novi Sad in 2010, he has focused his career on formal methods, continuously adopting and developing new verification methodologies and techniques.

Before joining Pure Silicon Solutions, Saša spent more than a decade at OneSpin Solutions and Siemens, working with semiconductor companies and engineering teams to apply formal verification to complex hardware designs. His experience spans a broad range of designs and verification challenges, with a particular focus on developing practical formal verification solutions that help teams achieve confidence and convergence on complex designs.



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Suraj Chakravarthi Raja

Application Engineer, MathWorks

Presentation Title:

From Algorithm to Verified Silicon: Accelerating Semiconductor Design with Model-Based Design, Shift-Left Verification, and AI

Abstract:

As semiconductor devices grow in complexity, engineering teams face increasing pressure to meet ambitious performance, power, schedule, and quality objectives. This presentation explores how Model-Based Design and shift-left verification methodologies help teams identify and resolve issues earlier in the development process.

Attendees will learn how Model-Based Design supports workflows spanning algorithm development, architectural exploration, HDL generation, high-level synthesis (HLS), and verification. The session also examines the emerging role of agentic AI and highlights real-life case studies demonstrating improved productivity, design quality, and time to silicon.

Speaker Biography:

Suraj Chakravarthi Raja is an Application Engineer working in the areas of signal processing, controls, embedded AI, and HDL code generation at MathWorks. With a PhD in Electrical Engineering from the University of Southern California, Suraj has a decade of experience in hardware-software codesign of low-latency embedded accelerator pipelines for humanoid robotics applications. His prior work was funded by DARPA, NIH, NSF, and DoD. He also has master's degrees from USC in Electrical Engineering and Computer Engineering.

Oscar Gustafsson

Associate Professor, Linköping University

Presentation Title:

Surfer – debugging digital waveforms on most platforms

Abstract:

The open-source multi-platform waveform viewer Surfer is introduced. Features and design principles are presented, including some firsts in the open-source world and some likely unique even considering commercial tools. We give examples of how Surfer can communicate with other programs and how this can be beneficial for debugging and understanding designs. Finally, the road map for future development is outlined.

Speaker Biography:

Oscar Gustafsson is an associate professor at the Division of Electronics and Computer Engineering, Linköping University, Sweden. His research interests include design and implementation of computations, typically for communication systems, ranging from algorithms and architectures down to arithmetic circuits, as well as tools to help with the design and implementation. He has published and co-published more than 200 scientific papers in international journals and conferences and is a regular contributor to many open-source projects.



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Gurpreet Singh Kalsi

Principal Engineer, Intel

Presentation Title:

BiFrost: A Composable, Resilient Interconnect Network Architecture for Scalable AI Systems

Abstract:

AI scaling is increasingly limited by communication, memory, and system complexity. BiFrost is a composable interconnect architecture that unifies communication across chiplets, packages, and large-scale systems. A scalable FatTree fabric, shared address space, and packet-address compute engine enable software-transparent resource composition, while adaptive routing and dynamic remapping provide resilience under failures. BiFrost demonstrates how a unified fabric can simplify AI system design, improve scalability and programmability, and enable the next generation of composable AI infrastructure.

Speaker Biography:

Gurpreet Singh Kalsi is a Principal Engineer in Intel's Datacenter Group, specializing in large-scale system architecture, AI infrastructure, and hardware-software co-design. Over two decades at Intel, he has contributed to more than 10 revenue-generating silicon programs and led innovations spanning AI accelerators, GPU architectures, memory systems, and high-performance networking. He has held technical leadership roles across Intel and U.S. Government research programs, enabling scalable system connectivity through silicon photonics and co-packaged optics technologies. Gurpreet holds over 50 issued or submitted patents, has published more than 20 papers in leading IEEE venues, and is the lead author of BiFrost, a composable interconnect architecture for scalable AI systems.



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Allen Nejah

Founder and Chief Executive Officer, SunMan Engineering, Inc.

Presentation Title:

Product Development from Concept to Production at SunMan Engineering

Abstract:

This presentation examines SunMan Engineering's approach to developing electronic and Mechanical products, from requirements and feasibility studies through system architecture, component selection, PCB design, firmware, and mechanical integration. Allen Nejah will discuss practical challenges in coordinating engineering disciplines, building prototypes, validating performance, and preparing designs for manufacturing. The session will highlight how early technical decisions affect cost, schedule, and product reliability. SunMan's AI Care Platform will serve as one example of integrating sensors, embedded processing, connectivity, and software into a complete system.

Speaker Biography:

Allen Nejah is Founder and CEO of SunMan Engineering, Inc., a San Jose company focused on electronic and Mechanical product design and development. He leads engineering programs that bring together system architecture, custom electronics, embedded firmware, mechanical design, and prototyping. His work includes helping customers define requirements, evaluate technical feasibility, and develop products through successive design and testing stages. Alongside customer development programs, Allen leads SunMan's AI Care Platform initiative. He also mentors senior engineering projects at San José State University.



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Frank Schirrmeister

Executive Director, Strategic Programs, Synopsys

Presentation Title:

Verifying Physical AI Systems: The Evolution of Software-Defined Hardware-Assisted Verification

Abstract:

Physical AI systems, from autonomous vehicles and robotics to intelligent edge devices, are driving a new era of verification. Unlike traditional AI workloads, these systems must continuously interact with the physical world, requiring validation of hardware, software, sensors, power behavior, and real-time decision making. This presentation examines how hardware-assisted verification is evolving toward software-defined, and hybrid architectures that combine emulation, prototyping, and virtual platforms. We explore the growing bifurcation between hyperscale AI infrastructure and Physical AI systems, the role of AI-assisted verification workflows, and emerging methodologies that enable software bring-up, system validation, and power-performance analysis long before silicon is available.

Speaker Biography:

Frank Schirrmeister is Executive Director, Strategic Programs, System Solutions in Synopsys' Market and Products Group. He leads strategic activities across system software and hardware assisted development for industries like automotive, data center and 5G/6G communications, as well as for horizontals like Artificial Intelligence / Machine Learning. Prior to Synopsys, Frank held various senior leadership positions at Arteris, Cadence Design Systems, Imperas, Chipvision, and SICAN Microelectronics, focusing on product marketing and management, solutions, strategic ecosystem partner initiatives, and customer engagement. He holds an MSEE from the Technical University of Berlin and actively participates in cross-industry initiatives as Panel Chair of the Design Automation Conference.



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Abhyarthana Bisoyi

Assistant Professor, Odisha University of Technology and Research

Presentation Title:

Co-Design and Verification of FPGA-Efficient CNNs and Next-Generation Deep Video Codecs

Abstract:

Deploying deep learning at the resource constrained edge requires a paradigm shift in hardware software codesign. This presentation details state of the art architectures for FPGA efficient convolutional neural networks and deep video codecs. We exploit hardware aware hybrid model compression, utilizing column-based bit level sparsity, mixed precision quantization, and sparsity aware multipliers to reduce on chip dynamic power. Furthermore, we explore scaling neural video coding models and leveraging multimodal large language models for semantic reconstruction. Finally, we establish rigorous verification and hardware emulation strategies to guarantee functional accuracy while maximizing energy efficiency for edge deployed autonomous vision systems.

Speaker Biography:

Mrs. Abhyarthana Bisoyi is an Assistant Professor in the School of Electronic Sciences at Odisha University of Technology and Research (OUTR). She has completed her Bachelors in Electronics and Communication Engineering in the year 2011 and Masters from National Institute of Technology Rourkela (NIT Rourkela) in Electronics and Instrumentation Engineering in the year 2013. From then to now, she has teaching experience of more than 12 years. She has guided 22 Masters students and more than 100 undergraduate students. She is currently pursuing her PhD from OUTR and her research area includes Digital VLSI, FPGA, CNN, Approximate and Neuromorphic Computing.



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Chiranjeevi Sirandas

Senior Verification Engineer, NVIDIA

Presentation Title:

Extending UVM RAL for Application-Specific Register Verification

Abstract:

As hardware designs evolve, register verification must handle new access rules and a wider range of requirements. This presentation shows how to extend UVM RAL while keeping existing tests and sequences unchanged. It uses registers protected by access control as an example. The adapter selects a valid requestor for normal accesses. Extensions let tests choose invalid requestors to check that access is denied. A shared register database provides policy information, while the predictor helps keep the register model accurate. The approach focuses on simple design, easy maintenance, and support for future requirements with limited changes to the existing verification environment.

Speaker Biography:

Chiranjeevi Sirandas is a Senior Verification Engineer at NVIDIA with experience in ASIC microarchitecture, design, verification, and validation. His work spans PCIe-based DMA, SmartNICs, high-speed networking, and crossbar interconnects. He has developed testbenches at the chip, subsystem, and unit levels using SystemVerilog and UVM, including constrained-random and self-checking environments. His background also includes testbench architecture, test planning, system prototyping, and validation.

Sivaharan Janahan

Founder, WRAXK Corp.

Presentation Title:

Your RTL Changed – Which Evidence Is Still Valid?

Abstract:

When RTL or configuration changes, teams know which tests can run again. A harder question is whether evidence accepted for the previous release still supports the new one. This talk separates regression selection from evidence validity and uses a Release A-to-B example to show two outputs: the status of prior evidence and the new work created by the change. It introduces a release-linked Passport that records the reasoning, assumptions and limits. Sometimes full regression is correct, and reduced revalidation must be measured rather than assumed.

Speaker Biography:

Sivaharan Janahan is the founder of WRAXK Corp., where he is developing a release-evidence continuity system for semiconductor assurance. His work asks which earlier evidence remains usable after RTL, configuration or security-intent changes, which work must be repeated, and what new obligations were created. WRAXK combines release-specific analysis, change-impact reasoning and a durable evidence Passport. Sivaharan is testing the method through synthetic benchmarks, independent technical review and historical release discussions with semiconductor verification practitioners.



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Krupa Shah

ASIC Engineering, Technical Leader, Cisco Systems, Inc.

Presentation Title:

When 100% Coverage Isn't Enough: Verifying Multi-Chiplet GenAI Platforms

Abstract:

Your chiplet passed verification. Your partner's chiplet passed verification. Yet integration failures still appear at die boundaries. The presentation outlines the major verification problems emerging in GenAI-era platforms and the methodology evolution needed across tools, flows, and industry standards. It goes deeper into challenges like limited visibility into encrypted vendor models, poor reuse of pre-silicon environments, coverage that stops at die edges, and debug that loses context across package boundaries. GenAI workloads amplify these gaps through greater scale, vendor heterogeneity, and faster integration pressure.

Speaker Biography:

Krupa Shah is an ASIC Engineering Technical Leader at Cisco Systems in San Jose and an IEEE Senior Member. With over 20 years in the semiconductor industry, she specializes in verification across IP, subsystem, SoC, and multi-die levels using System Verilog and UVM. She is also a co-author of a paper under-review at IEEE Micro on GenAI-era chiplet verification. Her work focuses on multi-chiplet SiP integration and verification closure, with deep experience in PCIe, AMBA, DDR MultiPHY, and SerDes. Previously contributed at Intel/Altera, Synopsys, and Cadence, she led NiosV RISC-V verification, Open FPGA Stack and PCIe acceleration programs.



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Leon King

Senior Principal Product Validation Engineer, Cadence Design Systems

Presentation Title:

Beyond Circuits: Modeling Arbitrary Physics in Digital Verification

Abstract:

Most systems include some non-circuit elements. Complete verification of these systems requires including important behaviors of the non-circuit elements within digital verification simulations. This work reviews SystemVerilog behavioral modeling techniques that can be used to simulate a variety of non-circuit system elements. It includes relevant examples demonstrating the use of these modeling techniques.

Speaker Biography:

Leon King is a Senior Principal Product Validation Engineer and Solutions Expert at Cadence Design Systems with 25+ years of experience in mixed-signal simulation and verification. He specializes in the Xcelium Mixed-Signal App technologies including Real Number Modelling, SPICE/HDL co-simulation with Spectre, and developing best-in-class Mixed Signal Verification methodologies based on customer requirements. He is currently exploring AI based solutions to enable more seamless Mixed Signal Verification workflows. He holds a BS in Electrical & Computer Engineering from the University of California, Davis.



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Sandeep Sharma & Vijay Akkaraju

**Analog & Mixed Signal Design Verification Engineer, Meta &
Product Engineering: Analog Mixed Signal, Cadence Design Systems**

Presentation Title:

AI-assisted UVM-based AMS co-simulation and verification methodology for mixed signal designs

Abstract:

Analog content in modern SoCs keeps growing, yet AMS verification still lags digital in automation. This talk outlines a practical path to close that gap. It first revisits a UVM-based, digital-on-top methodology presented at DVCon US 2024, in which one testbench drives both SystemVerilog real-number models and SPICE netlists, enabling nightly mixed-signal regressions, constrained-random stimulus and assertions on analog nets. It then explores how AI agents can remove the next bottleneck, behavioral modeling, by generating models, checkers and testbenches from schematics, and closes with five high-impact opportunities for agentic AI across analog design and verification.

Speaker Biography:

Sandeep Sharma is an Analog & Mixed Signal Design Verification Engineer at Meta Reality Labs, focused on mixed-signal verification methodology for analog IP and SoCs, spanning UVM-based AMS co-simulation, SystemVerilog real-number modeling and AI-assisted automation. Sandeep presented a UVM-based AMS co-simulation methodology at DVCon US 2024 and is passionate about bringing the rigor of digital verification to analog.

Vijay Akkaraju works in AMS Product Engineering at Cadence Design Systems, partnering with customers and R&D on verification flows. Vijay brings 25+ years of mixed-signal experience, including IC design at Analog Devices and 14 years as an AMS specialist at Synopsys.



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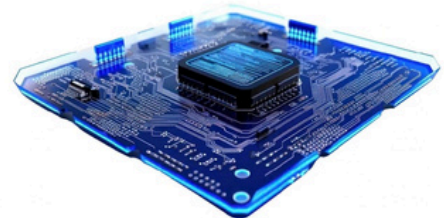
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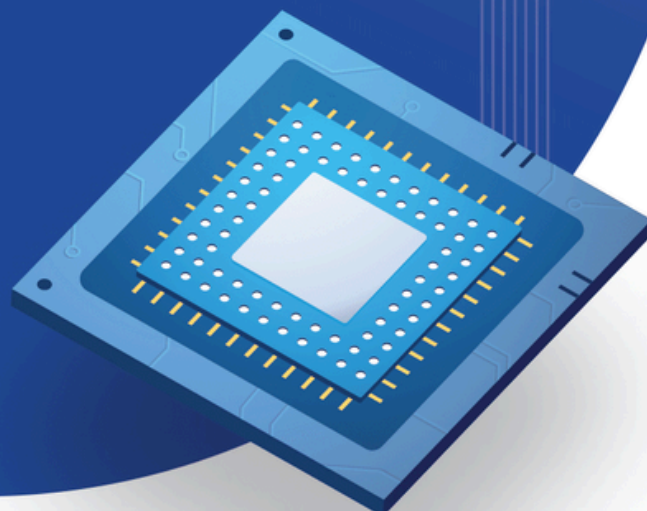
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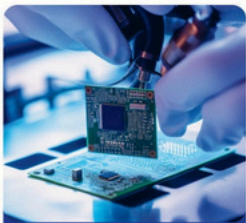
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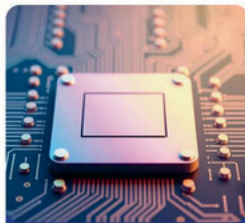
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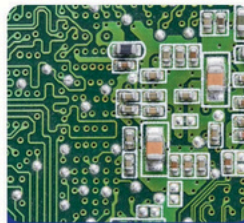
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