

Verification Futures Conference Austin 2025



Wednesday,
12 November 2025



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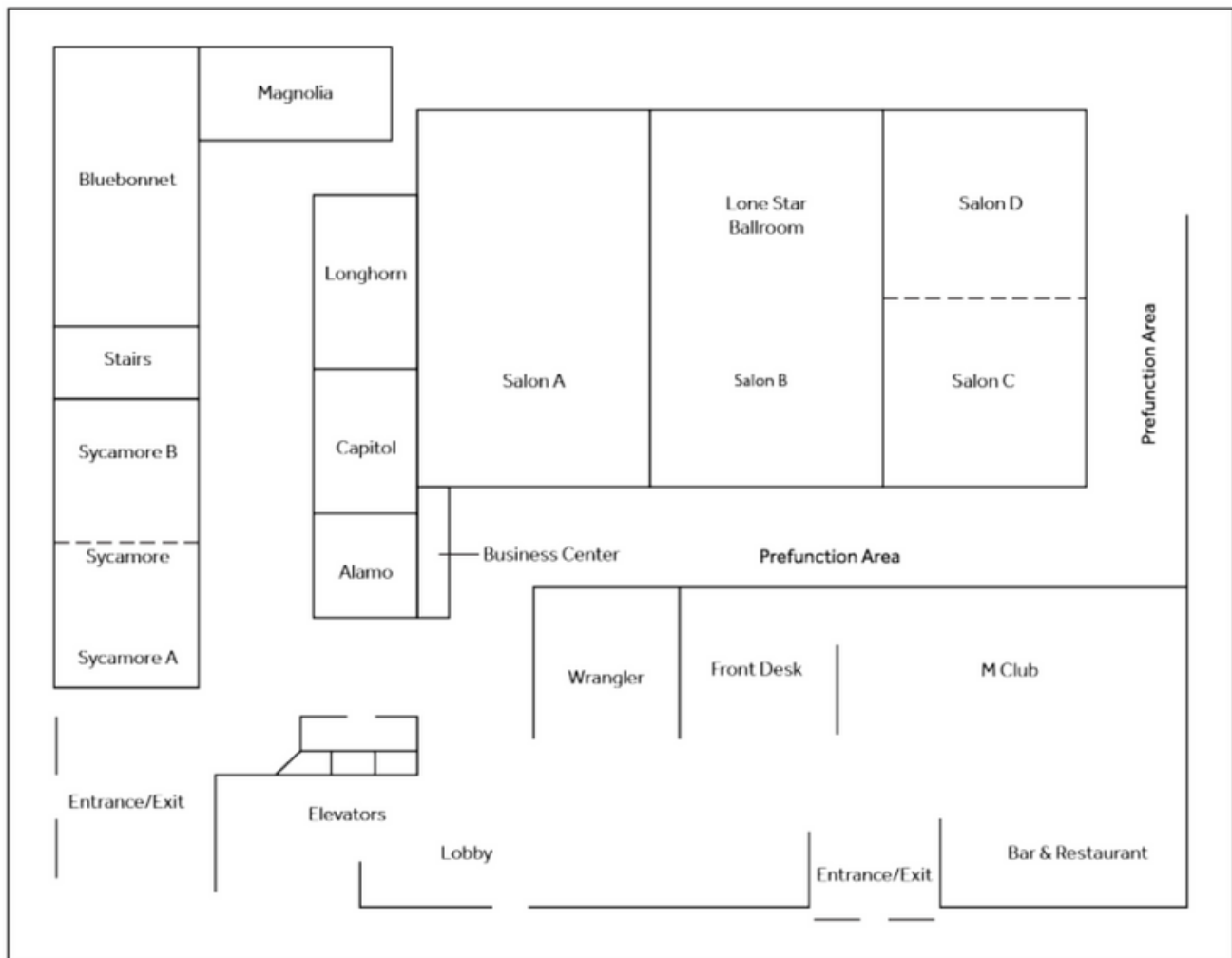
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FLOOR PLAN



Agenda

08:30	Arrival: Breakfast and Networking		
09:25	Welcome: Mike Bartley , Alpinum Consulting		
09:30	Revitalizing Semiconductor Startups Keynote - Tarun Verma , Managing Partner, Silicon Catalyst		
10:15	Overcoming the Challenges of Blending Hardware Verification Expertise with AI and Machine Learning Keynote Challenge Paper - Sohil Sri Mani Yeshwanth Grandhi - NVIDIA Corporation		
10:30	Acceleration of Complex RISC-V Processor Verification Using Test Generation Integrated with Hardware Emulation Wei-Hua Han - Synopsys		
11:00	Refreshments and Networking		
11:30	Verifying Heterogeneous Systems	Doulos KnowHow Tutorial: Beginner's Guide to Using AI for Hardware Engineering	Emerging Hardware Technologies and Startups
11:30	Static Sign-Off Methodologies: Liberating Functional Verification from Boolean Shackles Prakash Narain - Real Intent	Beginner's Guide to Using AI for Hardware Engineering Doug Smith	11:30–11:40 Overview of Si Catalyst Tarun Verma , Silicon Catalyst
11:50	Property Generator: simple generation of Formal Assertion IP Dr. Tobias Ludwig - LUBIS EDA		11:40–12:00 Emerging Trends in AI for Chip Design and EDA David Z. Pan , The University of Texas at Austin

12:10	Harnessing Agentic AI to Accelerate Verification Chuck Alpert , Cadence	12:00–12:15 Ultra-fast AI Inference at the Edge Frank Thiel , Gigantor Technologies 12:15–12:30 New sensing technologies providing insight inside batteries Rick Seger, SigmaSense
12:30	Lunch and Networking	
13:30	Improving Verification to Accelerate Shift-Left	
13:30	Bridging the Gap: A Practical Roadmap to Formal Verification for DV Engineers Gilberto Migliorin , Synopsys	
14:00	AI Agents for DV Debug Jeffrey Pan , Bronco AI, Inc.	
14:20	Improving verification to Accelerate Shift-Left Sheela Pillai	
14:40	The Intelligent Verification: Reinventing 5 DV Workflows with AI Shelly Henry - Moores Lab AI	
15:00	Refreshments and Networking	

15:30	Real Examples of Applying GenAI and Formal Verification	Doulos KnowHow Tutorial: Practical Asynchronous SystemVerilog Assertions	Continuing Progress in Verification: A Mixed Signal Approach
15:30	Rethinking AI Inference and Hardware Verification through Differentiable Logic Gate Networks (difflogic) Georg Meinhardt , DiffLogic Inc.	Practical Asynchronous SystemVerilog Assertions Doug Smith	Overcoming Obstacles to Model-based Verification Daniel Cross - Cadence Design Systems
15:50	Applying Generative AI in Post-Silicon Validation: Real Use Cases and Technical Insights Santosh Appachu Devanira Poovaiah - NVIDIA Corporation		Modelling a 4-Level DCDC Converter Using EEnets Abhijit Madhu Kumar - Cadence Design Systems
16:10	Deploying AI in DV for Smarter and Faster IP Verification Arjumand Yaqoob - Qualcomm Incorporated		Practical Approaches to Adopting State of the Art Mixed Signal Solutions Umar Lyles - Cirrus Logic
16:30	Event Closes		

Mike Bartley

CEO, Alpinum Consulting

Welcome Message :

Welcome to the Verification Futures Conference Austin 2025, which will be chaired by Mike Bartley from Alpinum Consulting.

Biography:

Mike has been involved in software testing and hardware verification since 1988 after completing a PhD in Math. He started his career in testing military software and safety-related aerospace applications using formal mathematical methods before moving into commercial software testing. Mike moved to semiconductor Design Verification (DV) in 1994 and has verified complex hardware products (on Silicon and FPGA) going into commercial and safety-related sectors such as mobile phones, avionics, automotive, comms, cloud/data servers, and, more recently, Artificial Intelligence. Mike built and managed state-of-the-art DV teams inside several companies (including STMicroelectronics, Infineon, Panasonic, and the start-up ClearSpeed), specialising in CPU verification and verifying over 15 different CPUs. Mike was invited to speak at many international conferences, helping him to become a well-known, global DV leader.

Mike founded and grew a DV services company to 450+ engineers globally, successfully delivering services and solutions to over 50+ clients on multiple continents and spanning the top 10 semiconductor companies through to start-ups, in various technologies and industries. He also advised several companies (ARM, NXP, and multiple start-ups) on organisational DV strategies. The company was acquired by Tessolve Semiconductors in 2020 and Mike worked at Tessolve as SVP in VLSI, managing the Centre of Excellence (CoE) for building new products and services across all Tessolve business units (VLSI, Test, PCB, and embedded SW) and developing AI capabilities and expertise across Tessolve. Mike is now running an AI and RTL to GDS VLSI services company Alpinum Consulting (www.alpinumconsulting.com) offering time-and-materials, fixed-price delivery-based, and full fixed-price turn-Key ASIC business models. Offices are both offshore and nearshore with development centres in Vietnam, India, Egypt, Eastern Europe, Mexico and Costa Rica.

Notes

Tarun Verma

Managing Partner, Silicon Catalyst

Keynote

Presentation Title:

Revitalizing Semiconductor Startups

Abstract:

Startups are a critical part of the semiconductor ecosystem and have been since the birth of the industry. Startups are integral to growth and innovation in the industry as they are capital efficient vehicles to explore new frontiers of chip technology and scale these from proof of concept to commercialization. Characteristically, startups in the semiconductor sector face significant challenges including scarce venture capital, non-trivial prototyping expenses, and significant time and resources needed to achieve produce-market fit. An overview of the investing landscape and recent promising developments in the semiconductor startup ecosystem will be described.

Speaker Biography:

Tarun Verma has over 25 years of experience in the semiconductor industry, with varied leadership and technology management roles in operations and engineering. Tarun joined Silicon Catalyst in 2015 as the first non-founder employee. Prior to that, he spent 22 years with Altera (now Intel PSG) where he led the packaging efforts for the organization. Tarun has Bachelors in Technology from Indian Institute of Technology, Kanpur, India and and MS in Materials Science from the University of California at Berkeley.



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Sohil Sri Mani Yeshwanth Grandhi

Senior Compiler Verification Engineer , NVIDIA Corporation

Keynote Challenge Paper

Presentation Title:

Overcoming the Challenges of Blending Hardware Verification Expertise with AI and Machine Learning

Abstract:

Verification complexity is exploding. While traditional methods are the bedrock of quality, new technologies like Machine Learning (ML) and Large Language Models (LLMs) offer powerful, but distinct, advantages. The challenge is knowing which tool to use—and when. In this talk, I'll draw on my experience at Intel and NVIDIA to break down common verification challenges, from endless regression cycles to debugging complex failures. I'll discuss frequent mistakes in adopting new technologies and present a clear-eyed approach for integrating them. We'll explore practical applications: using ML for predictive tasks like performance trend analysis and intelligent test selection, and leveraging LLMs for parsing logs, generating coverage models, and automating documentation. I'll share best practices for building a hybrid strategy that plays to the strengths of each method.

Speaker Biography:

Sohil Grandhi is a Senior Compiler Verification Engineer at NVIDIA Corporation with over six years of experience specializing in software development, test automation, and machine learning. His career, which includes roles at NVIDIA and Intel Corporation , has been focused on developing innovative automation frameworks that significantly reduce testing time and costs. Sohil holds two Master's degrees: one in Computer Science and Engineering from Pennsylvania State University and another in Machine Learning and Artificial Intelligence from LJMU.



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Wei-Hua Han

Senior Architect, Protocol Solutions Engineering, Synopsys

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Presentation Title:

Acceleration of Complex RISC-V Processor Verification Using Test Generation Integrated with Hardware Emulation

Abstract:

Simulation performance has long been seen as the bottleneck to design verification. Performance in the thousands of instructions per second, even tens of thousands of instructions per second, makes running long tests on complex designs difficult. However, long tests and complex stimulus are required to put complex processors into interesting states where micro-architectural bugs are more readily found.

With RISC-V processors and processing subsystems adding features including custom instructions to support high performance computing (HPC), AI, and automotive use cases among others, verification throughput becomes critical to achieving functional coverage closure.

While running software for various use cases is a necessary piece of the verification plan, this does not sufficiently stress the Device Under Test (DUT) and drive it into corner cases. Micro-architectural features such as caches and complex memory transitions are very difficult to verify without long-running, synthetic tests. For example, the simple scenario of filling up a 4MB L3 cache using single byte memory operations needs more than 4 million instructions to execute. Bugs in these micro-architectural areas not only lead to functional issues but may also introduce security vulnerabilities.

Two problems then need to be solved. First, interesting and relevant tests need to be generated, and second, a high-performance test execution platform and environment is required to achieve higher verification throughput.



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This presentation describes a solution to these problems using the STING test generator and the ZeBu hardware emulation platform. Multiple obstacles were overcome in implementing this solution:

- Configuring and extending the test generator for the complex processors and subsystems of interest
- Integrating test generation with hardware emulation using a transactor, and optimizing the interface so that there is no time wasted between one test and the next, resulting in close to 5000x speedup in test execution as compared to RTL simulations
- Extending debug and functional coverage tools to work in this environment

To demonstrate the viability of this solution, the open source XiangShan (superscalar, out-of-order) RISC-V processor was used. It supports the RV64GCBK extensions and includes L2 and L3 cache for multi-hart configurations. This presentation will discuss how the obstacles noted above were overcome, and detail some interesting bugs found using this environment.

Speaker Biography:

Weihua Han is a Sr. Architect Application Engineer at Synopsys Protocol Solution Engineering team. Weihua graduated from Beijing University of Posts and Telecommunications with Master of Science degree. For more than 20 years Weihua has been working on different aspects of functional verification with simulation and HAV (hardware-assisted verification), using SystemC, SystemVerilog, UVM and PSS. Weihua is now focusing on RISC-V related functional verification solutions.



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Prakash Narain

CEO & Founder, Real Intent

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Presentation Title:

Static Sign-Off Methodologies: Liberating Functional Verification from Boolean Shackles

Abstract:

Engineering teams are increasingly prioritizing early functional verification, achieving targeted verification and sign-off across more domains during RTL design—well before simulation. This early sign-off approach dramatically reduces downstream engineering changes and iterations. Successfully deploying sign-off during RTL design requires both tool speed and the scalability to handle IPs and SoCs, along with complete coverage that detects all targeted errors. Because static sign-off leverages abstract checking methods rather than the Boolean analysis used by simulation and formal verification, it delivers 10–100X faster runtimes, multi-billion-gate capacity, and a more efficient setup process. Additionally, its support for user-defined rules enables in-depth analysis for emerging applications where design requirements continue to evolve. Multiple experts will share production-proven methodology advances and best practices across key static sign-off applications, including: 1) RTL linting, 2) clock domain crossing, 3) reset domain crossing, 4) design-for-testability, 5) connectivity and glitch detection, and 6) hardware security sign-off. Attendees will gain a deeper understanding of static sign-off methodologies, along with practical insights tailored to specific applications.

Speaker Biography:

Dr. Prakash Narain is founder, president & CEO of Real Intent. His career spans IBM, AMD and Sun where he got hands on experience with all aspects of IC design, CAD tools design and methodology. He was the project leader for test and verification for UltraSPARC III at Sun Microsystems. He was an architect of the Mercury Design System at AMD. He has architected and developed CAD tools for test and verification for IBM EDA. Dr. Narain has a Ph.D. from the University of Illinois at Champaign-Urbana where his thesis focus was on algorithms for high level testing and verification.



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Dr. Tobias Ludwig

CEO, LUBIS EDA

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Presentation Title:

Property Generator: simple generation of Formal Assertion IP

Abstract:

The Property Generator is a proprietary tool developed by LUBIS EDA to simplify and accelerate formal verification. It results in correct-by-construction assertions, human readable, and, lastly, removes the need for a review of the assertions. The verification journey begins with writing a SystemC model that expresses functional intent. This model can be simulated using standard C++ and SystemC techniques, helping designers and verification engineers validate functionality early. The Property Generator then analyzes the model to autocompile assertions that comprehensively describe the expected behavior. Afterwards, the assertions are loaded together with the RTL design into a formal tool of your choice (or a simulator). In a typical setup, these assertions must be manually bound to RTL design signals—a process that is time-consuming and error-prone. To address this, the Property Generator integrates an AI-Refinement add-on, powered by Large Language Models (LLMs). These models can interpret both the abstract model and RTL structure, performing the refinement step with high accuracy and minimal user intervention.

Speaker Biography:

Dr. Tobias Ludwig is the CEO and co-founder of LUBIS EDA, a company specializing in electronic design automation (EDA) tools and formal verification consulting. He earned his Ph.D. in Electronic Design Automation from the University of Technology Kaiserslautern in 2021. During his doctoral studies, Dr. Ludwig identified inefficiencies in traditional formal verification processes within the semiconductor industry. This insight led him to work on an automated EDA software solution aimed at enhancing development processes and ensuring high-quality, efficient outcomes. Collaborating with Dr. Michael Schwarz and Dr. Max Birtel, he co-founded LUBIS EDA to advance formal verification in the semiconductor industry. Under Tobias' leadership, LUBIS EDA has focused on automating formal verification to uncover simulation-resistant and corner-case bugs in high-risk silicon designs. The company integrates cutting-edge tools and AI techniques to make formal verification more accessible and effective.



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Chuck Alpert

Fellow, Agentic AI, Cadence

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Presentation Title:

Harnessing Agentic AI to Accelerate Verification

Abstract:

This presentation, led by Chuck Alpert, Fellow, Agentic AI, explores the transformative impact of Agentic AI on digital verification. It highlights the application of AI in the automation of verification tasks leading to an increase in overall engineering efficiency. Key topics include AI-driven logic simulation, conversational LLM agents, and the integration of Agentic AI across the verification process. The ultimate goal is to leverage AI to reduce verification costs, improve productivity, and close the engineering resource gap, thereby accelerating the development of integrated circuits (ICs).

Speaker Biography:

Charles (Chuck) Alpert is Cadence's AI Fellow and drives cross-functional Agentic AI solutions throughout Cadence's software stack. Prior to this, has lead various pioneering teams in digital implementation, including Global Routing, Clock Tree Synthesis, Genus Synthesis, and Cerebrus AI. Charles has published over 100 papers and received over 100 patents in the EDA space. He is a Cadence Master inventor. He has served as Deputy-Editor-in-Chief for IEEE Transactions on Computer-Aided Design, chaired the IEEE/ACM Design Automation Conference, and earned IEEE Fellow. He received a B.S. and B.A. Degree from Stanford University and a Ph.D. in Computer Science from UCLA.



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Doug Smith

Engineer / Instructor, Doulos

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Presentation Title:

Beginner's Guide to Using AI for Hardware Engineering

Abstract:

Much hype surrounds AI. AI can generate some amazing results from answering complicated questions to generating video that looks convincingly real. Even so, AI has not yet changed the way hardware engineering is accomplished in our day-to-day projects. Many of us are reluctant to use AI, knowing that it has limitations and often produces unreliable results. Furthermore, there are issues of privacy, security, and even legality of using AI for project work. In this session, we explain the basic concepts behind using AI for engineering. We answer questions like "what are its requirements?", "how do large language models work?", "how does AI interact with other applications?", "what makes a good input prompt?", "how do I get started using AI?", "what are the uses for AI in engineering?", and many others. We show how you can tie in an AI model into your engineering workflow or even create an agentic workflow. If you are just getting started using AI, then join us to see how to practically put AI to work in your next project.

Speaker Biography:

Doug Smith is a verification engineer and instructor for Doulos based in the Austin Texas area with expertise in SystemVerilog, UVM, and formal verification. At Doulos, he delivers training in verification methodologies, hardware description languages, and formal technology.

Doug holds a masters degree in Computer Engineering from the University of Cincinnati and a bachelors degree in Physics and Biology from Northern Kentucky University. Currently, he resides in Paige Texas with his wife and family on a small farm where he raises bees, horses, chickens, and pigs and loves playing around on his tractor.



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Tarun Verma

Managing Partner, Silicon Catalyst

Presentation Title:

Overview of Si Catalyst

Speaker Biography:

Tarun Verma has over 25 years of experience in the semiconductor industry, with varied leadership and technology management roles in operations and engineering. Tarun joined Silicon Catalyst in 2015 as the first non-founder employee. Prior to that, he spent 22 years with Altera (now Intel PSG) where he led the packaging efforts for the organization. Tarun has Bachelors in Technology from Indian Institute of Technology, Kanpur, India and and MS in Materials Science from the University of California at Berkeley.



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David Z. Pan

Professor, Silicon Labs Endowed Chair, The University of Texas at Austin

Presentation Title:

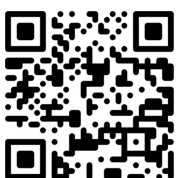
Emerging Trends in AI for Chip Design and EDA

Abstract:

AI for chip design and EDA has received tremendous interests from both academia and industry in recent years. It touches everything that chip designers care about, from power, performance, area (PPA) to manufacturability, reliability, and so on. It is everywhere, in all levels of design abstractions, for digital/analog/RF IC designs, verifications, as well as design for manufacturing (DFM). This talk will cover some recent trends in AI for chip design and EDA.

Speaker Biography:

David Z. Pan is Professor and holder of the Silicon Labs Endowed Chair at the Department of Electrical and Computer Engineering, The University of Texas at Austin. His research spans design automation for digital, analog, mixed-signal, RF and photonic ICs; synergistic AI/IC co-optimization; and cross-layer design, technology, and system co-optimizations. He has published over 540 refereed papers and holds 10 US patents. Prof. Pan has played key leadership roles in the community, e.g., serving DAC 2026 Vice Chair, DAC 2024 TPC Chair, and ICCAD 2019 General Chair. He has received many awards, including SRC Technical Excellence Award, over 20 Best Paper Awards from premier EDA/chips/AI venues, DAC Top 10 Author Award in Fifth Decade, among others. He has graduated 55 PhD students and postdocs, many of whom now hold key positions in academia and industry. He is a Fellow of ACM, IEEE, and SPIE.



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Frank Thiel

CTO, Gigantor Technologies

Presentation Title:

Ultra-fast AI Inference at the Edge

Abstract:

The age of edge AI inferencing is becoming a commercial reality. Using calibrated and trained models in optimized hardware can shift the inferencing workload from the datacenter to the edge, allowing near real-time object tracking and image recognition in portable devices, robots, drones, and more. By optimizing a deterministic hardware pipeline solution, lower latency and lower power can make the difference in the ability to detect an obstacle or a threat in time to take the appropriate action or to identify defective product moving through an assembly line.

Speaker Biography:

Frank is the CTO of Gigantor Technologies. He is an articulate and inspiring technical and business leader with over 40 years of innovating new products, technologies, and growing successful product lines in the semiconductor industry. Through his company, Kolvenier Solutions, he has helped multiple startup companies with their strategy and technology. He is also a long-time advisor for Silicon Catalyst. As a corporate executive, Frank ran profitable businesses and R&D teams for Microsemi, Zarlink, AMD and more. Starting his career as a circuit designer for Texas Instruments, he is still an engineer at heart. He holds 18 patents and is a published author.



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Rick Seger

Founder & SVP Corporate Development, SigmaSense

Presentation Title:

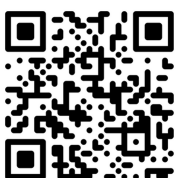
New sensing technologies providing insight inside batteries

Abstract:

This presentation will discuss a new technology development which, based on Electrochemical Impedance Spectroscopy can get more insight into the health and risks of batteries.

Speaker Biography:

Rick is a seasoned semiconductor executive with over 30 years of experience driving innovation in sensing technologies and IoT products at N-trig, Motorola, and Intel creating billions in value.



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Gilberto Migliorin

SOC Engineering, Principal Engineer, Synopsys

Vivek Raheja

Harsh Vardhan Gupta

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Presentation Title:

Bridging the Gap: A Practical Roadmap to Formal Verification for DV Engineers

Abstract:

Formal Verification (FV) has emerged as a powerful complement to dynamic simulation-based verification, offering exhaustive and mathematically rigorous analysis of digital designs. Despite its proven benefits, many Design Verification (DV) engineers face challenges in adopting FV due to a lack of clarity on where to begin and how to progress effectively. This paper presents a structured methodology — The Formal Pathway — designed to guide DV engineers through a practical and progressive adoption of Formal Verification.

The methodology is divided into three key stages: 1. Focuses on low-effort, high-impact applications such as Unreachability (UNR), Connectivity, Assertion IPs (AIP) apps, Linting, and Low Power checks. 2. Introduces more advanced use cases including Control and Status Register (CSR) verification, Clock and Reset Domain Crossing (CDC/RDC) analysis, and Security and Safety properties. 3. Addresses complex design scenarios, emphasizing Formal Property Verification (FPV), Sequential Equivalence Checking, and Datapath verification. Recent advancements in EDA tools are further easing the adoption of FPV. AI-powered features such as automatic generation of assertions based on design specifications are helping DV engineers overcome the initial barriers to formal property authoring. These innovations are making FPV more accessible and reducing the learning curve, enabling teams to integrate formal techniques earlier and more effectively. In parallel, the paper discusses strategies to manage and mitigate complexity, enabling scalable formal deployment across diverse design environments. By offering a clear roadmap and actionable insights, this paper aims to empower DV engineers to confidently integrate Formal Verification (using VC Formal) into their workflows, ultimately enhancing design quality and verification efficiency.



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Speaker Biography:

Gilberto Migliorin is a Principal SOC/Subsystem Verification Engineer at Synopsys Inc., currently working within the Systems Solutions Group. With over two decades of experience in digital design verification, Gilberto has contributed to successful projects in the automotive domain and across a range of general-purpose microcontroller platforms. Throughout his career, he has taken initiative in both leading verification programs and independently owning critical technical areas, spanning SOC-level and subsystem-level verification, embedded software, and post-silicon validation. His expertise includes ARM and Tensilica architectures, and he has collaborated with global teams across multiple engineering disciplines. Gilberto holds a Master's degree in Computer Science from Universidade Federal do Amazonas, with a focus on Digital Video Processing, and a Bachelor's degree in Electrical Engineering from Universidade Federal do Rio Grande do Sul. He is recognized for his technical depth, cross-functional collaboration, and contributions to verification methodology improvements.



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Jeffrey Pan

Co-Founder & CTO, Bronco AI, Inc.

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Presentation Title:

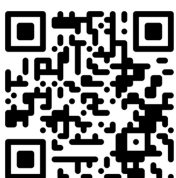
AI Agents for DV Debug

Abstract:

Debug consumes 40-60% of verification time and represents the critical path to tape-out in modern chip development. AI agents, powered by generative AI and integrated with AI-native EDA tools, can transform debug productivity by autonomously analyzing complex waveforms, identifying root causes, and iterating on solutions. Unlike traditional approaches requiring extensive customization, generative AI generalizes across diverse design environments, enabling rapid deployment and consistent performance without project-specific fine-tuning.

Speaker Biography:

Jeffrey Pan is the cofounder and CTO of Bronco AI, with extensive experience advancing AI applications. At age 15, Jeffrey was the youngest-ever author at CVPR (the highest-impact ML conference). He then won the MIT-IBM Best Paper Award at KDD's AdvML (Adversarial ML) Workshop, and his real-time edge model won First Place in an international competition focusing on efficient ML and hardware-software co-design. He was then a founding member of an AI research team that deployed generative AI models to hundreds of millions of monthly active users before cofounding Bronco to bring AI to semiconductors and other fundamental industries.



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Sheela Pillai

Independent Consultant

Presentation Title:

Improving Verification to Accelerate Shift-Left

Abstract:

Verification is no longer just a technical challenge—it is a leadership challenge in achieving predictability, quality, and accelerated convergence. As SoCs and AI workloads grow in complexity, shift-left methodologies are essential to bring verification into the earliest phases of design. In this session, Sheela Pillai, will share her leadership perspective and philosophy on how verification can be accelerated, made more predictable, and drive early design convergence. Drawing on over 25 years of experience at AMD, Intel, Qualcomm, Microsoft, and Renesas, she will discuss how shift-left practices—such as integrating physical design and scan insertion earlier—enable multifaceted closure and improved silicon quality. Attendees will gain both technical strategies and leadership insights into making verification not only a technical enabler but also a driver of innovation and organizational success.

Speaker Biography:

Sheela Pillai is a senior semiconductor industry leader with more than 25 years of experience in the semiconductor industry. Sheela has a proven record of delivering breakthrough products, scaling global engineering organizations, and driving transformation across design and verification. Throughout her career, Sheela has guided complex SoC programs from concept through delivery, spanning compute, automotive, and communications markets. She is recognized for her ability to align strategy with execution, transforming engineering teams to achieve efficiency, first-pass silicon success, and accelerated time-to-market. Sheela combines deep technical knowledge in SoC design and verification strategy with a leadership style rooted in clarity, empathy, and empowerment. Most recently Sheela was Senior Director of Engineering at Renesas, in the High Performance Computing group leading automotive SOC design and development. Prior to Renesas, Sheela held senior leadership roles at Intel, Qualcomm, Microsoft, AMD, and Altera. At Qualcomm, she led post-silicon validation and customer enablement for the company's first flagship ARM-based server SoCs in 10nm and 7nm.



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At Intel, she served as Senior Director of Engineering in the Intel Foundry Services group, leading IP development and automotive SoC methodology, and earlier contributed to industry-defining initiatives such as InfiniBand and PCI Express. At AMD, Sheela played a pivotal role in transforming the company's design methodology, leading the adoption of SoC/IP-based development approaches that enabled multiple parallel product launches and accelerated time-to-market. Known as a change agent and organizational "fixer," Sheela has been repeatedly called upon by senior leadership to transform underperforming teams and deliver on critical programs. Passionate about mentorship, she is dedicated to building high-performance teams, nurturing technical leaders, and shaping the future of semiconductor innovation.



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Shelly Henry

CEO / Co-Founder, Moores Lab AI

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Presentation Title:

The Intelligent Verification: Reinventing 5 DV Workflows with AI

Abstract:

The Intelligent Verification: Reinventing 5 DV Workflows with AI showcases how AI transforms chip verification from spec to debug. By automating testplan creation, UVM generation, testcases, assertions, and debug, AI accelerates workflows, improves coverage, and enhances traceability— enabling faster, smarter, and more efficient silicon verification.

Speaker Biography:

Shelly Henry is the CEO and Co-Founder of Moores Lab AI, with over 25 years of semiconductor industry experience. Prior to founding Moores Lab AI, Shelly led silicon teams at Microsoft and ARM, successfully delivering chips that power billions of devices worldwide. Passionate about driving efficiency and innovation, Shelly and his team at Moores Lab AI are transforming chip development through specialized AI-driven automation solutions.



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Georg Meinhardt

Founding Engineer, DiffLogic Inc.

Presentation Title:

Rethinking AI Inference and Hardware Verification through Differentiable Logic Gate Networks

Abstract:

Efficient AI inference is critical for edge computing and real-time systems. However, current hardware inference solutions such as binarized neural networks or quantization-based methods still rely heavily on resource-intensive operations like matrix multiplications and frequent memory access, limiting their latency, throughput, and power efficiency. In this presentation, we provide an introduction to differentiable logic gate networks (difflogic), a new neural network (AI) architecture designed specifically to address these limitations while enabling formal and functional verification directly at the logic-gate level. Logic gate networks are neural network architectures using only fundamental digital circuit elements such as AND, OR, and XOR gates—completely eliminating matrix multiplications, integer arithmetic, and RAM-based weight storage. Previously, logic gate-based models required combinatorial optimization techniques for training, which limited their scalability and practical deployment. By employing

differentiable relaxation techniques, logic gate networks can now be trained effectively using standard gradient descent methods. Using differentiable relaxations and end-to-end gradient-based learning leads to advances in both inference and verification efficiency:

- Dramatically reduced inference latency, achieving full-model inference latencies as low as 1.3–40 ns.
- Ultra-high throughput inference, enabling up to 770M inferences/s through pipelined logic gate implementations.
- Reducing power consumption by up to 98%
- Automatic functional verification built into the training process (Results from published ASIC-emulation on FPGA; compared against existing solutions such as AMD Xilinx FINN)

Attendees will gain insights into the core principles behind difflogic, practical techniques for training and optimizing logic gate networks, and performance comparisons against traditional neural networks and other inference methods

Speaker Biography:

Georg Meinhardt is Founding Engineer at DiffLogic Inc, the team behind commercializing differentiable logic gate networks in the financial industry. A mathematician (Oxford) turned hardware-AI specialist, he bridges algorithm design and chip implementation, pushing sub-10ns neural inference on FPGAs.



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Santosh Appachu Devanira Poovaiah

Senior CPU Verification Engineer , NVIDIA Corporation

Presentation Title:

Applying Generative AI in Post-Silicon Validation: Real Use Cases and Technical Insights

Abstract:

Post-silicon validation is one of the most demanding phases in the silicon lifecycle, where real hardware is stressed to uncover bugs that escaped pre-silicon verification. Despite extensive simulation, emulation, and formal verification, subtle issues especially those involving cache coherency, memory ordering, or multi-core synchronization often manifest only on silicon. Traditional approaches rely on constrained-random instruction generators, directed assembly tests, and workload-based stress tools, but these methods have limitations in scalability and in covering rare interleaving's.

Generative AI (GenAI), powered by large language models and domain-tuned generative frameworks, introduces a new paradigm. In post-silicon, GenAI can be used to automatically synthesize coherency stimulus programs, generate assembly/microcode sequences for stressing MESI/MOESI state transitions, or mutate existing directed tests to explore unanticipated access patterns. For example, a GenAI model can take a high-level directive such as "generate a four-core workload with simultaneous atomic operations to shared cache lines" and produce runnable test code that stresses invalidation, downgrade, and writeback races across cores.

Beyond stimulus generation, GenAI can assist in failure triage by summarizing long counterexample traces, correlating performance counter anomalies with expected states, and suggesting candidate root causes. These capabilities reduce debug turnaround time and allow engineers to focus on hypothesis validation rather than manual log sifting. Early experiments show that AI-generated stimulus can complement traditional random generators by increasing test diversity and reaching otherwise difficult-to-hit corner cases.



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This session will present real examples of GenAI applied in post-silicon validation of complex SoCs, highlighting both the measurable benefits (coverage, debug efficiency, reduced engineering effort) and the guardrails required to ensure correctness. Attendees will gain a deeper understanding of how GenAI augments, rather than replaces, existing validation flows, and how it can be systematically integrated into mission-critical post-silicon environments.

Speaker Biography:

Santosh is an experienced engineer with over seven years in SoC design and verification, currently specializing in full-chip coherency verification for advanced, high-performance computing systems. At NVIDIA, Santosh plays a key role in validating flagship architectures such as Grace Hopper and Blackwell GPUs—core components of DGX-class platforms deployed across AI, data center, automotive, and HPC domains.

With a proven track record in verifying silicon optimized for AI acceleration, Santosh works closely with cutting-edge designs that challenge the limits of compute, memory, and interconnect complexity. Santosh holds a Master's degree in Computer Engineering from the University of Southern California. Prior to joining NVIDIA, Santosh developed firmware with a focus on security at Robert Bosch, gaining valuable experience at the intersection of low-level software and hardware security.

Santosh is deeply knowledgeable in modern computer architecture, with expertise in cache coherence protocols, multi-agent interconnect systems, and memory consistency models. Their work centers on verifying complex heterogeneous SoC architectures, including CPU-GPU interactions under parallel, high-throughput workloads. Passionate about building robust, scalable, and high-efficiency hardware for next-generation AI training and inference systems, Santosh is driven by the challenge of ensuring correctness and security in large, tightly integrated computing platforms.



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Arjumand Yaqoob

Staff Engineer , Qualcomm Incorporated

Presentation Title:

Deploying AI in DV for Smarter and Faster IP Verification

Abstract:

AI is set to play a key role in optimizing the traditional design verification flows and challenges. Providing a faster and smarter platform to deploy and use in design verification while verifying designs of different complexities. We will be presenting a case study based on our AI strategy model which can be deployed on a DUV (design under verification) to achieve the desired results.

Speaker Biography:

Arjumand Yaqoob is semiconductor professional with around 15 years of experience, currently working as Staff Engineer in Qualcomm Incorporated in it's HQ at San Diego CA. In this role he is working on Complex design verification tasks and projects contributing to the cutting-edge technology developed and delivered by Qualcomm. He has worked across different business units and teams for last decade while working in Qualcomm and contributed to many critical tasks including process improvements, verification strategies and planning and developed complex verification architectures and Test Benches. He has been part of methodology development teams and helped in automating and flows development for verification reviews and signoff processes. In addition to technical tasks, Arjumand has worked actively in different technical committees in Qualcomm and helped in organizing technical talks and seminars.



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Doug Smith

Engineer / Instructor, Doulos

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Presentation Title:

Practical Asynchronous SystemVerilog Assertions

Abstract:

Nearly all digital designs have asynchronous behaviors or may be inherently asynchronous by design. Likewise, asynchronous behaviors appear in the form of asynchronous handshaking protocols for peripheral devices or in the case of synchronizers between clock domain crossings. SystemVerilog assertions (SVA) provide a great way of testing and describing design behaviors. However, using SVA to capture asynchronous behavior is not always straightforward due to the scheduling semantics of SystemVerilog. While triggering on an asynchronous event is easy enough, the sampling of the assertion inputs is either dependent on its context or synchronous by nature. Often, asynchronous events occur before the design has updated its state, requiring the checking of the RTL to be delayed. Furthermore, the timing of asynchronous events may be hard to predict, making it harder to describe using an assertion. This session will cover eight common asynchronous scenarios and the SVA solutions for checking them.

Speaker Biography:

Doug Smith is a verification engineer and instructor for Doulos based in the Austin Texas area with expertise in SystemVerilog, UVM, and formal verification. At Doulos, he delivers training in verification methodologies, hardware description languages, and formal technology.

Doug holds a masters degree in Computer Engineering from the University of Cincinnati and a bachelors degree in Physics and Biology from Northern Kentucky University. Currently, he resides in Paige Texas with his wife and family on a small farm where he raises bees, horses, chickens, and pigs and loves playing around on his tractor.



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Daniel Cross

Sr Principal Solutions Engineer, Cadence Design Systems

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Presentation Title:

Overcoming Obstacles to Model-based Verification

Abstract:

There are many obstacles that prevent design teams from effectively adopting a model-based verification methodology. Many of these are not obvious before adoption of a methodology. The purpose of this presentation is to make the audience aware of the potential roadblocks to successful model-based verification, provide some guidance about overcoming the issues, and to highlight some of the benefits of overcoming the obstacles to successfully implement a model-based verification flow.

Speaker Biography:

Daniel Cross holds MSECE and BSEE degrees from the University of Miami. He has been applying behavioral modeling and mixed signal simulation to verification problems for over 15 years, achieving first pass success with RF ASICs and SOCs. He joined Cadence in 2019 and has championed the adoption of Real Modeling and advanced verification methodologies to mixed signal designs. He is a Senior Member of the IEEE and participates in several IEEE standards working groups.



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Abhijit Madhu Kumar

Principal Solutions Engineer, Cadence Design Systems

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On behalf of Paul Denny

Presentation Title:

Modelling a 4-Level DCDC Converter Using EEnets

Abstract:

There are many challenges associated with verifying analog circuits where high accuracy and high performance are required from the simulator. This talk presents a case for Digital Mixed-Signal (DMS) modelling, specifically EEnet models, as a tool to achieve these goals. The presentation also discusses advantages and challenges associated with this kind of verification.

Speaker Biography:

Abhijit graduated from Georgia Tech in 2014 with an MS in Electrical Engineering. He joined Cadence in 2015 and works as a Solutions Engineer providing mixed signal verification solutions to several Cadence accounts wanting to adopt advanced methodologies. Abhijit's work focuses on analog and real-number modelling, and the introduction of Metric-Driven Verification and UVM concepts to the verification of mixed signal systems.



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Umar Lyles

Mixed Signal Modelling & Verification Manager, Cirrus Logic

Presentation Title:

Practical Approaches to Adopting State of the Art Mixed Signal Solutions

Abstract:

Over reliance on AMS driven verification for Increasingly complex mixed signal product needs has become increasingly inadequate leading to declining product quality and/or inability to develop state of the art products. System-Verilog spice emulation modeling is emerging and has been shown as a good solution to address these issues. Despite industry awareness of emerging technology, widespread adoption is lagging. The goal of this talk is to highlight some key lessons learned, obstacles, and solutions that have enabled Cirrus Logic to be an industry leader in this area of expertise.

Speaker Biography:

Umar Lyles is an Industry leading expert in the field of analog design, mixed-signal modelling, design integration, and tops down methodology. He has 8 patents and published 2x in ISCC. He currently leads a team that is recognized for developing some of the most advanced mixed signal modelling approaches in industry.



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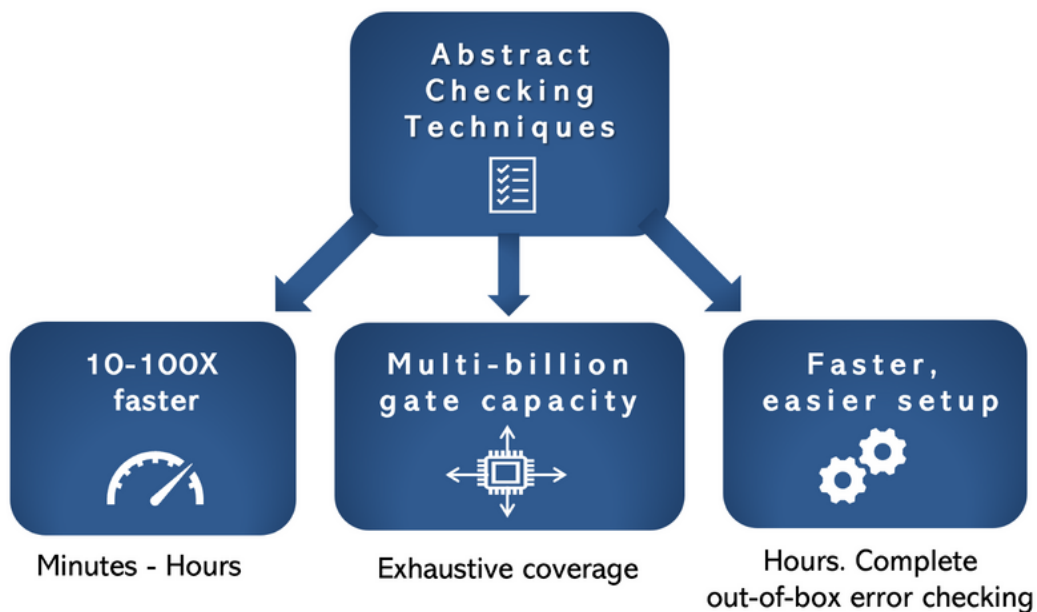
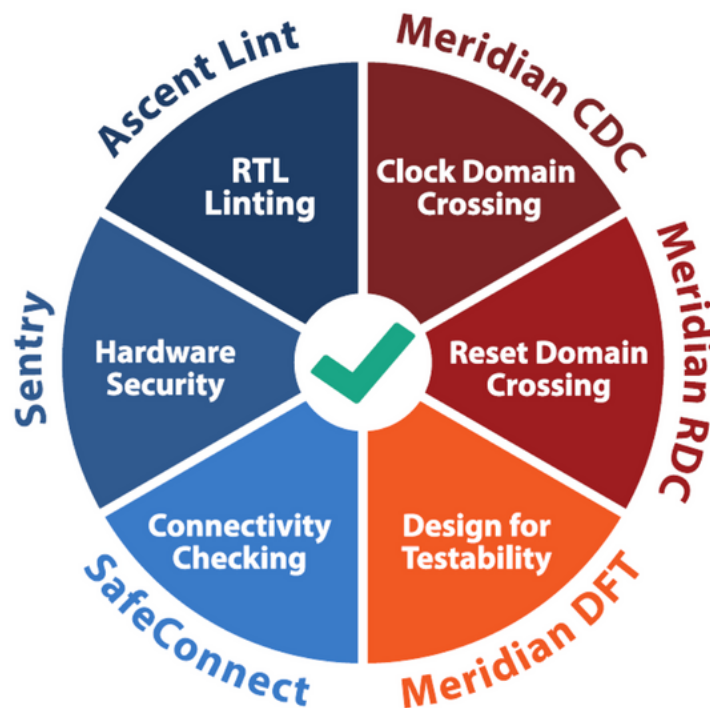
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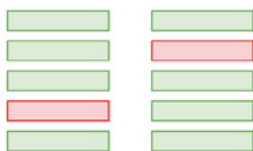
Self-Improving

AI-powered learning that transfers across tasks, bugs, and projects.

Spotlight: Bronco Agentic Debug

Inputs

Simulation Runs (Waves & Logs)



Project Context

- Paths to RTL, UVM, specs, docs etc.
- Input/Feedback

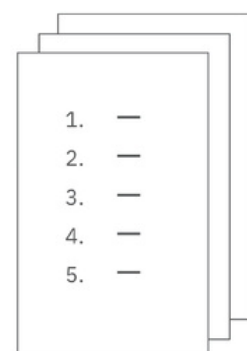
Bronco AI

Routine DV Work

1. Makes playbook for how to debug a given failure.
2. Extracts specifics from the project context.
3. Performs debug and remembers for next time.

Outputs

Root Causes & Tickets



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LUBIS EDA is a Germany-based startup empowering chip designers with cutting-edge Formal Verification services. Our mission is to ensure microchips are developed faster, more reliable, and entirely bug-free.



HERE TO TALK

Dr. Tobias Ludwig, 11.50 am,
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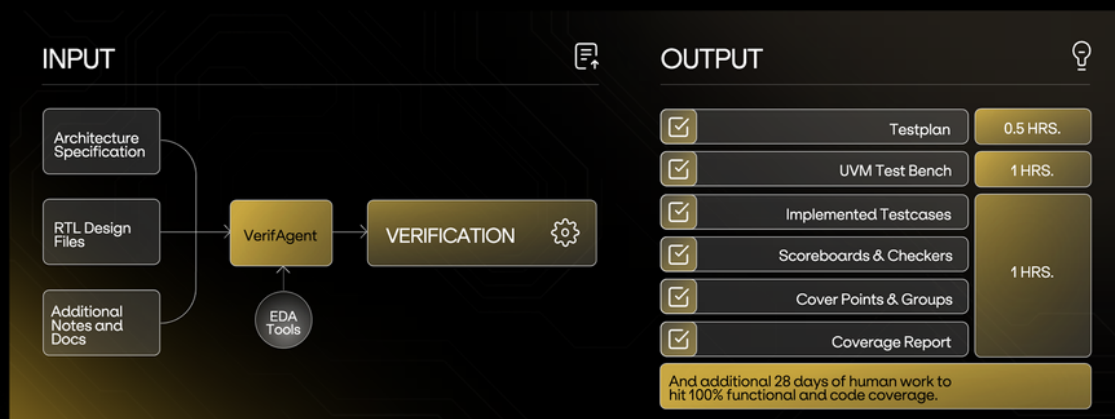


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CRITICAL BUGS FOUND 1	CRITICAL BUGS FOUND 3	CRITICAL BUGS FOUND 5

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Expertise

- IP Verification
- SOC Verification
- CPU/GPU Verification
- DFX Validation
- Low-power RTL and Netlist verification
- Gate Level Simulations

Scale

- ~400 Engineers across:
- IP
- SS/SOC
- GLS
- DFX

Methodologies

- SV-UVM; C/C++ ; Vmanager
- Formal Verification
- PSS – Portable Stimulus standards
- Adaptation of AI/ML methodologies

Low-speed peripherals

- SPI/QSPI
- I2C/I3C
- I2S
- UART
- CAN 1.0/2.0
- SPDIF

Memory interfaces

- SD Card 3.0
- ONFI 3.2
- LPDDR/DDR 3/4/5
- UFS
- NVMe

MIPI

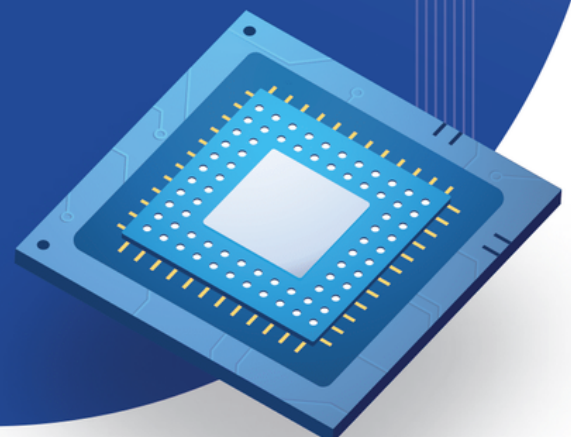
- RFFE
- DSI
- CSI
- D-PHY
- C-PHY

CPU Core & Infra

- ARM Cortex M*, A*
- RISC-V
- Tensilica

HSIO

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- PCIe GEN 3/4/5/6
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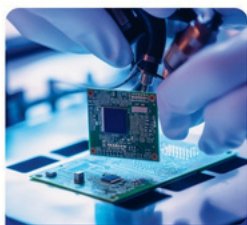
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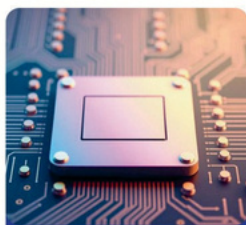
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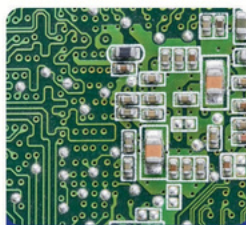
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