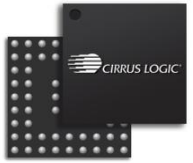
Practical Approaches to Adopting State of the Art Mixed Signal Solutions

Umar Lyles



Audio Experts in a Voice Connected World

Motivation – Recent Trends

- **ASIC Development Trends**
  - Re-spins
  - Cost
  - Behind Schedule Execution

- *"Alarmingly, first-silicon success rates have declined to their lowest level in two decades, with only 14 percent of projects achieving this milestone. To mitigate these challenges, the study highlights the growing adoption of advanced methodologies…"*

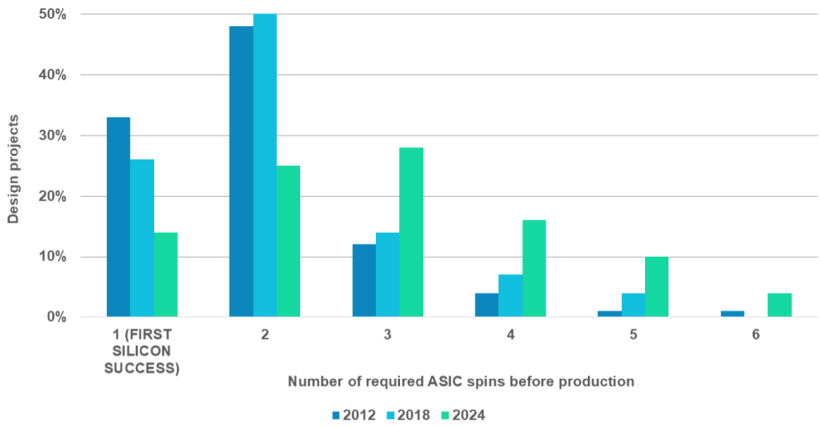


Figure 3. IC/ASIC spins required before production.

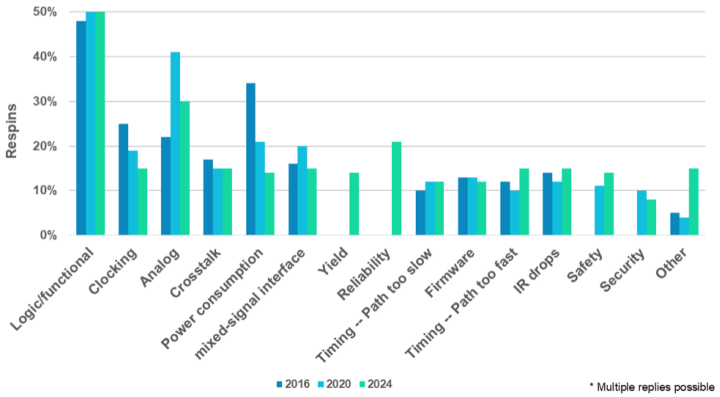


Figure 4. Types of flaws contributing to respins.

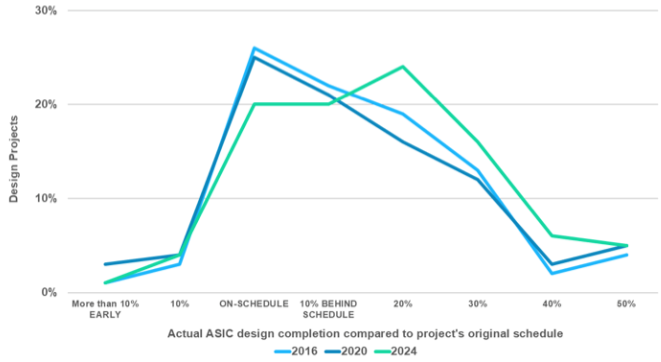


Figure 6. Percentage of IC/ASIC project time spent in verification.

H. Foster (2025), 2024 Wilson Research Group Functional Verification Study: IC/ASIC functional verification trend report (Siemens Digital Industry Software white paper).

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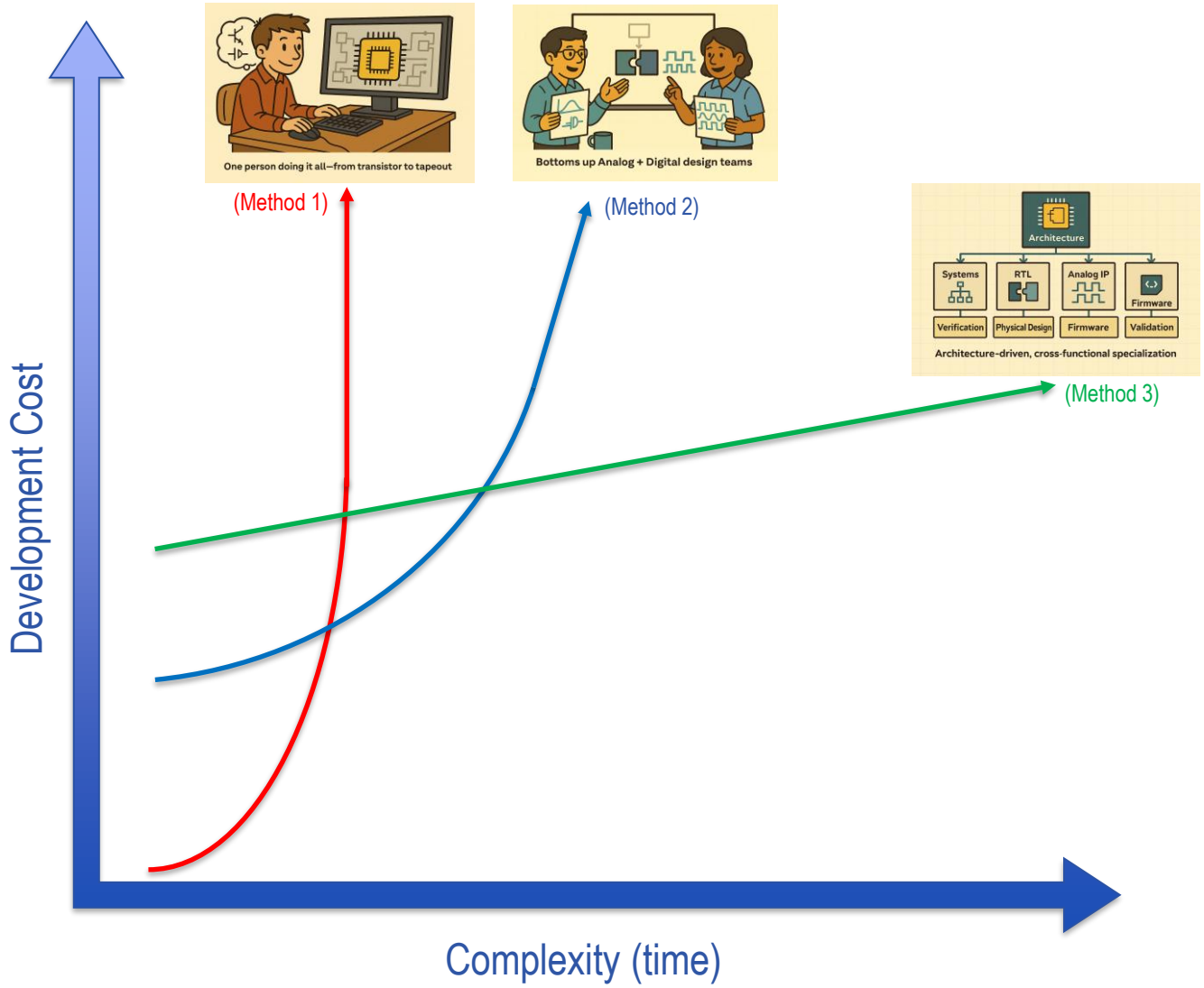
Motivation – Future Outlook



- **Advanced development techniques…**
  - Scalable vs complexity (time)
  - Dramatically reduces cost of lower complexity once mature
- **Cultural Pitfalls**
  - “Creatures of Habit” Reluctance to change results in need to experience significant pain before adapting
  - “Nostalgia Bias” Feeling that return to obsolete methods would be better (DANGER can cause re-adoption of costly methods)

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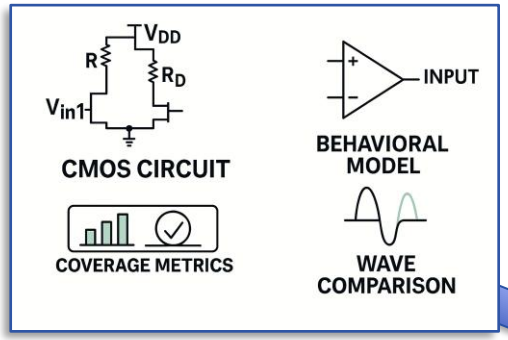
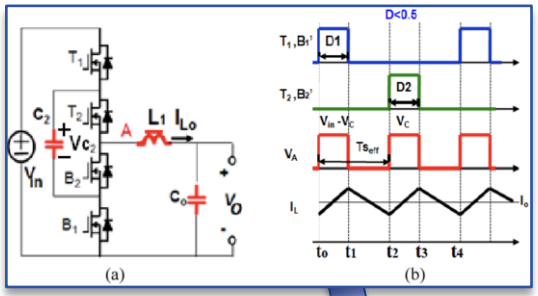
Goal – State of the Art Mixed Signal Validation & Verification

Coverage driven fully verified SV-RNM models & CMOS circuits

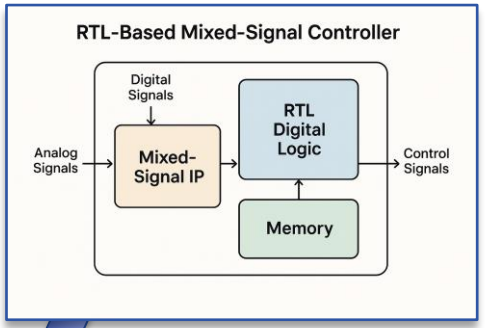


High throughput SV-UDT circuit solving

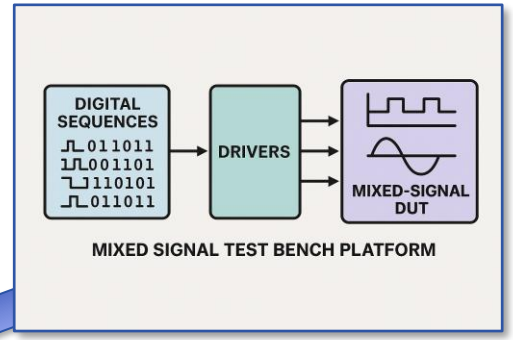
(>> spice sim performance)



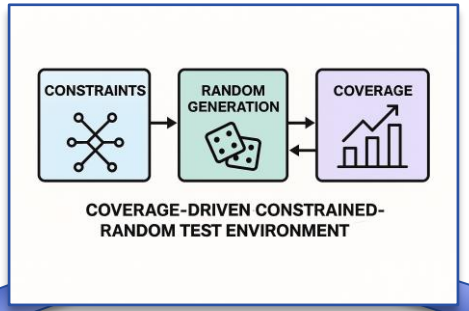
RTL



Universal DMS/AMS Test Bench



UVM Environment

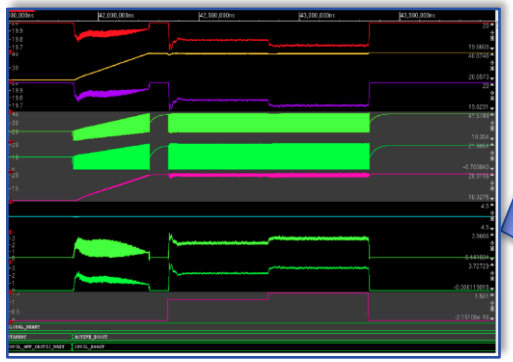


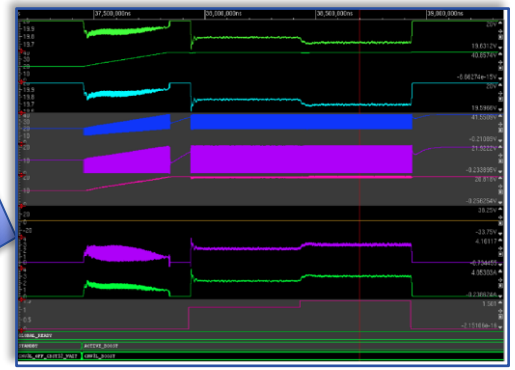
DMS

~20 min self checked sim

(10,000-500,000) scenarios

Functional circuit fidelity





AMS

~2 week wave reviewed sim

(1-100) scenarios

Functional circuit fidelity

Some parasitic fidelity

A contemporary SOC product can have state space > 100,000 scenarios

Reliance on traditional AMS verification approach is inadequate

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Defining the Mixed Signal Engineer

- **Deliverables**
  - SV models with complete features, fully verified, high fidelity, & high performance
  - Facilitate architectural exploration
  - Chip level and subsystem level AMS-UVM platform
  - IP development
  - Tool development
  - Chip integration
- **Attributes**
  - Strong analog design background
  - Strong control systems background
  - Expert in sv-RMM and sv-UDT modeling
  - Expert in AMS
  - Expert in MS debug - Go-to team members for understanding of how device works
  - Strong MS DV – test bench and test development expert

Adoption Challenges

- Mindset
- Staffing
- Technology
- Methodology

Adoption Challenges – Mindset

- **Belief that only spice is useful for block/subsystem architectural exploration and bug finding**
- **Belief that only AMS is useful for RTL+Analog simulation**
- **Many analog designers not proficient with mixed signal flows**
  - Digital on top test benches and test cases
  - Mixed signal debug tools tend to be digital design focused
  - Command line environments

Adoption Challenges – Staffing

- **Traditional Mixed Signal Organization**
  - No dedicated mixed signal team will try to leverage analog designers who typically lack expertise and time
  - Org with dedicated teams often view role as design service rather than design/systems/ms partnership
  - Ratio of mixed signal to analog design is usually inadequate
  - Analog design led = more bottoms up (circuits lead models) instead of tops down (models lead circuits)

Adoption Challenges – Technology

- **Tools**
  - Have not been optimized for analog solving means technical innovations are needed to bridge gaps in short term
  - Vendors solutions typically focus on global/general usage over highly custom solutions. General solutions may never be sufficient
- **Technology**
  - Issues requiring more consideration – performance, convergence, correctness
  - Repeated learning and refinement required during early years
  - Up front investment – IP libraries, automation, training, etc…

Adoption Challenges – Methodology

- Bottoms up (circuits lead models) vs. Tops down (models lead circuits)
- Reluctance for rigidity in analog to follow feature lock and pin lock plans
- X-func collaboration analog+digital+verification+systems+mixed signal

Traits of State of the Art Mixed Signal Validation & Verification

- **Product impact**
  - Enable reliable development of extremely complex SOC products
  - 0 Pre-silicon AMS bugs
  - 0 Post-silicon AMS ECOs
  - 0 Post-silicon Functional ECOs
  - A0 to market
- **Schedule impact**
  - Increased frequency of on-time execution
  - Improved ability to absorb scope changes with minimal schedule impact
- **Cost impact**
  - Reduced number of spins
  - Reduced likelihood of late-stage staffing surges

Conclusions

- **Creating a SOA MS Verification flow is practical but challenging**
- **Strategies needed to address common issues**
  - Mindset
  - Staffing
  - Technology
  - Methodology
- **Continuous focused efforts needed**
- **ROI is verry high**
  - Significantly improved quality
  - Ability to develop differentiated products
  - Significantly lower cost
    - Less spins
    - Reduced opportunity cost
    - Reduced time to market
  - Improved customer satisfaction


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