The Intelligent Verification: Reinventing 5 DV Workflows with AI

Transforming design verification through artificial intelligence

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The Five Pillars

AI-Powered Verification Workflows

1. Testplan Generation

Spec-to-Testplan Automation

2. UVM Testbench Creation

Automated UVM Scaffold

3. UVM Testcase Implementation

Testplan Items → Sequences

4. SVA & Functional Coverage

Assertion Mining & Covergroups Generation

5. Debug Automation

Waveform & Log Based Debug Intelligence

1. Testplan Generation

01

Spec-to-Testplan Automation

AI parses natural-language specifications to create structured, coverage-oriented testplans.

02

Bidirectional Traceability

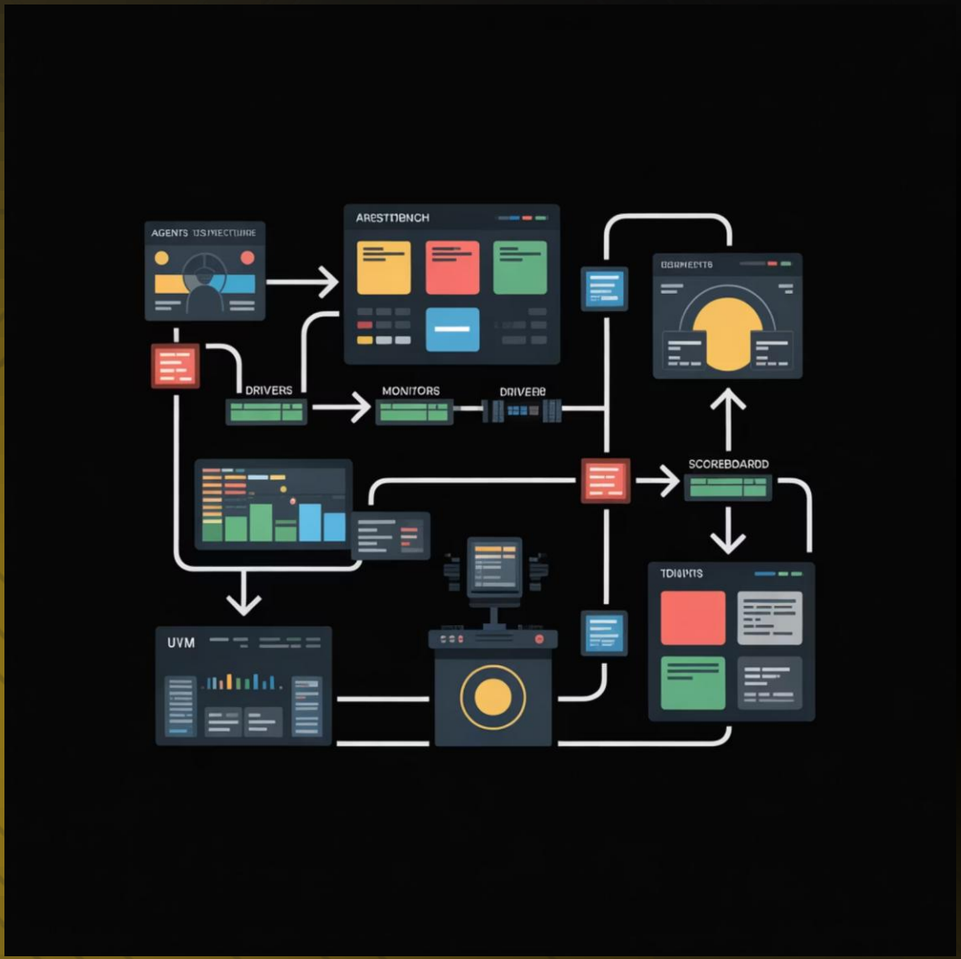
Each test item links directly to spec spec sections for audit and review by by designers and architects.

03

Dynamic Updates

Auto-sync testplans with evolving specs—incremental regeneration on on change detection.

2. UVM Testbench Creation



Automated UVM Scaffold

AI generates UVM agents, drivers, monitors, scoreboards, and connects them connects them per DUT interfaces.

VIP Reuse Optimization

Recommends internal or third-party VIPs based on past projects and protocol matching.

3. UVM Testcase Implementation

Testplan Items → Sequences

Converts scenario descriptions into runnable UVM sequences with constraints and coverage hooks.

Coverage-Driven Refinement

Reinforcement learning generates new stimuli for under-covered covered areas.

4. SVA & Functional Coverage

Intelligent property extraction and coverage optimization

Assertion Mining

Extracts design properties and proposes SystemVerilog Assertions via pattern recognition.

Coverage Groups & Bins

Generate covergroups and coverpoints based on the protocol and architecture specification

5. Debug Automation

Waveform & Log Intelligence

Clusters failures via signal correlation;
highlights root-cause candidates.

Anomaly & Log Summarization

AI summarizes regression logs,
flags behavioral outliers, and identifies failure trends.

Reinventing Design Verification

- Testplan
- UVM Test Bench
- UVM Testcases
- SVA & Cover Groups
- Debug Automation

Book a Demo!

Moores Lab AI

www.mooreslab.ai