Verification Futures Austin, Nov. 12, 2025

Emerging Trends in AI for Chip Design and EDA

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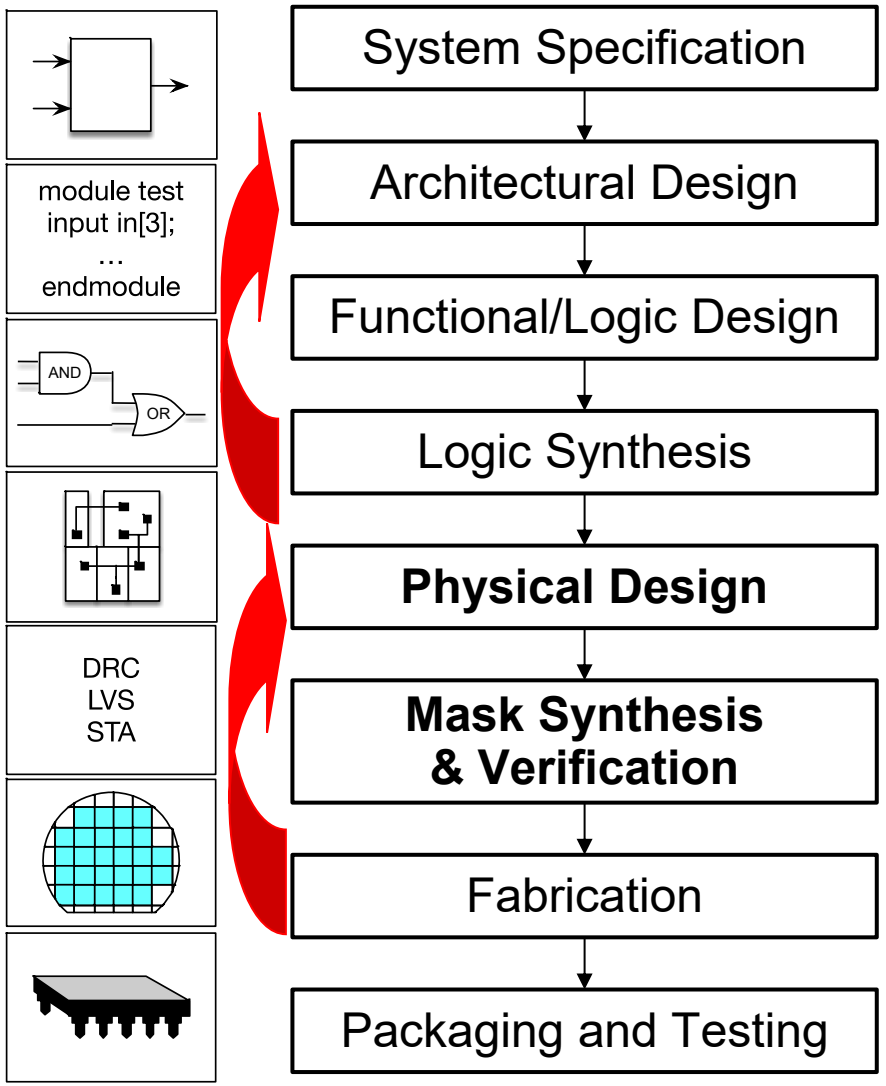
TEXAS
The University of Texas at Austin

Si SILICON CATALYST

AI for Chip Design and EDA



- AI can serve as hammers and bridges to improve design productivity and quality + GenAI
- **Everything:** power, performance, area (PPA), yield, cost, ...
- **Everywhere:** All levels of design abstractions, digital, analog, RF, verification, …
- **All at once?** not yet!

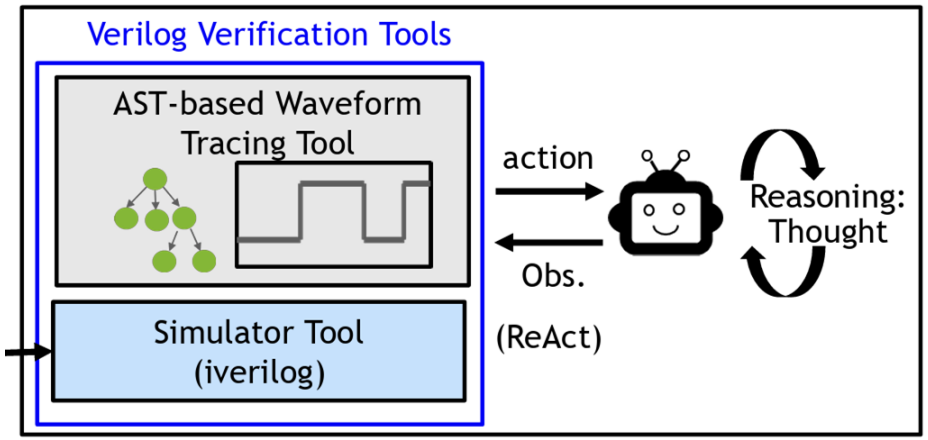
AI for RTL / Verilog Design

- AI for software coding is widely successful
- Many papers on RTL generation, e.g. ➔
  - However, they still cannot guarantee correctness
  - Not to mention high-quality PPA
- Hardware consists of inter-dependent concurrent modules
  - In contrast, software is native to LLM because it executes in a sequential order

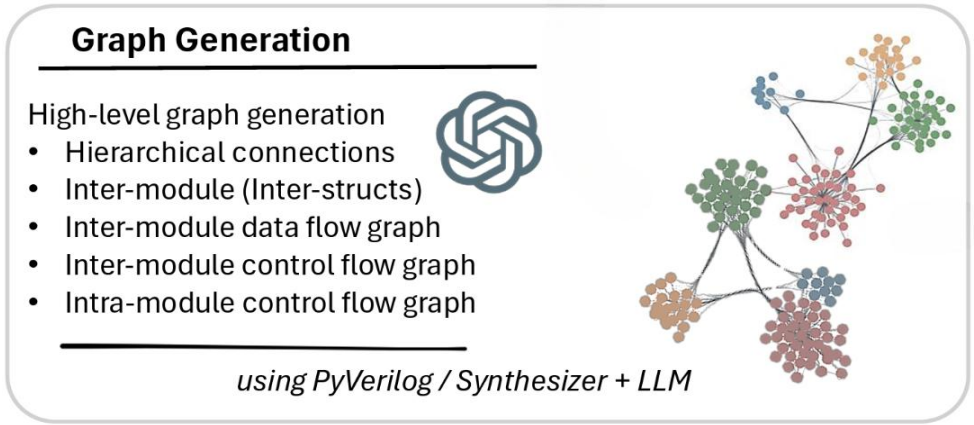
Name	Techniques
MAGE	Agentic, Debug
VerilogCoder	Agentic, Debug
Aivril	Agentic
RTLFixer	Agentic, RAG
AutoVCoder	Finetune, RAG
VeriReason	Finetune, RL
VeriGen	Finetune
Autochip	Agentic
BetterV	Finetune, Opt
RTLCoder	Finetune, RL
VeriAssist	Agentic, Opt
ChipNeMo	Finetune
Paradigm-based	Agentic
C2HLSC	Spec2HLS, RAG
HLSPilot	Spec2HLS, RAG
LHS	Spec2HLS, RAG, Opt
VeriOpt	Agentic, RAG, Opt
Autosilicon	Agentic, RAG, Debug

RTL Generation with Formal Guidance

- VerilogCoder (Nvidia Research)
- Use Abstract Syntax Tree (AST) to identify errors related to specific signals



- RTL++ (Univ. Central Florida)
- Use Control Data Flow Graph (CDFG) to analyze control logic and signal dependency

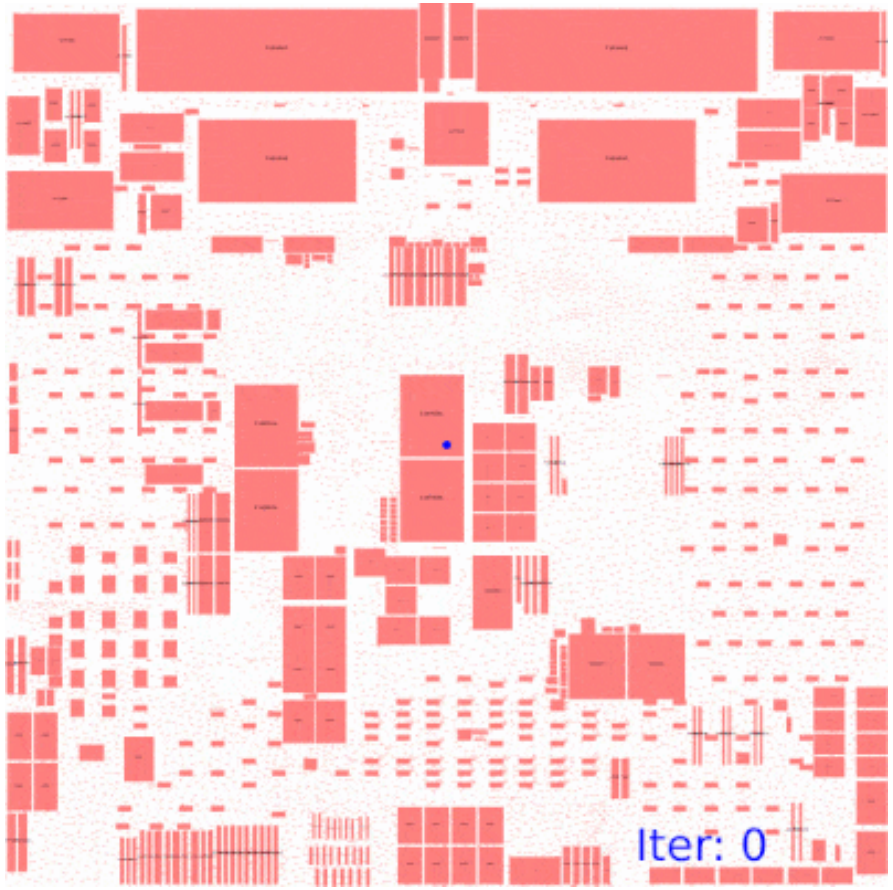


However, verification is always difficult after completion.

Our ongoing work focuses on stepwise verification during the design process.

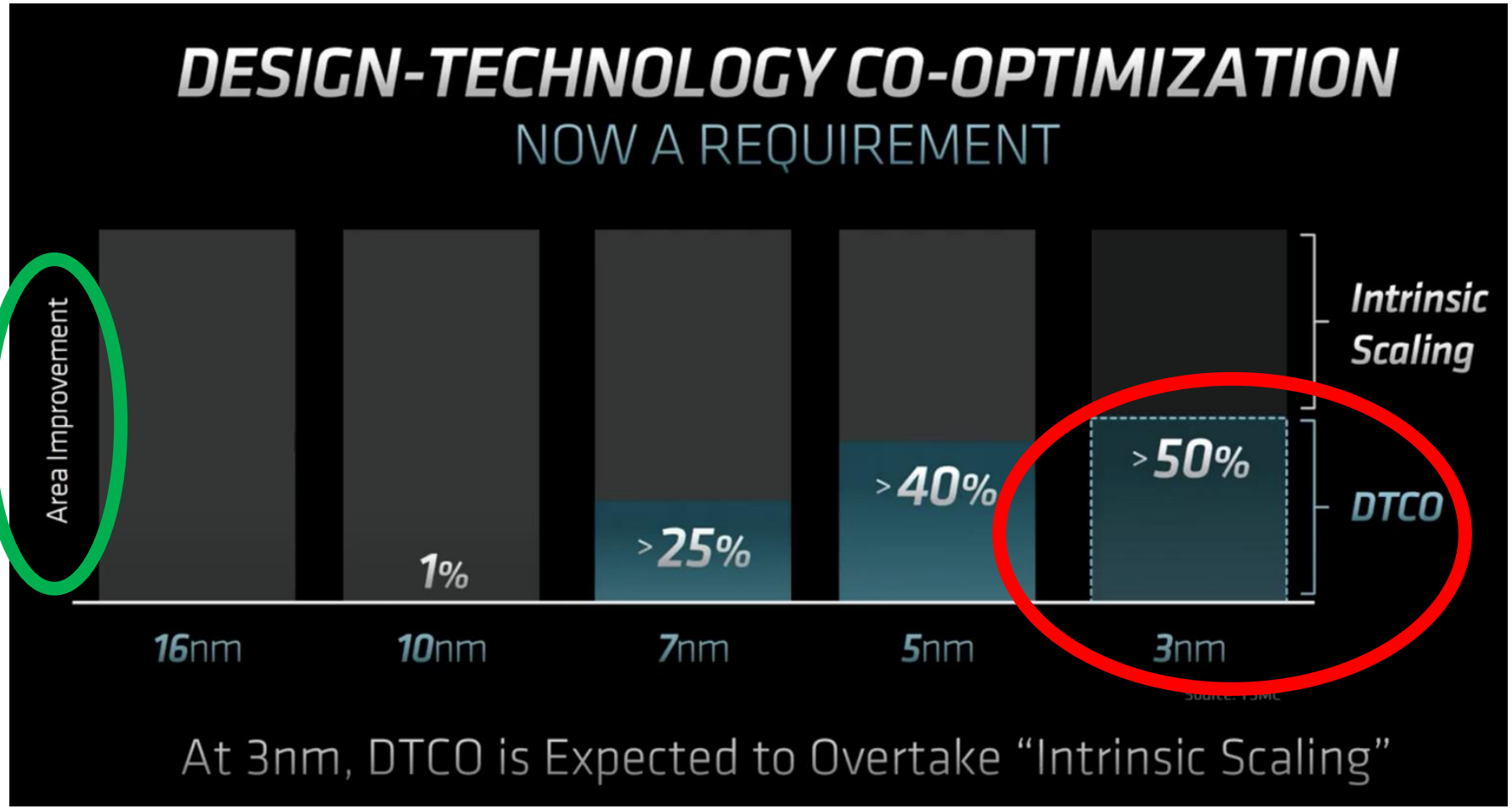
VLSI Placement and SSTA: Differentiable

- Plays a **central** role in modern chip design closure for PPA
- Our DREAMPlace [DAC'19 BPA and TCAD'21 BPA] pioneered deep-learning inspired GPU acceleration (888 Github stars as 11/11/2025)
- INSTA [DAC'26 BPA] from Nvidia: differentiable SSTA and timing driven global placer

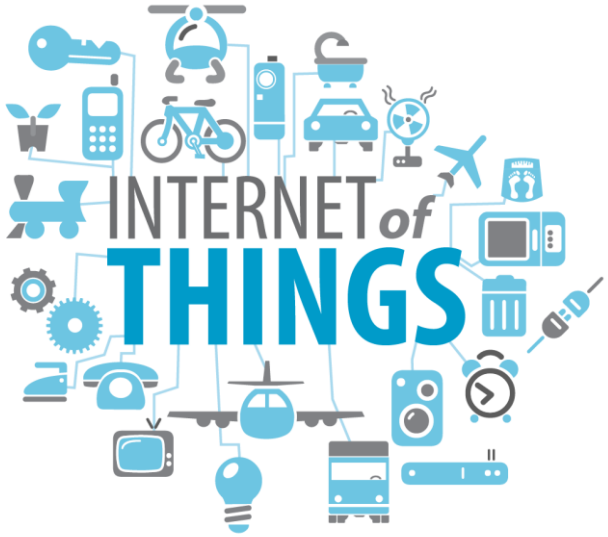


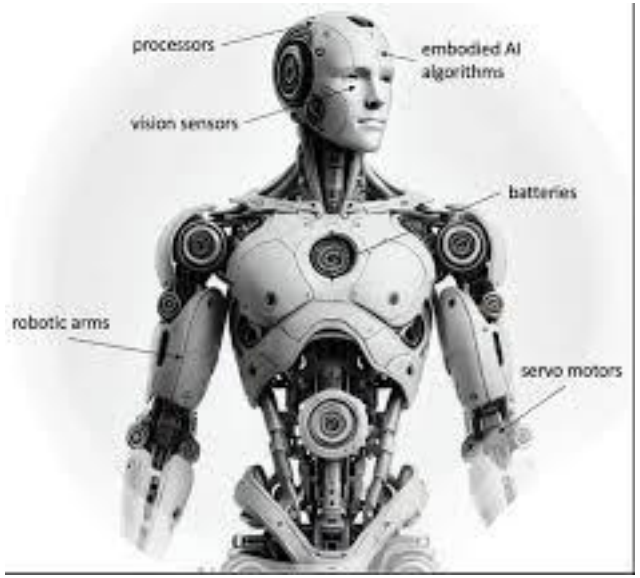
Push for Extreme DTCO (and STCO)

- Mark Papermaster (AMD CTO) DAC 2022 Keynote



Growing Analog/RF IC Demand





Even Compute Systems are Analog Enabled!

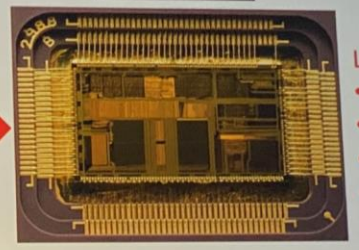
Compute Systems are Analog-Enabled Digital

View of some digital designers

Some annoying ANALOG stuff that we probably don't need

Compute (DIGITAL)

i486 1989



Limited to:
- 100MHz clock
- 1Gb/s I/O
- No DVFS
- Limited security

Without **integrated analog**, our processor capability would **resemble i486**

IEEE MTT-S SSCS SOLID-STATE CIRCUITS SOCIETY RFIC SPONSORS: qorvo GlobalFoundries

RFIC 2024 Plenary

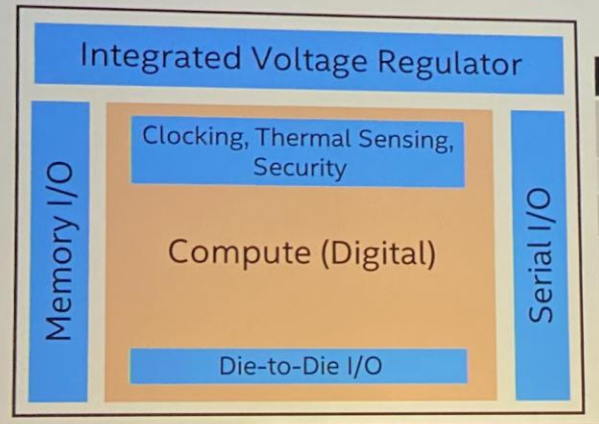
Analog Evolution in Digital CMOS-Centric Technologies

Tsu-Jae King Liu

Department of Electrical Engineering and Computer Sciences

Compute Systems are Analog-Enabled Digital

Analog and Mixed-Signal (AMS) Circuits are ubiquitous



Integrated AMS Systems	Enables
Digital Thermal Sensor (DTS) and Power Management Unit	Monitors optimum core performance. Prevents thermal runaway
Phase-Locked Loop (PLL)	High-frequency clocking
Integrated Voltage Regulator	Energy-efficient power delivery
Wireline Transceivers (I/O)	Communication to outside die
Data Converters (ADC/DAC)	Interface between real-world signals and digital compute
Wireless Communication	Dense integration of radios (WiFi, Bluetooth...)
ESD	Protection against triboelectric discharge

Innovations in integrated analog functions have **enabled compute performance scaling**

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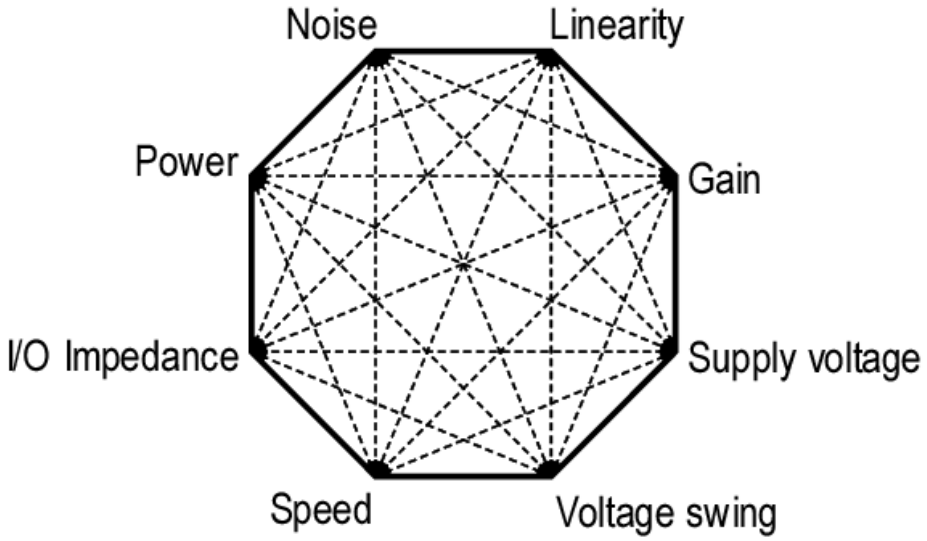
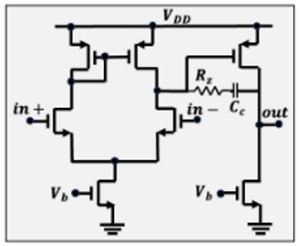
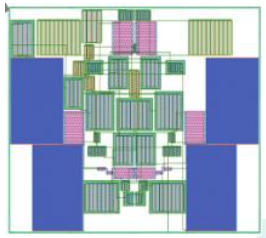
Analog / RF IC Designs are Hard

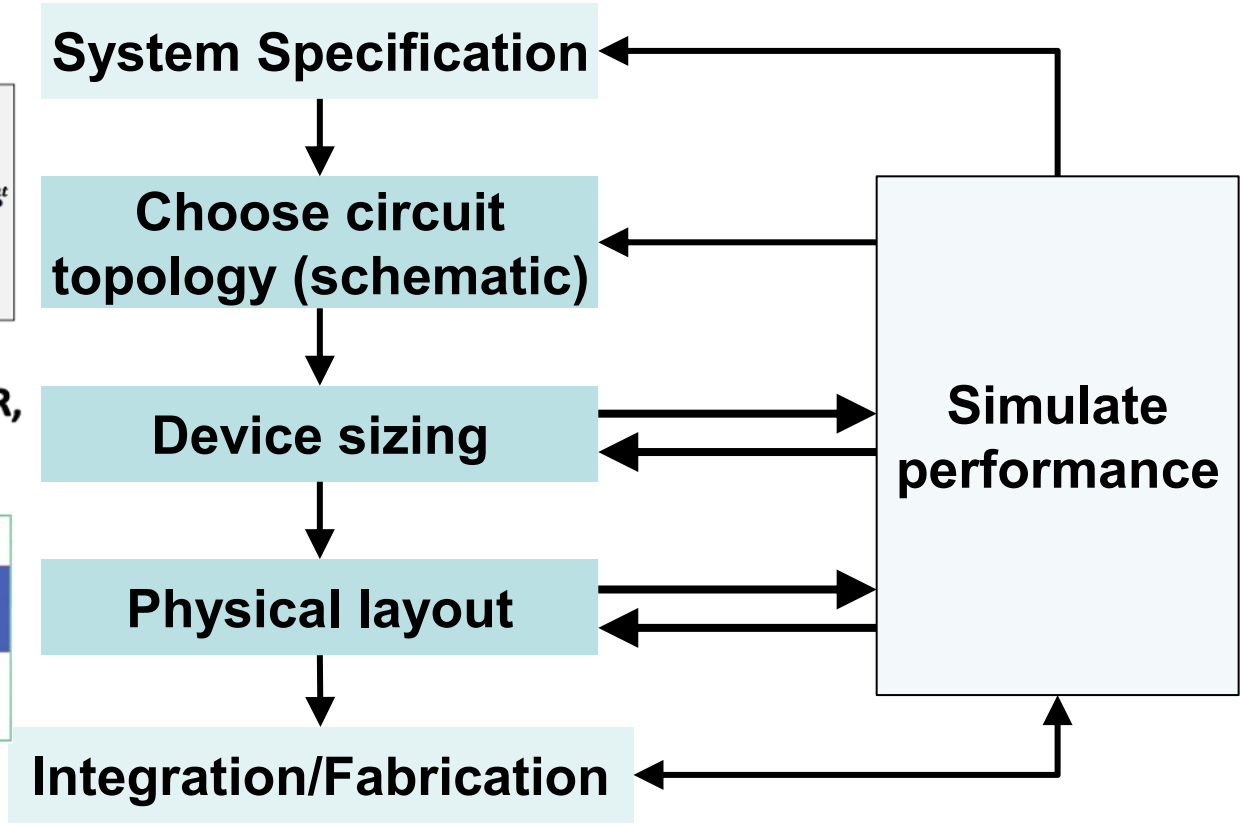


[Razavi, Design of Analog IC]



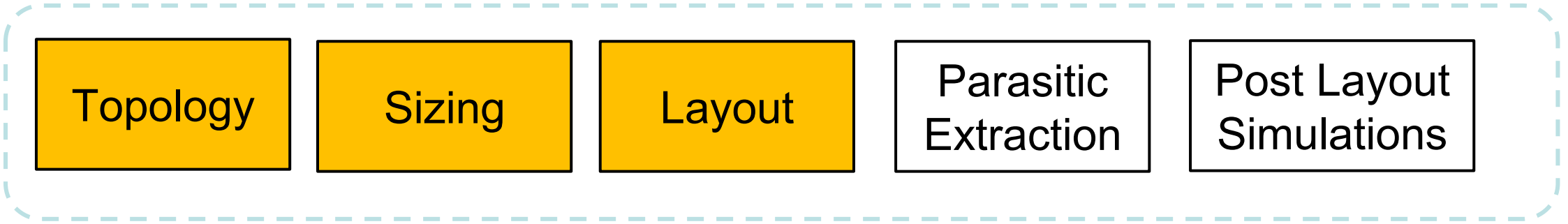
L, W, fingers, R, C, biases, etc.





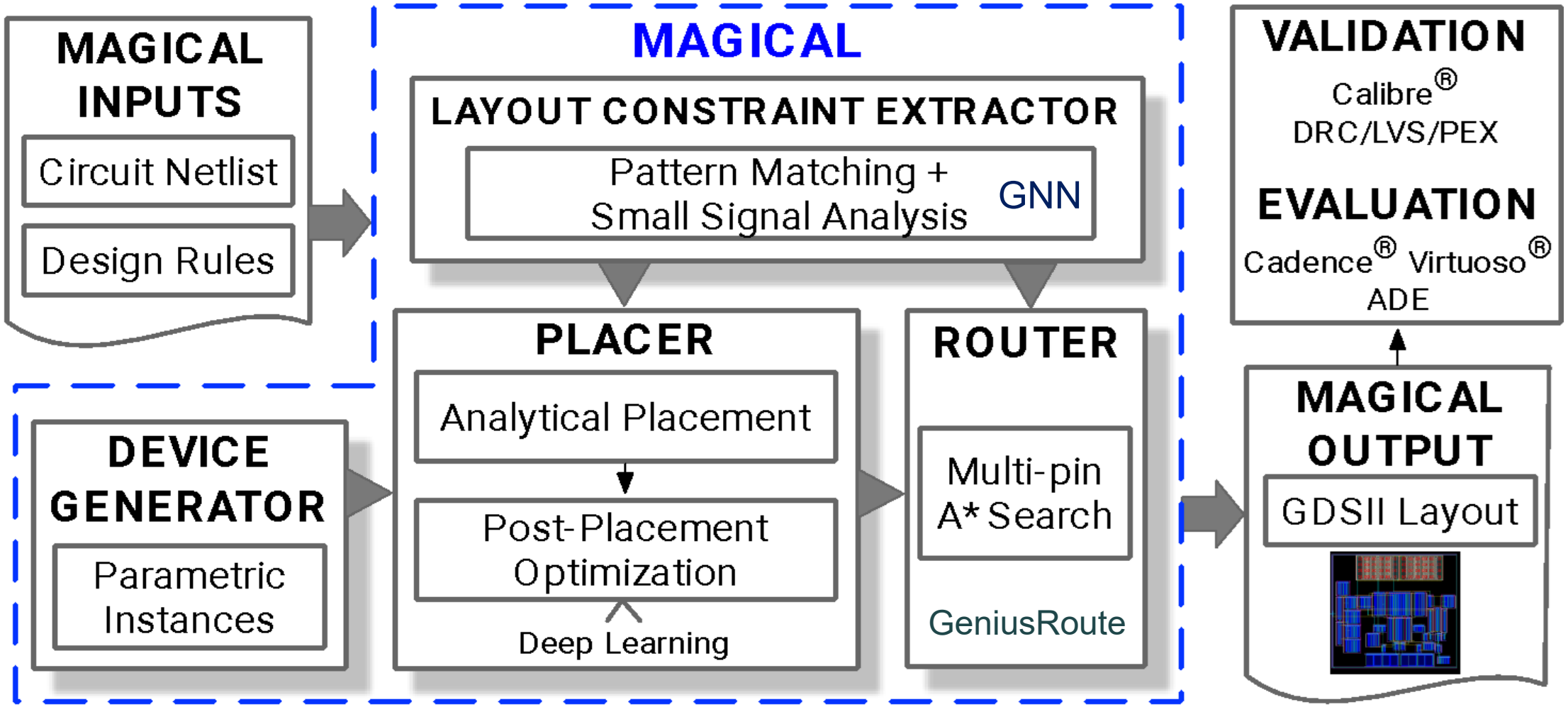
- Many design specs to juggle
- Heavily rely on designer experience
- **Tons of simulations**

End to End Analog Design Automation (?)



- Our overarching goal (dream): an end-to-end analog DA flow?
- **Analog "S&PR", like RTL to GDSII for digital**
  - Need to connect different steps together
  - Surrogate modeling to speed up the feedback-loop
- **LLM and Agentic AI as design co-pilot**

MAGICAL Layout Automation System



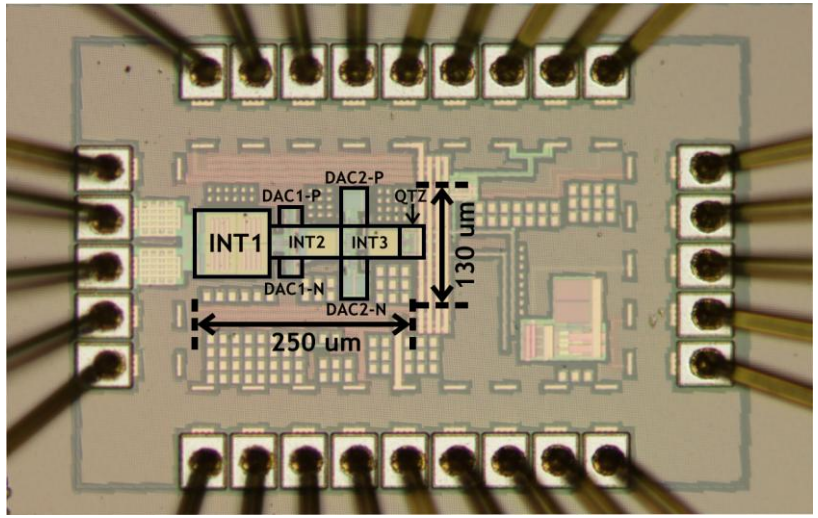
https://github.com/magical-eda/MAGICAL

- 20+ papers; open-sourced

Fork 59 | Starred 258

MAGICAL Tapeout Proven

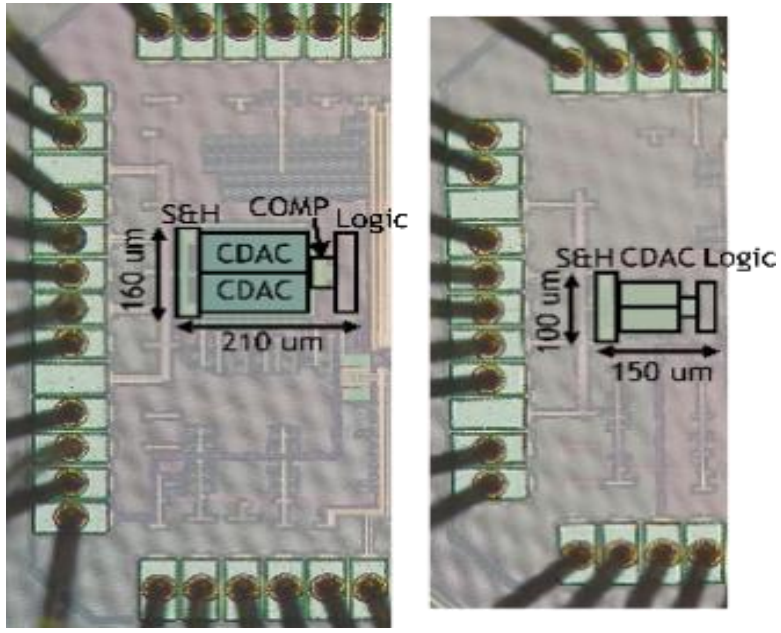
- 1GS/s 3rd-order high-performance continuous time ΔΣ modulator
- State-of-the-art performance, cf. original design [SSC-L'20]
- Various sub-block types
- **O(month)** vs. **O(min)** for layout



[Chen+, CICC'21]

TSMC 40nm

- Extend MAGICAL to larger AMS systems
- OpenSAR for end-to-end SAR ADC compilation



12-bit ADC **10-bit ADC**

[Liu+, ICCAD'21, SSC-L'22]

Analog Sizing using RL [DAC'21 BPA Candidate]

minimize $Power$
s.t. DC Gain > 60 dB
CMRR > 80 dB
PSRR > 80 dB
Output Swing > 2.4 V
Output Noise $< 3 \times 10^{-4}$ V_{rms}
Phase Margin > 60 deg
Unity Gain Frequency > 40 MHz
Settling Time $< 3 \times 10^{-8}$ s
Static error < 0.1
Saturation Margin > 50 mV

Specifications

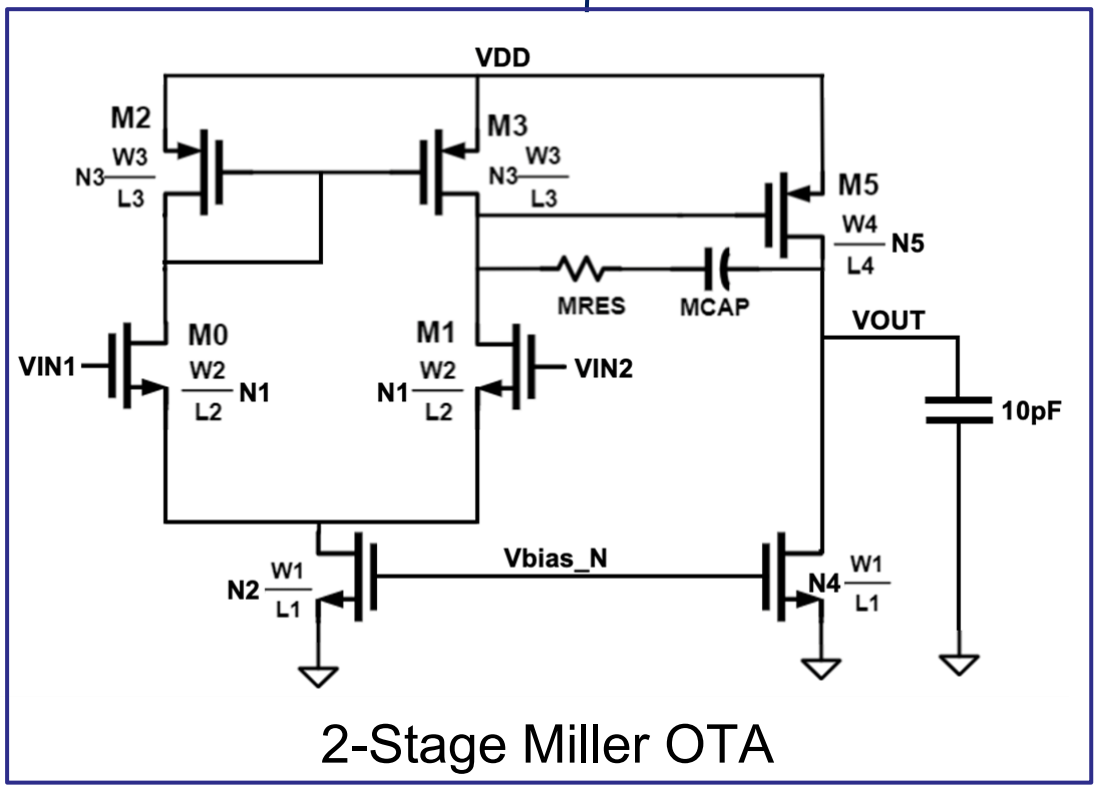
TABLE I: Design parameters and their ranges for Miller OTA

Parameters	LB	UB	Parameters	LB	UB
L1(μm)	0.18	2	MCAP(fF)	10	2000
L2(μm)	0.18	2	MRES(Ω)	100	100k
L3(μm)	0.18	2	N1 (integer)	1	10
L4(μm)	0.18	2	N2 (integer)	1	10
L5(μm)	0.18	2	N3 (integer)	1	10
W1(μm)	0.22	150	N4 (integer)	1	10
W2(μm)	0.22	150	N5 (integer)	1	10
W3(μm)	0.22	150	N6 (integer)	1	10
W4(μm)	0.22	150	NC (integer)	1	10
W5(μm)	0.22	150	NR (integer)	1	10

W:width; L=length; UB:upper bound; LB:lower bound

Design Parameters & Ranges

Topology

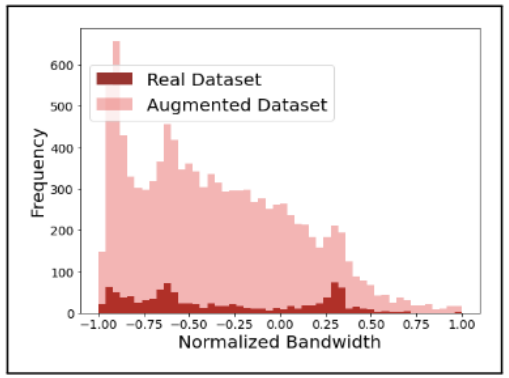


2-Stage Miller OTA

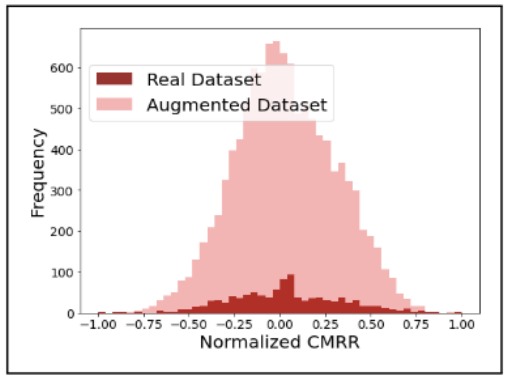
➔ **SoTA results to meet stringent specs while obtaining best results**

[Budak+, DAC'21]

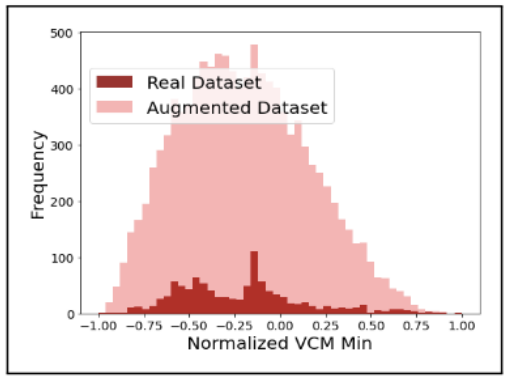
Sized-Topology Selection [Poddar+, DATE'24]



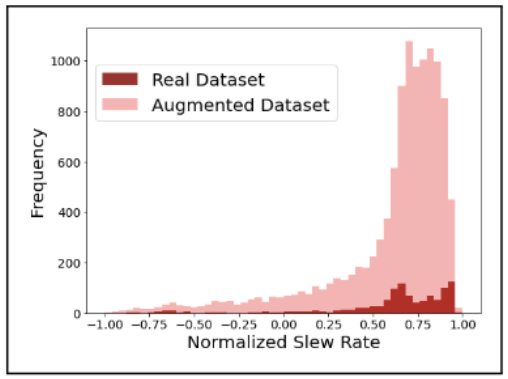
(a) Normalized BW



(b) Normalized CMRR



(c) Normalized VCM Min



(d) Normalized Slew Rate

- Previous methods generate/pick topologies first, then size and select, using simulations/ML, etc.
- Can we start from a rich set of data points with sized topology library (which can be generated offline, with best sizing algorithms/simulations)?
- Dataset augmentation, e.g., using VAEs and GANs
- Then we can skip computationally intensive tasks

SRC CADT Annual Review, 1st Place in Poster Competition

AnalogCoder: Analog Circuit Design via LLM

Method	Fully Automated [1]	Auto Fix Errors [2]	Benchmark	Open-Source	Training-Free	Circuit Type
ChipChat [7]	×	×	✓	✓	✓	Digital
ChipGPT [8]	×	×	✓	×	✓	Digital
VeriGen [9]	✓	×	✓	✓	×	Digital
AutoChip [10]	✓	✓	×	✓	✓	Digital
VerilogEval [12]	✓	×	✓	×	×	Digital
RTLLM [13]	✓	×	✓	✓	✓	Digital
RTLfixer [14]	✓	✓	×	✓	✓	Digital
RTLCoder [15]	✓	×	×	✓	×	Digital
ChipNeMo [18]	✓	×	×	×	×	Digital[3]
BetterV [16]	✓	×	×	×	×	Digital
AnalogCoder	✓	✓	✓	✓	✓	Analog

Analogcoder: Analog circuit design via training-free code generation

~~31~~ 80 2025

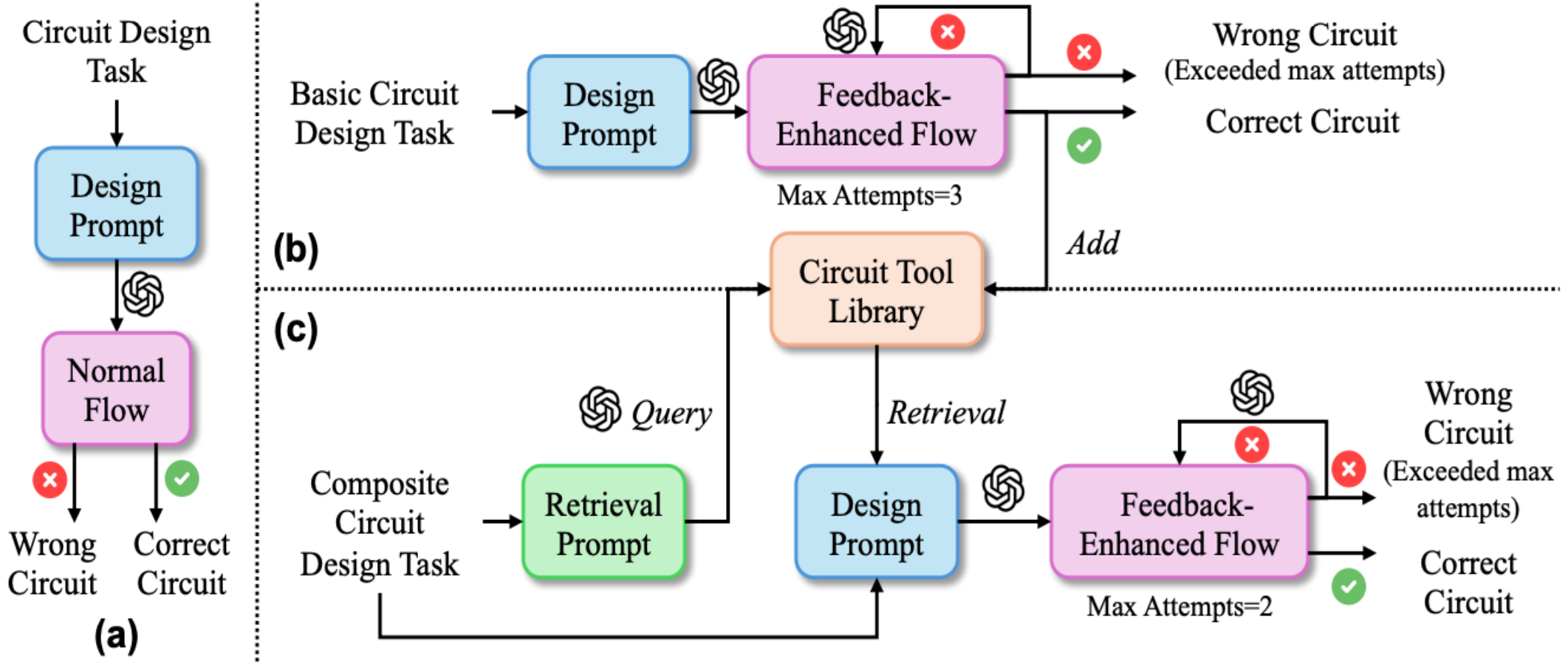
Y Lai, S Lee, G Chen, S Poddar, M Hu, DZ Pan, P Luo

Proceedings of the AAAI Conference on Artificial Intelligence 39 (1), 379-387

AAAI 2025 Oral (< 5% acceptance rate), already got 80 citations!

Open sourced: https://github.com/laiyao1/AnalogCoder

AnalogCoder Design Flow (Training-Free)



AnalogCoder-Pro: AnalogCoder with Multimodal & Optimization

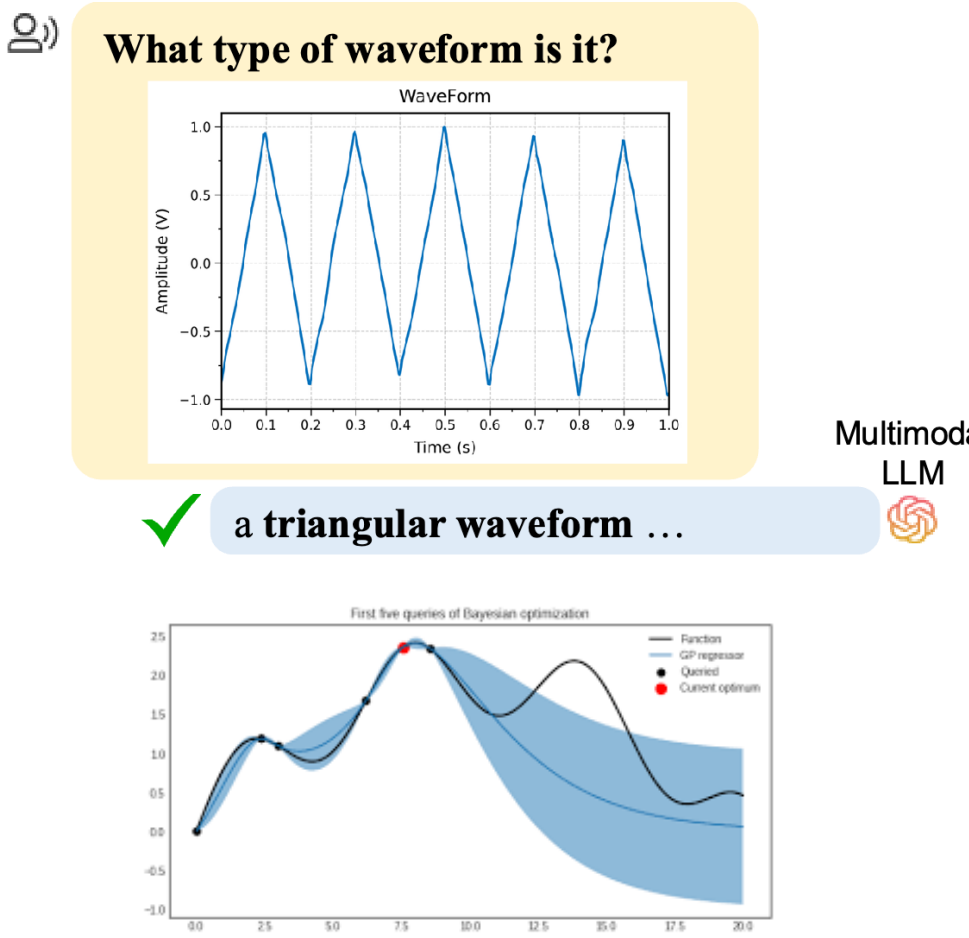
https://arxiv.org/abs/2508.02518

TABLE I **LLM-based Methods for Analog Design**

Work	Multiple Types[1]	Training-Free	MLLM Debug[2]	Circuit Gen.	Circuit Opt.	Open-Source
CktGNN [23]				●	●	●
LADAC [24]	●	●			●	
ADO-LLM [25]	●	●			●	
LaMAGIC [26], [27]				●	●	
AnalogCoder [28]	●	●	○	●		●
SPICEPilot [29]	●	●	○	●		
LEDRO [30]		●			●	
Aritsan [31]				●	●	
AmpAgent [32]		●			●	
Atelier [33]		●		●	●	
AnalogXpert [34]		●	○	●		
Malasa-Chai [35]	●			●		●
AnalogGenie/Lite [36], [37]	●			●	●	●
AnalogFed [38]	●			●	●	
AutoCircuit-RL [39]				●	●	
SPICEAssistant [40]		●	○	●	●	
AnalogCoder-Pro	●	●	●	●	●	●

[1] Whether the work supports multiple circuit type designs.

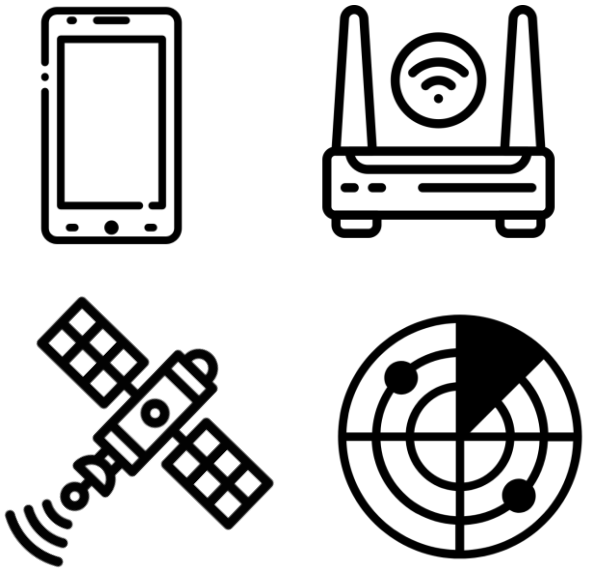
[2] ● - Full multi-modal debugging capability by signal images (e.g., waveform, frequency response), ○ - Text-only debugging.



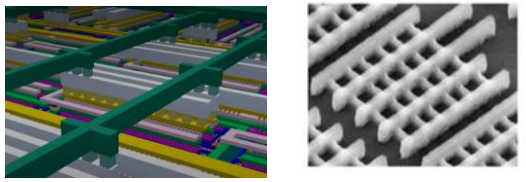
https://github.com/laiyao1/AnalogCoderPro

RFIC (Radio Frequency Integrated Circuit)

- RFIC components are fundamental in wireless systems
- RFIC = active (transistors) + **passive** components
- **Passive** designs are **bottlenecks** for RFIC design

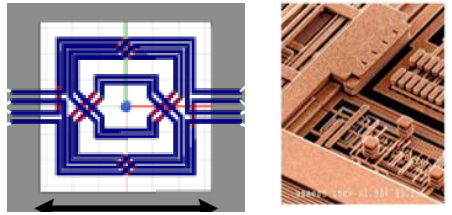


[Behzad Razavi, RF Microelectronics]



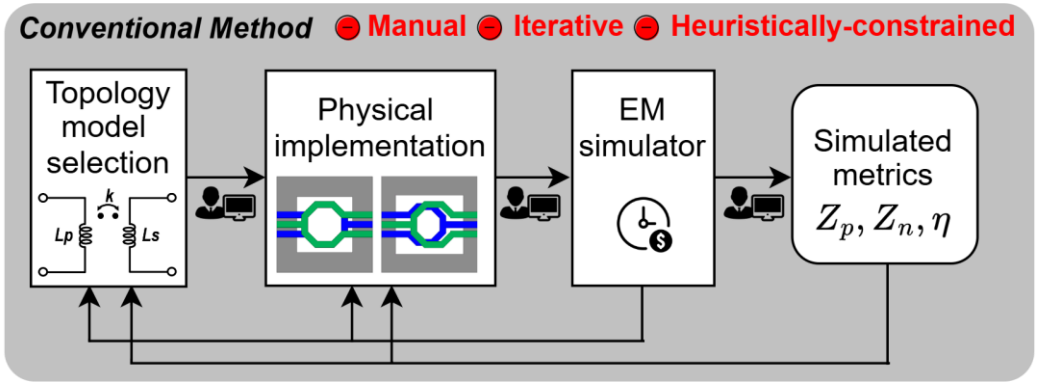
Active Components

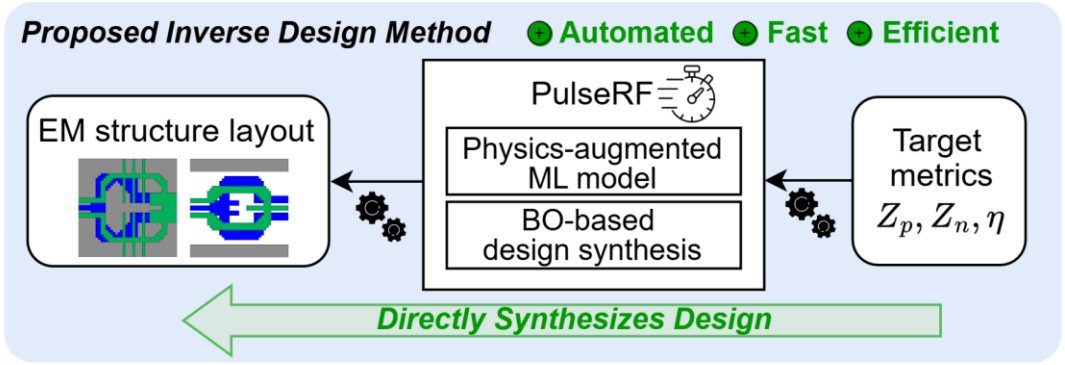
Passive Components



PulseRF for RFIC Passive Design

- Conventional vs. our **PulseRF** approach [Chae+, ICCAD'24]





☹ Slow simulation restricts the number of optimization iterations possible

☹ Optimization is confined to a limited set of topology templates

☺ Physics-augmented ML model for fast design evaluation

☺ Bayesian optimization-based inverse design

☺ Super-human, non-intuitive designs

➔ **UT Team won the very first NSTC Jump Start R&D Project!**

3DHI of Everything

- Digital/FPGA, analog, RF, photonics, emerging memory, …
- A lot of “mismatches” and “multi-physics” (thermal, stress, …)
- All kinds of AI-driven EDA tools needed for modeling, optimization, and STCO (system-technology co-optimization)

Jul 18, 2024

UT’s Texas Institute for Electronics Awarded $840M To Build a DOD Microelectronics Manufacturing Center, Advance U.S. Semiconductor Industry

TSV Stress-Aware Full-Chip Mechanical Reliability Analysis and Optimization for 3D IC

By Moongon Jung, Joydeep Mitra, David Z. Pan, and Sung Kyu Lim

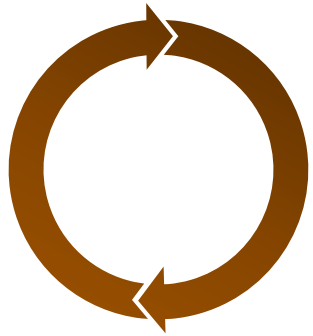
Communications of ACM
01/2014 Research Highlights

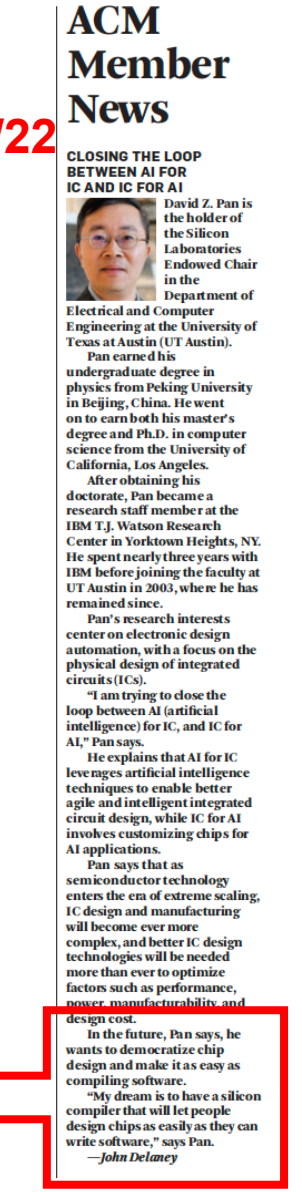
Conclusion

- AI for chip design: everything, everywhere!
  - PPACT, digital, analog, RF, **3DHI**, …
  - Prediction, Acceleration, Generation, Optimization …
  - **Verification!**
  - **Architecture Exploration** …
- Issues: DATA, model generalization, transferability, bias, explainability, optimality…
- Still far away from **super-human "all at once!"** **(my dream ☺)**

"My **dream** is to have a silicon compiler which can let people design chips as easily as they can write software"

Jan. 2023 Issue,
Interviewed 06/22
ChatGPT released 11/22





ACM Member News

CLOSING THE LOOP BETWEEN AI FOR IC AND IC FOR AI

David Z. Pan is the holder of the Silicon Laboratories Endowed Chair in the Department of Electrical and Computer Engineering at the University of Texas at Austin (UT Austin).

Pan earned his undergraduate degree in physics from Peking University in Beijing, China. He went on to earn both his master's degree and Ph.D. in computer science from the University of California, Los Angeles.

After obtaining his doctorate, Pan became a research staff member at the IBM T.J. Watson Research Center in Yorktown Heights, NY. He spent nearly three years with IBM before joining the faculty at UT Austin in 2003, where he has remained since.

Pan's research interests center on electronic design automation, with a focus on the physical design of integrated circuits (ICs).

"I am trying to close the loop between AI (artificial intelligence) for IC, and IC for AI," Pan says.

He explains that AI for IC leverages artificial intelligence techniques to enable better agile and intelligent integrated circuit design, while IC for AI involves customizing chips for AI applications.

Pan says that as semiconductor technology enters the era of extreme scaling, IC design and manufacturing will become ever more complex, and better IC design technologies will be needed more than ever to optimize factors such as performance, power, manufacturability, and design cost.

In the future, Pan says, he wants to democratize chip design and make it as easy as compiling software.

"My dream is to have a silicon compiler that will let people design chips as easily as they can write software," says Pan.

—*John Delaney*

AI for Chip Design