Overcoming Obstacles to Model-based Verification

Verification Futures Austin

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Overcoming Obstacles

Outline

Overcoming Obstacles to Model-based Verification

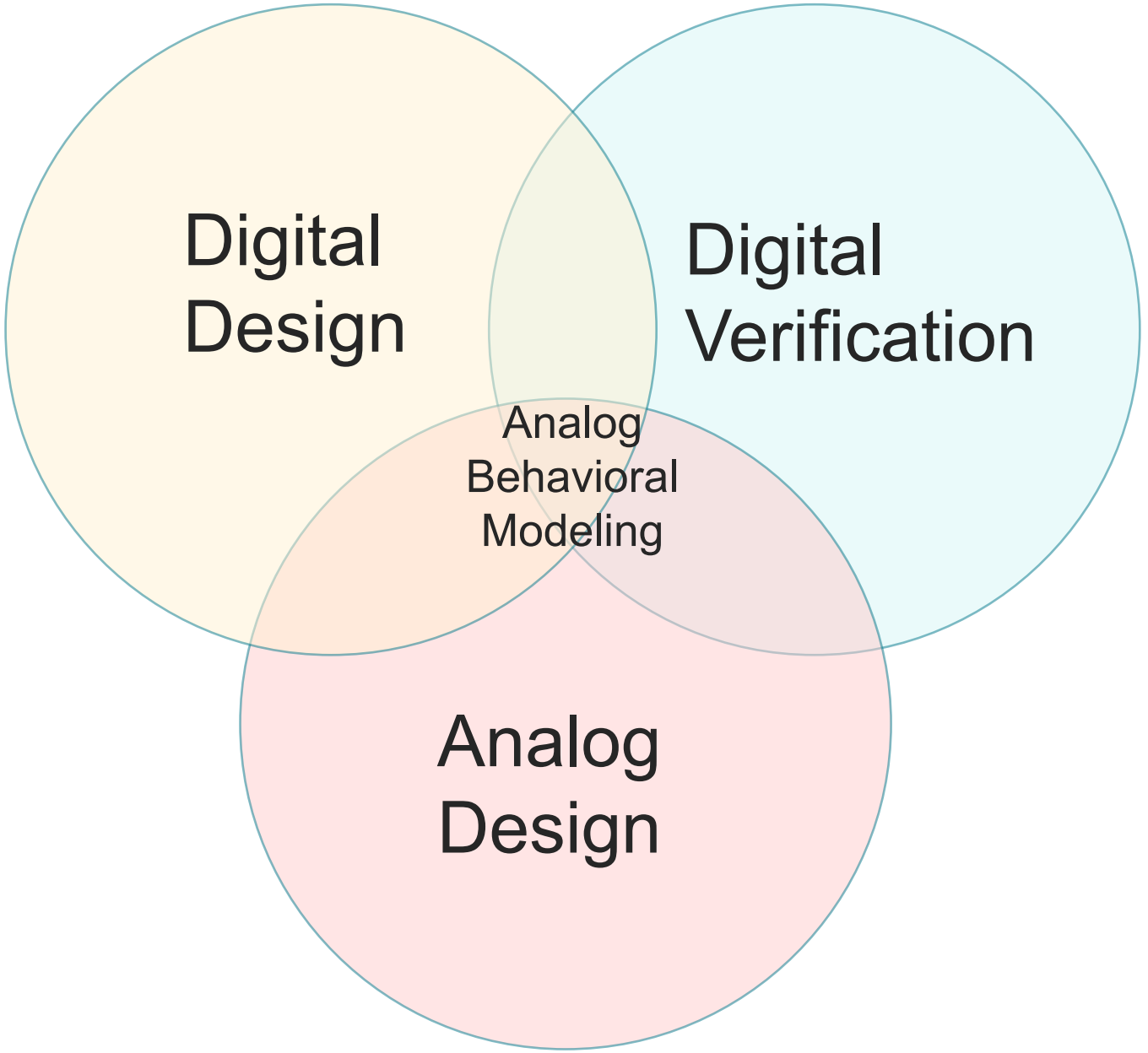
- You won’t believe what #1 is!
- One weird trick …
- Don’t make me come over there
- As Ye sow, so shall Ye reap
- Models, models everywhere!

Our focus will be on behavioral models of analog system components

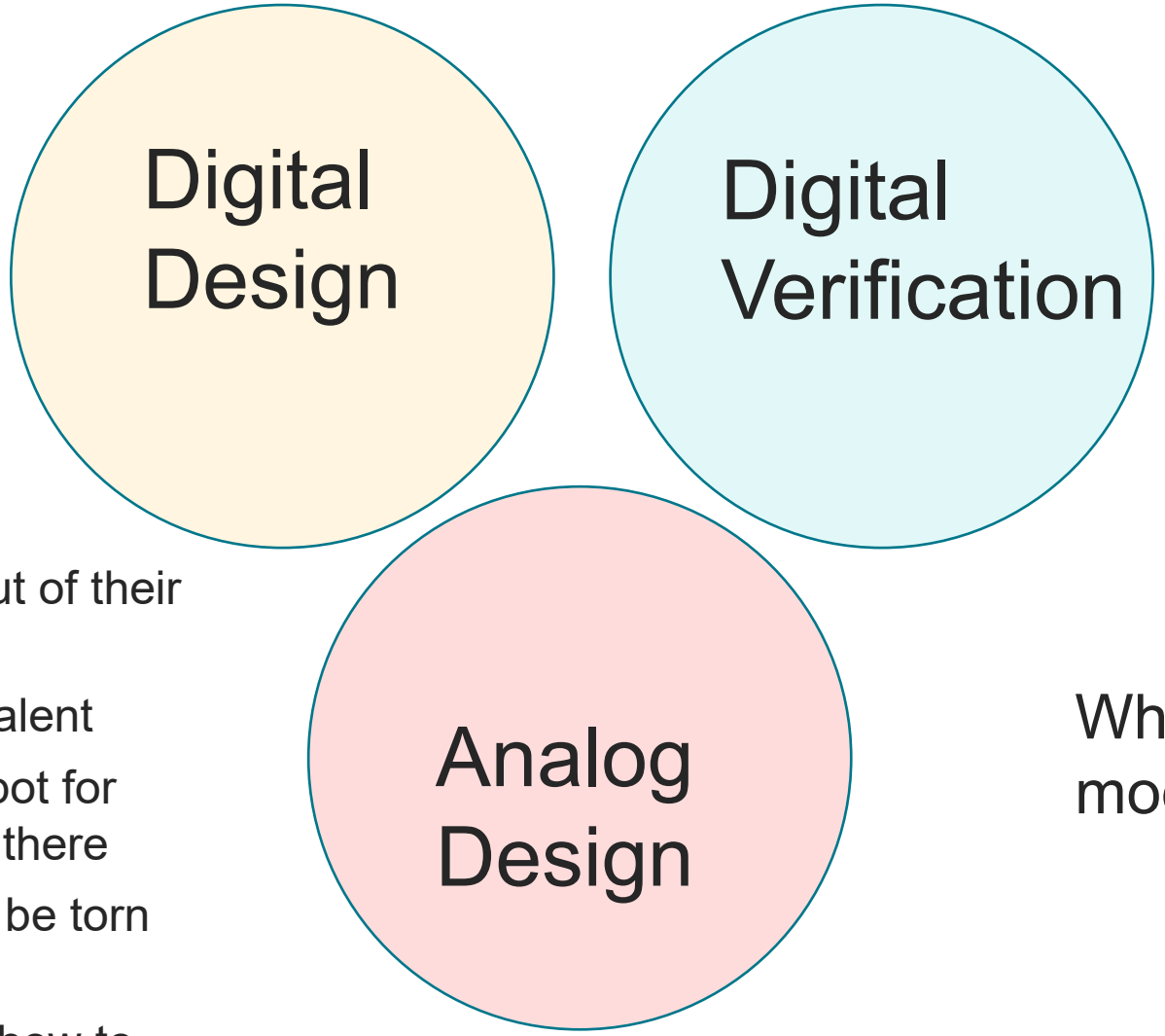
People Have Questions (an incomplete list)

- What modeling language should I use?
- How do I make models?
- How can I make models visible to those who need them?
- How am I sure the models are correct?
- How do models fit into my verification flow?
- How can models support my overall verification goals?
- What should my organization look like to take advantage of a model-based verification strategy?

IC Design Disciplines



YOUR Organization



- No one wants to move out of their comfort zone
- Hard to bring in outside talent
- If there were already a spot for modelers, they would be there
- Obstacles would already be torn down
- IT and CAD would know how to support

Where do my analog modelers live?

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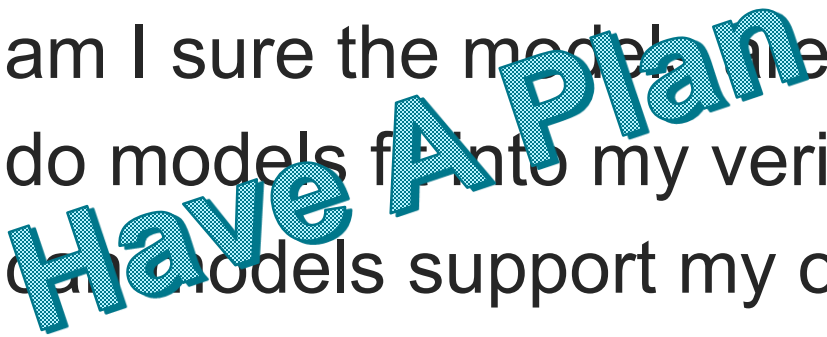
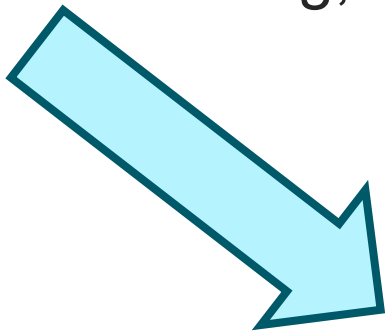


Essential Elements of a Verification Plan

- Know the features and specifications you are testing for
- Detailed plan for testing, scenarios and use cases, metrics for success



- What models are needed and what they need to do

- Models of system elements
- Models of things connected to the system
- Various model abstractions
- What checks of the models are needed
- How much time/people/money needed

Examples of how plans can feed model requirements

1. Requirement: “has an I2C”

I2C uses a PLL-based clock

PLL configuration registers are controlled by I2C

Implicit requirement: “I2C must stay synchronized over changes to its clock”

Demands system-level simulation

PLL model must respond realistically to configuration setting changes

Metric: no lost packets

2. Requirement: Interference Immunity

A. Digital Signal Processing responds to detected interference by adjusting bias of RF Front-end

Signal path models must be able to carry interferer information to DSP

B. Interference immunity only depends on VCO far-out phase noise

Only VCO device noise, inductor Q, and on-chip losses matter. No benefit to including phase noise in PLL model.

Knowing what the models need to do tells you what to check to verify that the models are correct. These checks are also part of the plan!!!

Have A Plan

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Model Storage and Availability

Digital Design, Digital Verification

"Models are text-based, they should be managed with git."

"I don't use Virtuoso. Too much overhead."

Analog Designer, Model Validator

"I need the models in Virtuoso so I can compare them to the original circuits."

"They are part of the analog netlist, so I need them here."

Both groups can be satisfied, but it requires organizational discipline.

See: Tips for a Successful Digital Mixed Signal System Verification
https://support.cadence.com/apex/ArticleAttachmentPortal?id=a1OPP000000GwRR2A0&pageName=ArticleContent

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SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification Training

Instructor-Led Schedule + Online Courses +

Length: 20 virtual sessions with Instructor (2 hours per session)

Digital Badges

Course Description

Semiconductor ICs and SoCs increasingly include both digital and analog IP. As such, mixed-signal verification is a sign-off requirement and accurate, high-speed models are needed to achieve that. IEEE 1800 SystemVerilog includes constructs to support these models known collectively as Real Number Modeling (SV-RNM).

This advanced course consists of 27 video modules and associated code examples for the lab

CONTACT TRAINING

https://www.cadence.com/en_US/home/training/all-courses/86274.html

Common Objections

“We’ve been doing it this way for thirty years.”

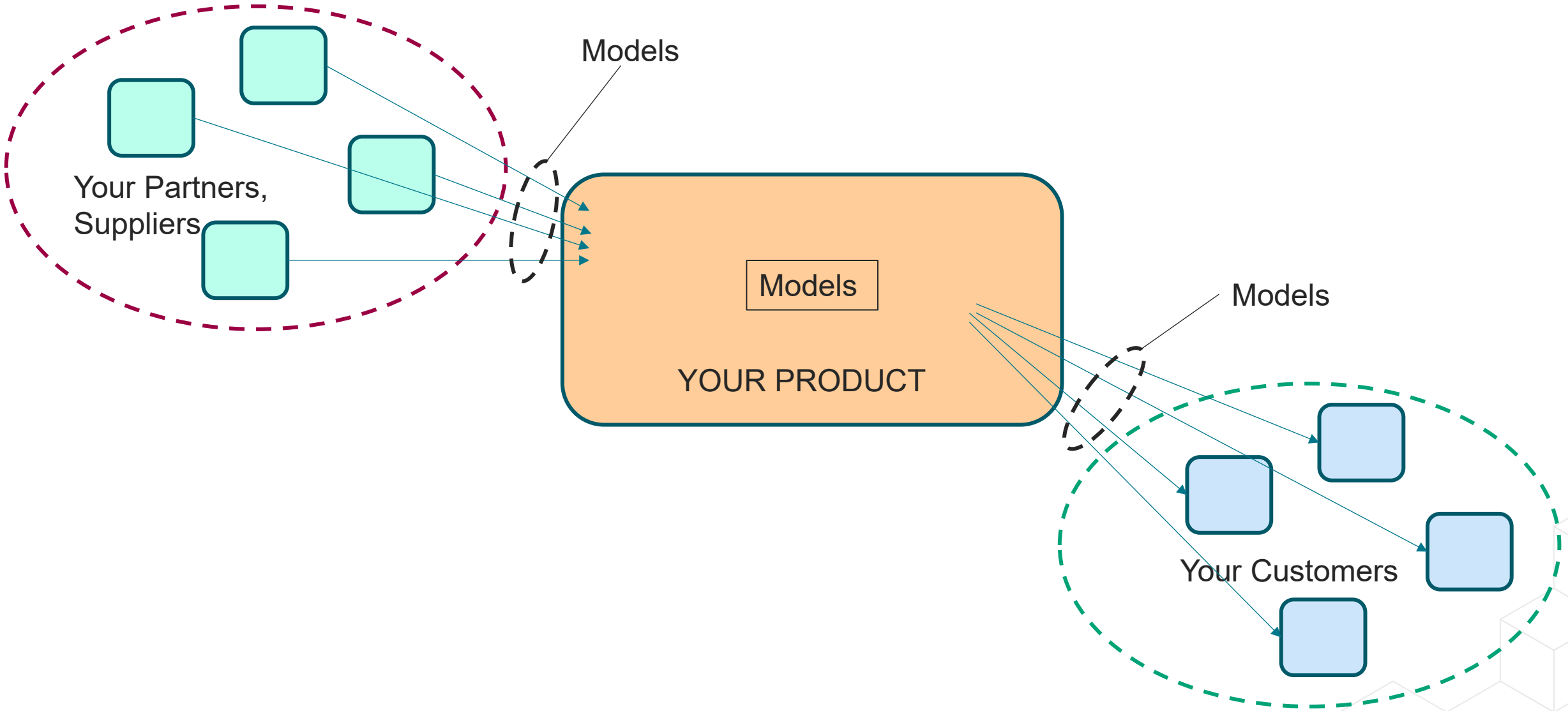
“I don’t code.”

“I don’t want *those guys* breaking my simulations.”

“We don’t have time (money, people) in the schedule.”

“Maybe next project …”

The Model Value Chain



You can get to a model-based verification flow

- Tune up your organization – make modelers feel at home.
- Institute up-front verification planning as part of your process.
- Get everyone involved with creating, storing, and using models – designers, verifiers, IT, CAD, Project Management.
- Learn how to model.
- Recognize the benefits: reduced defects, greater insights into system behavior, improved relationships with customers and suppliers.