Questa™ One
SFV

Faster Engines
Faster Engineers
Fewer Workloads
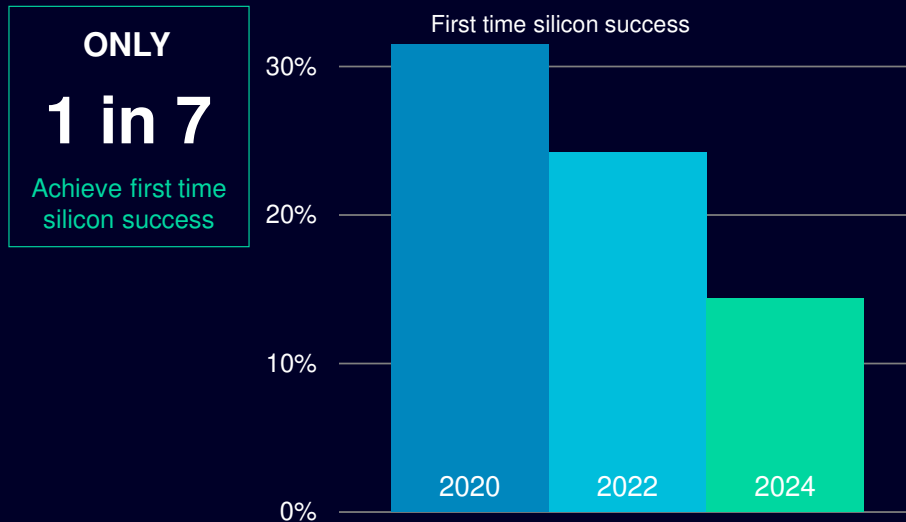
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Industry challenges

Current headwinds impacting success

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First silicon success declining faster, projects finishing later in recent years
Decline in ASIC first silicon success & increase in projects behind schedule
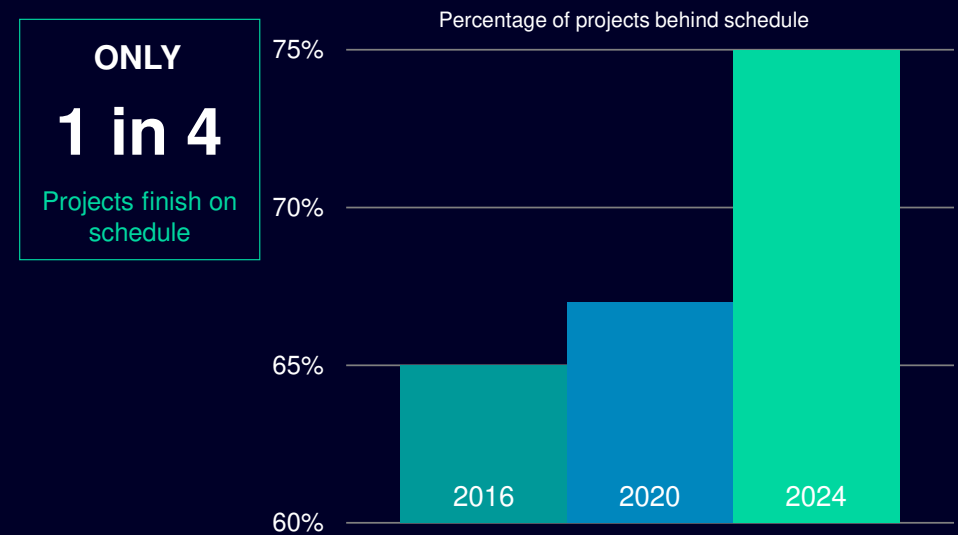
First silicon success

Number of spins before production

ONLY
1 in 7
Achieve first time silicon success

First time silicon success

	2020	2022	2024

(bar chart: 2020 ≈ 31%, 2022 ≈ 24%, 2024 ≈ 14%; y-axis 0%–30%)

Decline in first silicon success combined with increasing wafer and mask cost

Schedule overruns

Projects finishing late

ONLY
1 in 4
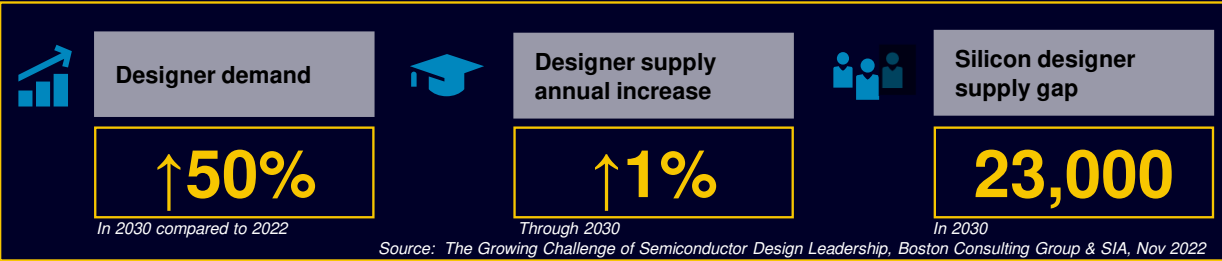Projects finish on schedule

Percentage of projects behind schedule

	2016	2020	2024

(bar chart: 2016 ≈ 65%, 2020 ≈ 67%, 2024 ≈ 75%; y-axis 60%–75%)

Despite declines in first-silicon success, teams are investing more in development

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Ever-present productivity gap is growing, with resource deficits predicted
Growth in DV teams, where possible, only slowed the growing gap

DV engineers	Functional respins	Schedule overruns
↑**29%**	↑**15%**	↑**10%**
Since 2020	*Since 2020*	*5% worse than 2020*

Source: Siemens EDA and Wilson Research Group, 2024 Functional Verification Study

Hardware & software co-development	Compliance amidst customization	Massive-scale interconnect
↑**27%**	↑**30%**	↑**20%**
Since 2016	*Since 2020*	*Since 2020*

Source: Wilson Research Group and Siemens EDA, 2022 Functional Verification Study

Designer demand	Designer supply annual increase	Silicon designer supply gap
↑**50%**	↑**1%**	**23,000**
In 2030 compared to 2022	*Through 2030*	*In 2030*

Source: The Growing Challenge of Semiconductor Design Leadership, Boston Consulting Group & SIA, Nov 2022

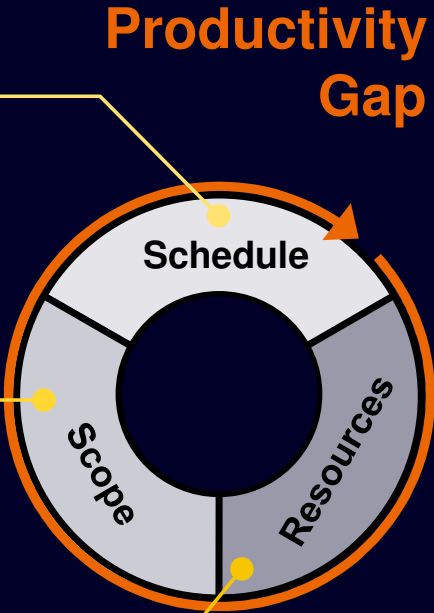**Minimal time-to-market impact**
Investing in verification resources did not deliver expected returns

Increasing complexity
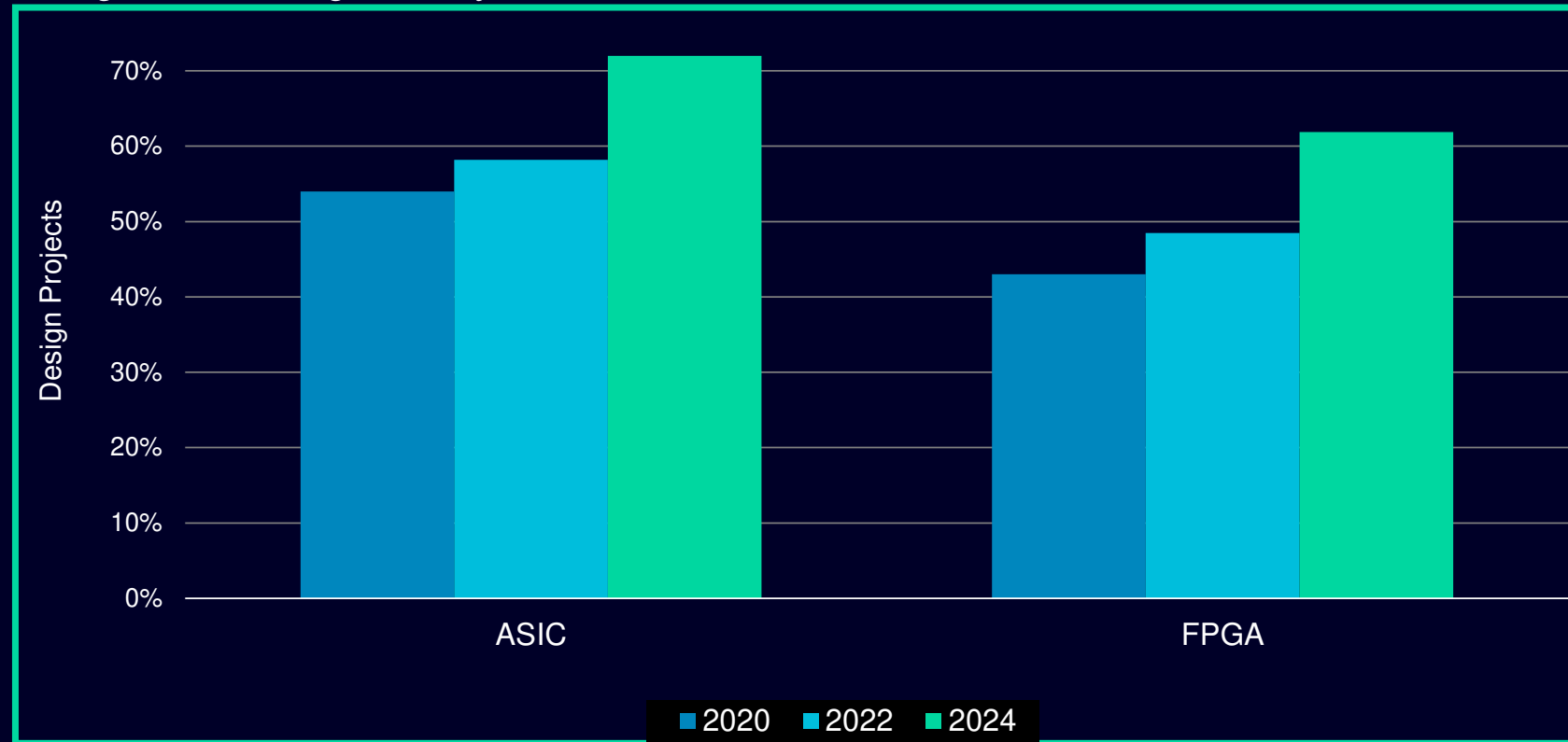Continuing the never-ending trend

Labor shortages
Growing gap of talent emerging from education

Productivity Gap

Schedule · Scope · Resources

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Security features deliver no security if not verified
Rate of projects including security requirements increase faster in recent years

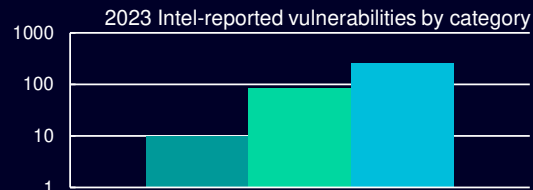Designs containing security features

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Failure-intolerant applications are increasing in high-vulnerability environment
Current verification methods can not deliver proof of compliance

Hardware vulnerabilities in CPUs and GPUs

2023 Intel-reported vulnerabilities by category

- HW
- FW
- SW

https://www.intc.com/news-events/press-releases/detail/1677/intel-releases-2023-product-security-report-highlighting20240223917900/en/

Security and assurance requirements

enisa
European Network and Information Security Agency

NATIONAL SECURITY AGENCY · UNITED STATES OF AMERICA

Security features In designs

ASIC	FPGA
↑**33%**	↑**44%**
Since 2020	*Since 2020*

Source: Siemens EDA and Wilson Research Group, 2024 Functional Verification Study

Vulnerabilities
Increased awareness is not eliminating issues

Requirements
New and increasing frequently

Complexity
More features to verify to ensure compliance & security in design

Increasing demand for hardware assurance

- **Supply chain vulnerabilities**
- **Data confidentiality & integrity**
- **National Security concerns**
- **Regulatory requirements**
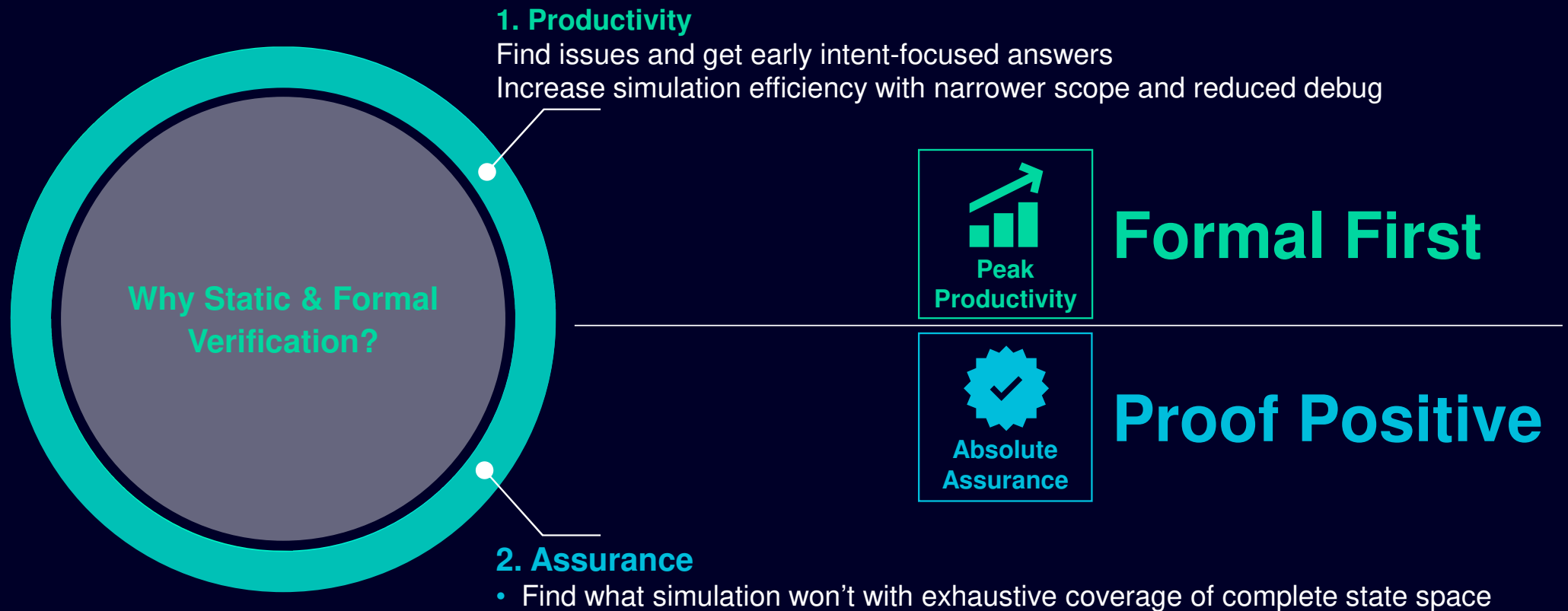- **Growing complexity**
- **Increased security threats**

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Addressing these challenges with static & formal technologies

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Static and formal are critical to success amidst today's industry challenges
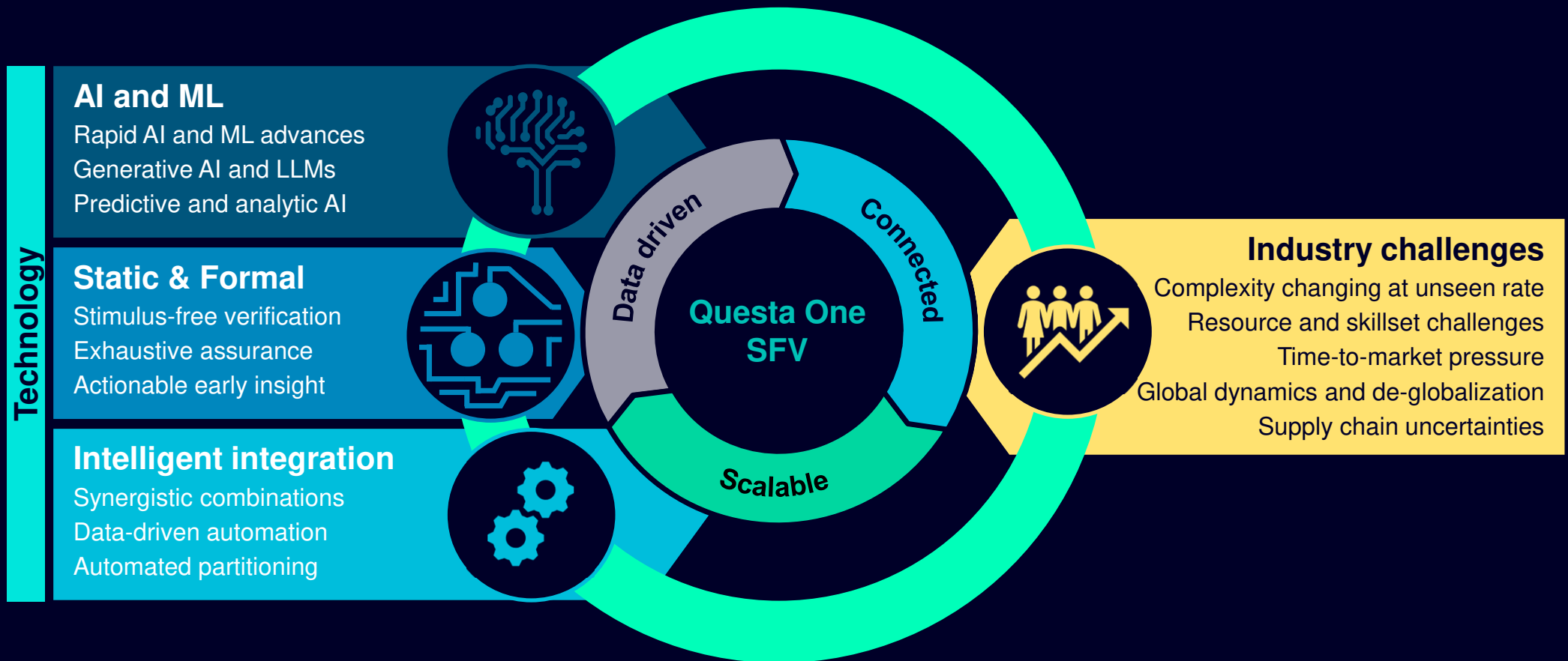Complementary to simulation, deliver assurance and productivity

1. Productivity
Find issues and get early intent-focused answers
Increase simulation efficiency with narrower scope and reduced debug

Why Static & Formal Verification?

Peak Productivity

Formal First

Absolute Assurance

Proof Positive

2. Assurance
• Find what simulation won't with exhaustive coverage of complete state space

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Convergence of new technology and new industry challenges
AI/ML, automation and integration enable new verification flows and solutions

Technology

AI and ML
Rapid AI and ML advances
Generative AI and LLMs
Predictive and analytic AI

Intelligent integration
Synergistic combinations
Data-driven automation
Automated partitioning

Opportunity

Industry challenges
Complexity changing at unseen rate
Resource and skillset challenges
Time-to-market pressure
Global dynamics and de-globalization
Supply chain uncertainties

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Introducing Questa One SFV: Purpose-built stimulus-free verification
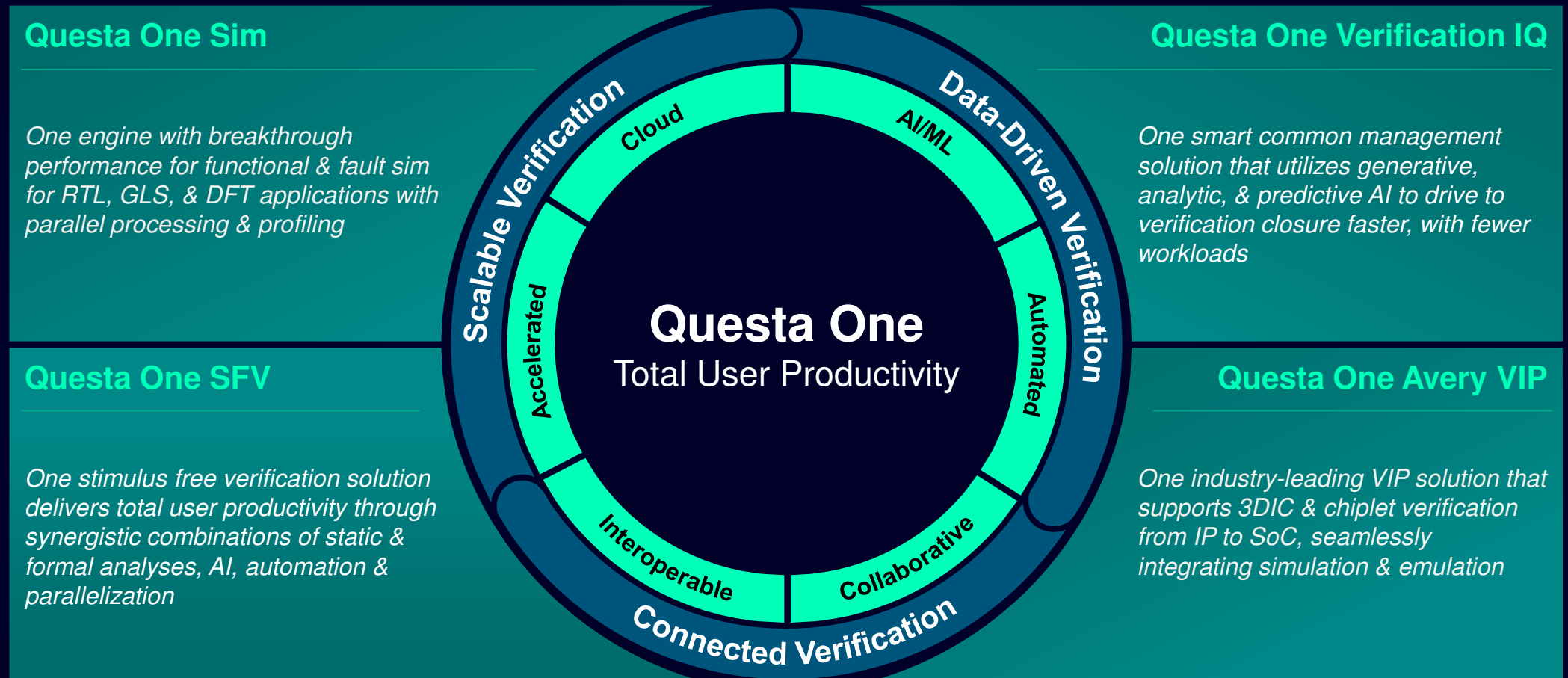## AI/ML, automation and integration enable new verification flows and solutions

Technology

AI and ML
Rapid AI and ML advances
Generative AI and LLMs
Predictive and analytic AI

Static & Formal
Stimulus-free verification
Exhaustive assurance
Actionable early insight

Intelligent integration
Synergistic combinations
Data-driven automation
Automated partitioning

Data driven
Connected
Scalable

Questa One SFV

Industry challenges
Complexity changing at unseen rate
Resource and skillset challenges
Time-to-market pressure
Global dynamics and de-globalization
Supply chain uncertainties

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What is
Questa One SFV?

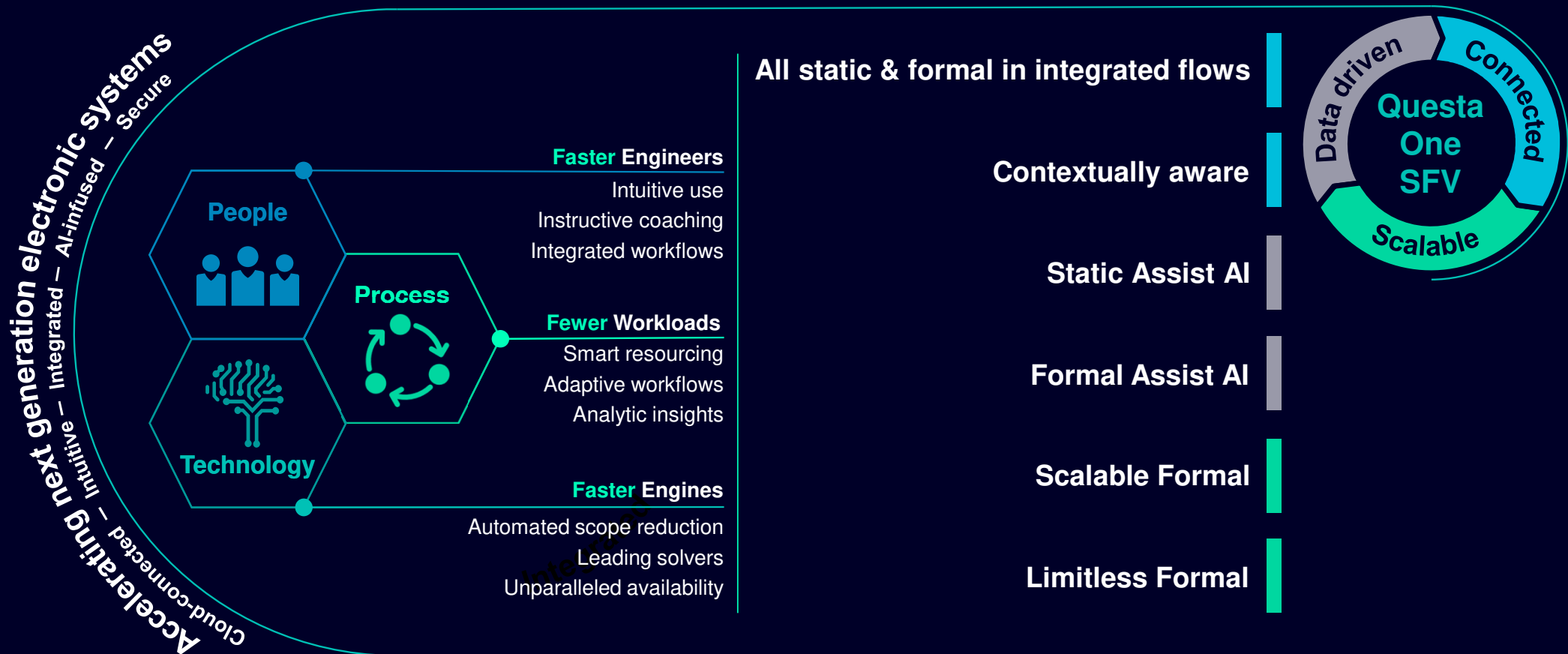Full availability, full utilization, scalable performance delivering stimulus-free verification for today's challenges

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Questa One Smart Verification Solution enabled by AI
Faster engines, faster engineers, fewer workloads

Questa One Sim

One engine with breakthrough performance for functional & fault sim for RTL, GLS, & DFT applications with parallel processing & profiling

Questa One SFV

One stimulus free verification solution delivers total user productivity through synergistic combinations of static & formal analyses, AI, automation & parallelization

Questa One Verification IQ

One smart common management solution that utilizes generative, analytic, & predictive AI to drive to verification closure faster, with fewer workloads

Questa One Avery VIP

One industry-leading VIP solution that supports 3DIC & chiplet verification from IP to SoC, seamlessly integrating simulation & emulation

Questa One
Total User Productivity

Scalable Verification · Cloud · AI/ML · Data-Driven Verification · Accelerated · Automated · Interoperable · Collaborative · Connected Verification

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Questa One SFV: Integrated stimulus-free verification
Delivering static & formal's long-held promise of solving next-generation problems

People

Process

Technology

Faster Engineers
Intuitive use
Instructive coaching
Integrated workflows

Fewer Workloads
Smart resourcing
Adaptive workflows
Analytic insights

Faster Engines
Automated scope reduction
Leading solvers
Unparalleled availability

Accelerating next generation electronic systems
– Integrated – AI-infused – Secure
– Intuitive –
Cloud-connected

All static & formal in integrated flows

Contextually aware

Static Assist AI

Formal Assist AI

Scalable Formal

Limitless Formal

Data driven

Connected

Questa One SFV

Scalable

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Questa One SFV: a new product encapsulating analyses, AI and IVE
Enabling full utilization and availability within a single product

Questa One Integrated Verification Environment (IVE)
Integration of analyses, AI/ML and automation
Insight services
User interfaces

AI/ML and Automation
Generative AI and LLMs
Predictive and Analytic AI
Automation of flows and processes

Analyses
20 legacy products combined into a single package

Static & Formal Foundation
Best-in-class library of solvers
Best-in-class orchestration
Limitless Formal parallel scalability

Questa OneSpin Static & Formal Product Line

Questa One SFV
- Single product
- AI/ML features
- Synergistic features
- 20 analyses
- Flexible scalability

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What is Questa One IVE?

The Integrated Verification Environment is foundational technology enabling increased total user productivity

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Questa One SFV: Integrated stimulus-free verification
Delivering static & formal's long-held promise of solving next-generation problems

Accelerating next generation electronic systems — Integrated — AI-infused — Secure — Intuitive — Cloud-connected

People

Process

Technology

Faster Engineers
Intuitive use
Instructive coaching
Integrated workflows

Fewer Workloads
Smart resourcing
Adaptive workflows
Analytic insights

Faster Engines
Automated scope reduction
Leading solvers
Unparalleled availability

All static & formal in integrated flows

Contextually aware

Static Assist AI

Formal Assist AI

Scalable Formal

Limitless Formal

Data driven — Connected — Scalable

Questa One SFV

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Questa One SFV's IVE delivers integrated and interconnected flows
Single entry point of Developer enables access to multitudes of analyses

Developer

Design Browser

Smart Editor

Integrated Analyses
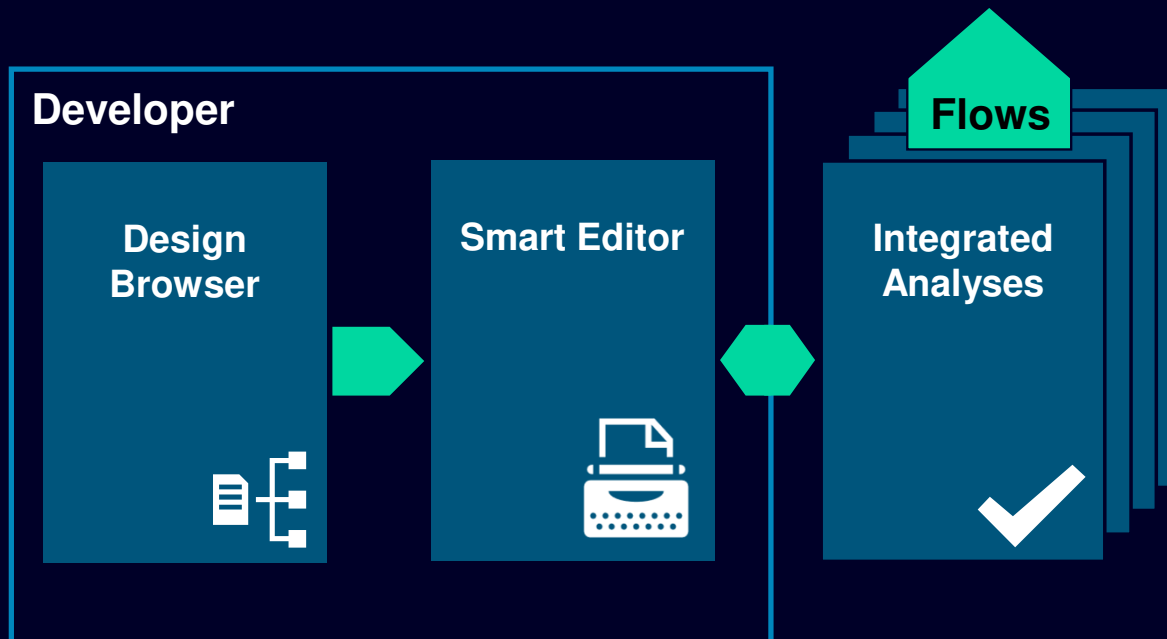
Flows

Design and project management

Smart editing

Seamless integration

Source navigation

Graphical visualization*

* target with 25.3 release

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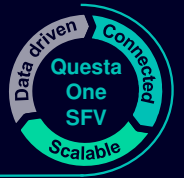
Questa One SFV delivers integrated and interconnected flows through IVE
Example: Lint Confirm: invoking formal linting to determine if Lint issues are real

How can I confirm the lint issue is real?

Syntax correct RTL

Lint issue list

Actionable Lint issue list

Smart editing On-the-fly linting

Lint analysis

Formal inspection (2025.3)

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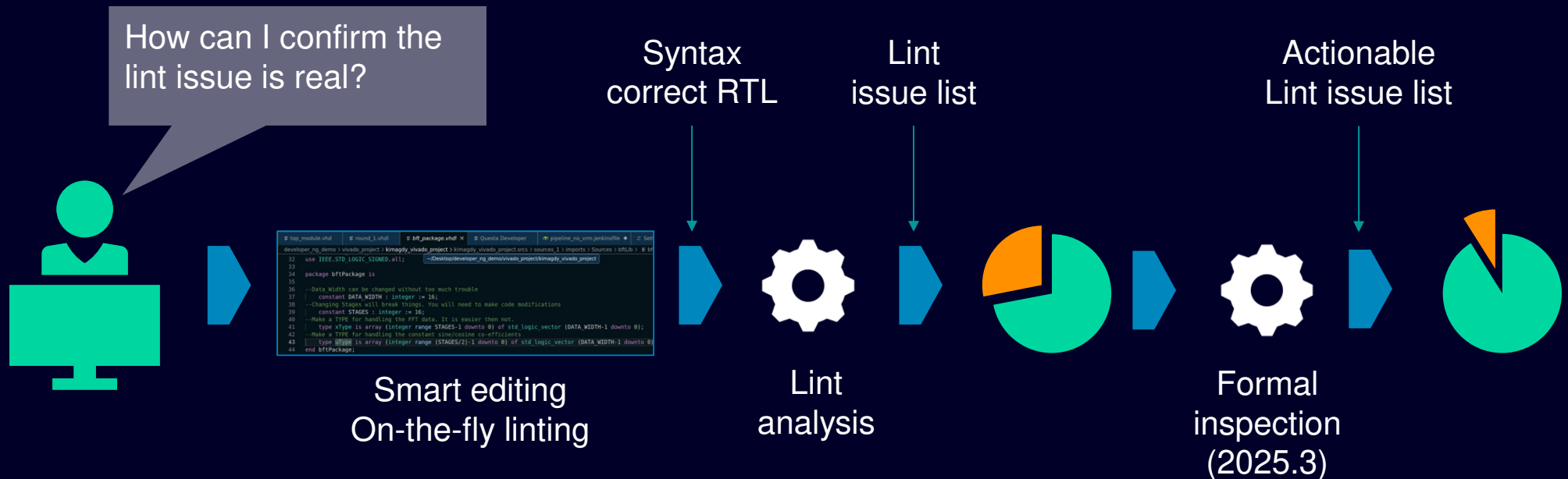
Questa One SFV's IVE delivers flexibility and control for developers
Comprehensive project management in development environments
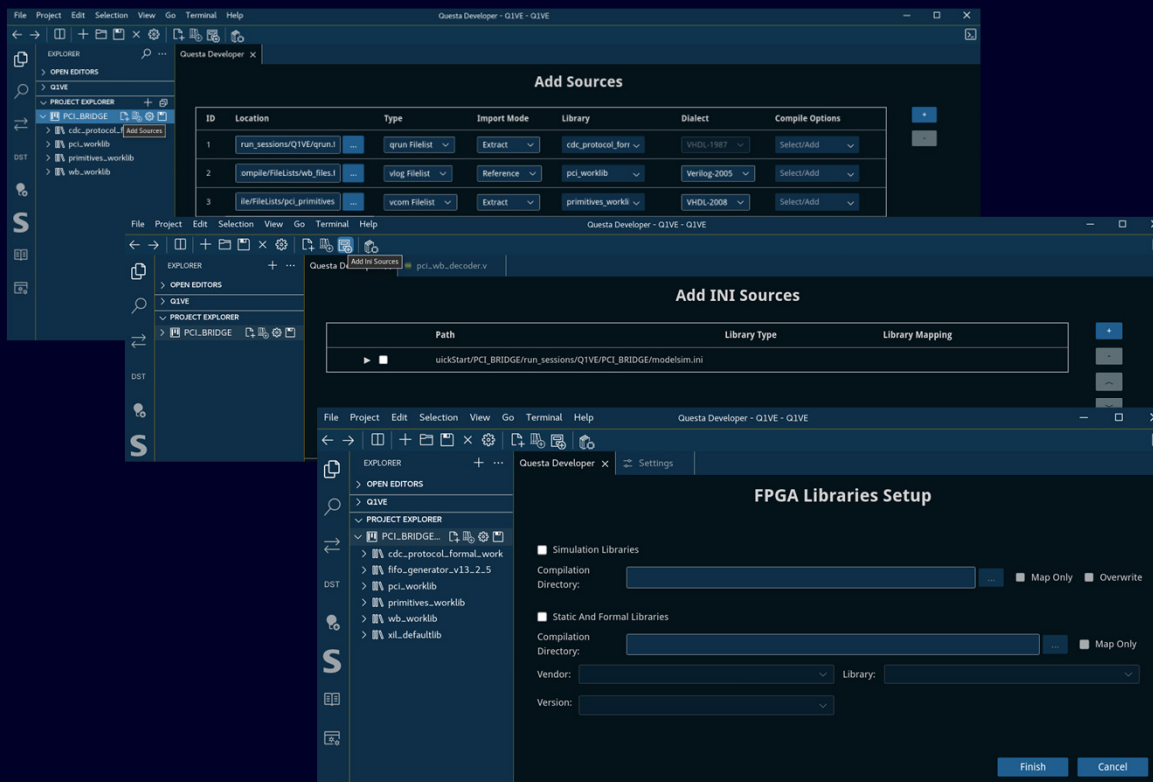
Design and project management

- Project creation and management

- Continuous enhancement

- Source management and SCM

- Flexible workflow and visualization

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Questa One SFV's IVE delivers enhanced code development features
Activates support for mixed language, real-time validation and advanced linting

Smart editing
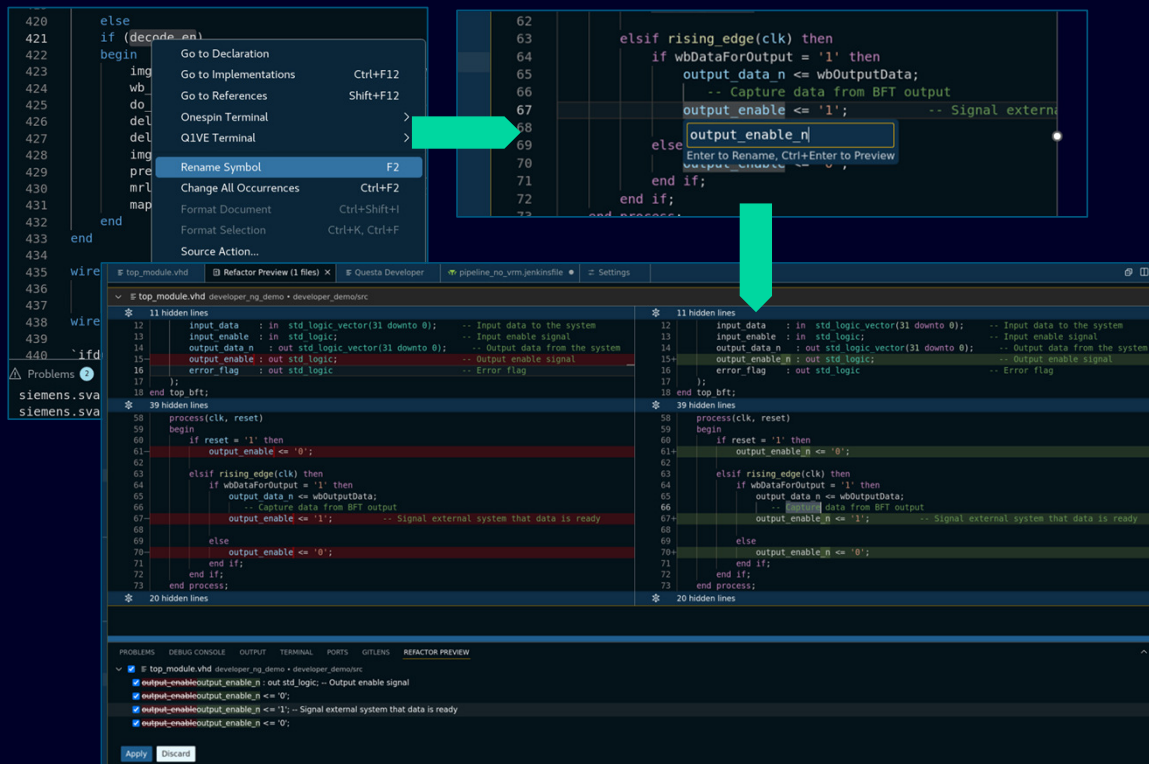
- Mixed language support

- Real-time syntax validation

- Code refactoring

- Advanced linting and auto-fixing

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Questa One SFV's IVE connects static and formal analyses
Seamless integration delivers a comprehensive verification environment

Seamless integration

- Lint integration

- Static solution integrations

- Formal solution integrations

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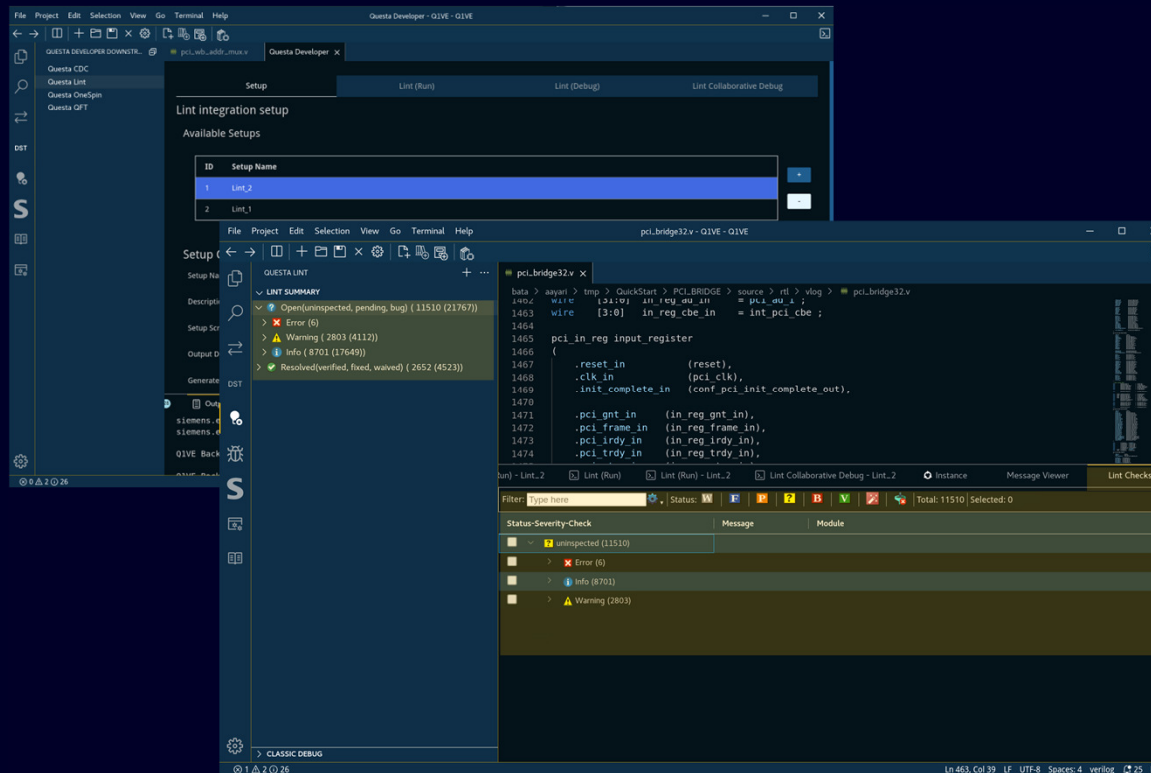
Questa One SFV's IVE enables code navigation and reference management
Streamlines access to code locations and modules
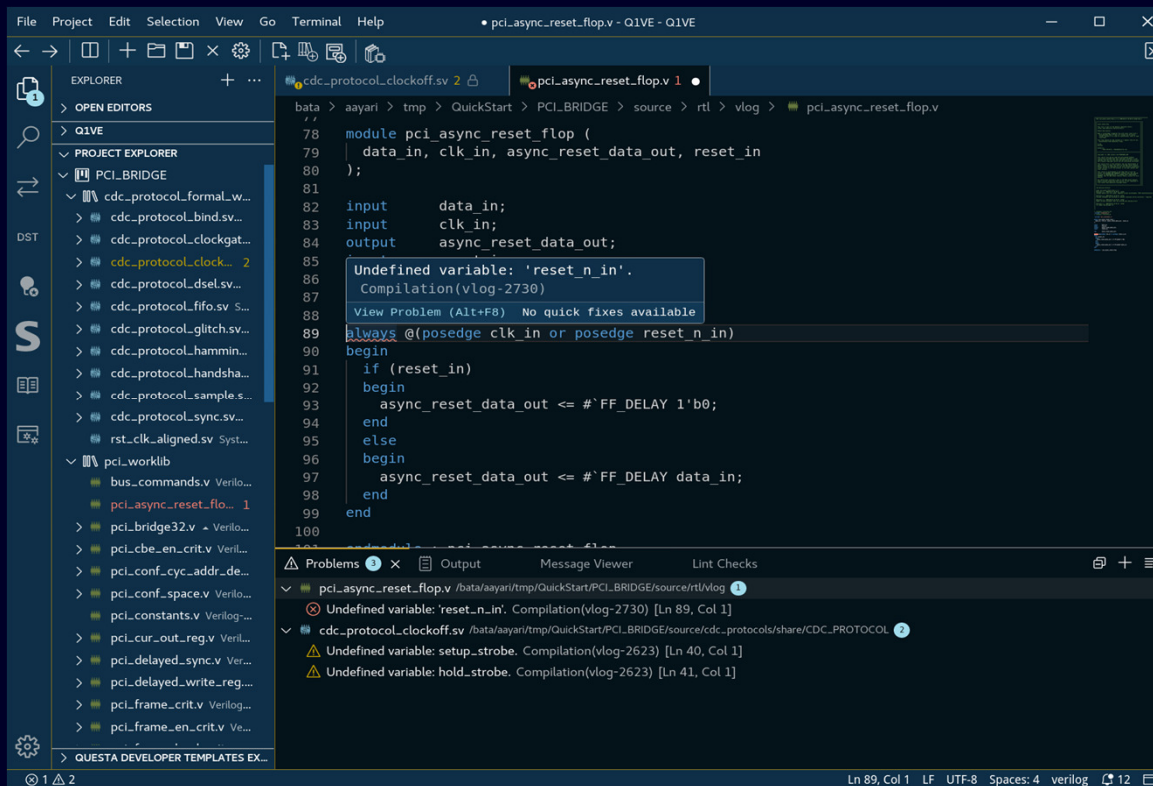
Source navigation

- Reference linking

- Message navigation

- State-machines and module access

- Declaration navigations

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Questa One SFV: Static Assist AI

Create and maintain a clean, efficient codebase and deliver high-quality RTL designs with ease

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Questa One SFV: Integrated stimulus-free verification
Delivering static & formal's long-held promise of solving next-generation problems

Accelerating next generation electronic systems — Intuitive — Integrated — AI-infused — Secure — Cloud-connected

People · Process · Technology

Faster Engineers
Intuitive use
Instructive coaching
Integrated workflows

Fewer Workloads
Smart resourcing
Adaptive workflows
Analytic insights

Faster Engines
Automated scope reduction
Leading solvers
Unparalleled availability

All static & formal in integrated flows

Contextually aware

Static Assist AI

Formal Assist AI

Scalable Formal

Limitless Formal

Questa One SFV — Data driven · Connected · Scalable

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Questa One Lint Assist AI: Productivity through static, formal, AI integration
Identify, auto-fix and verify changes in a single flow

How can I get clean code faster?

Known list of issues

Clean code

Clean equivalent code

Smart editing
On-the-fly linting
Automated full linting
Formal lint cross-check

Auto-fix
(or auto-waive)

Automated equivalence check
(2025.3)

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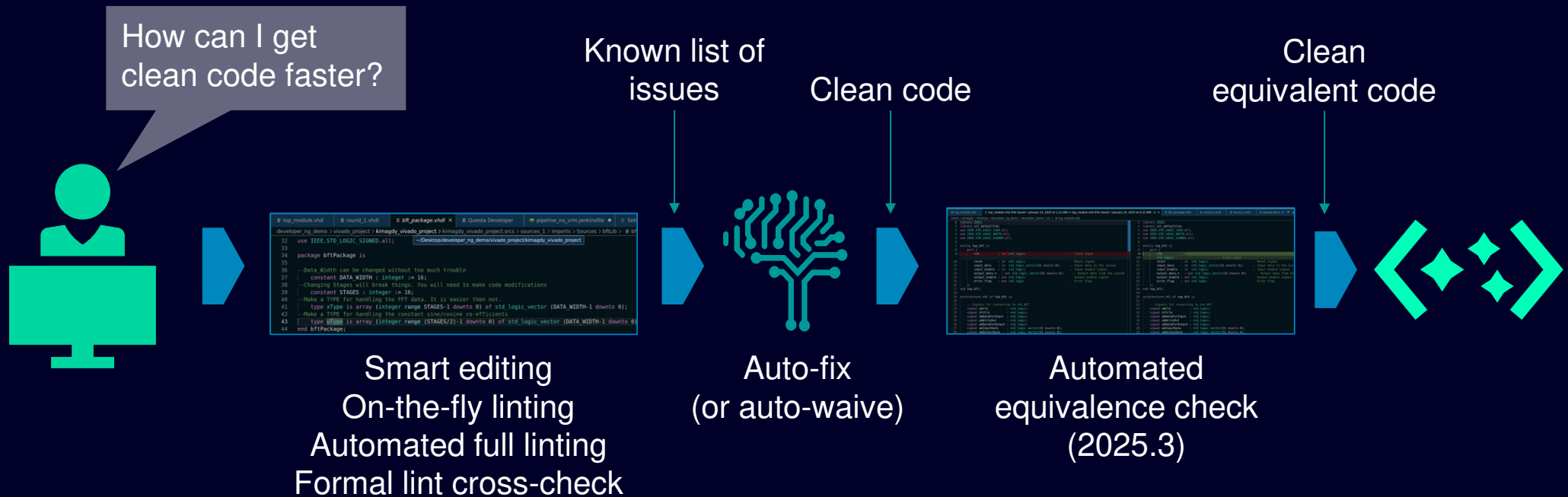
Lint Assist AI: high-productivity path to high-quality RTL designs
Integrated view of Lint issues with dedicated easily-accessible tab
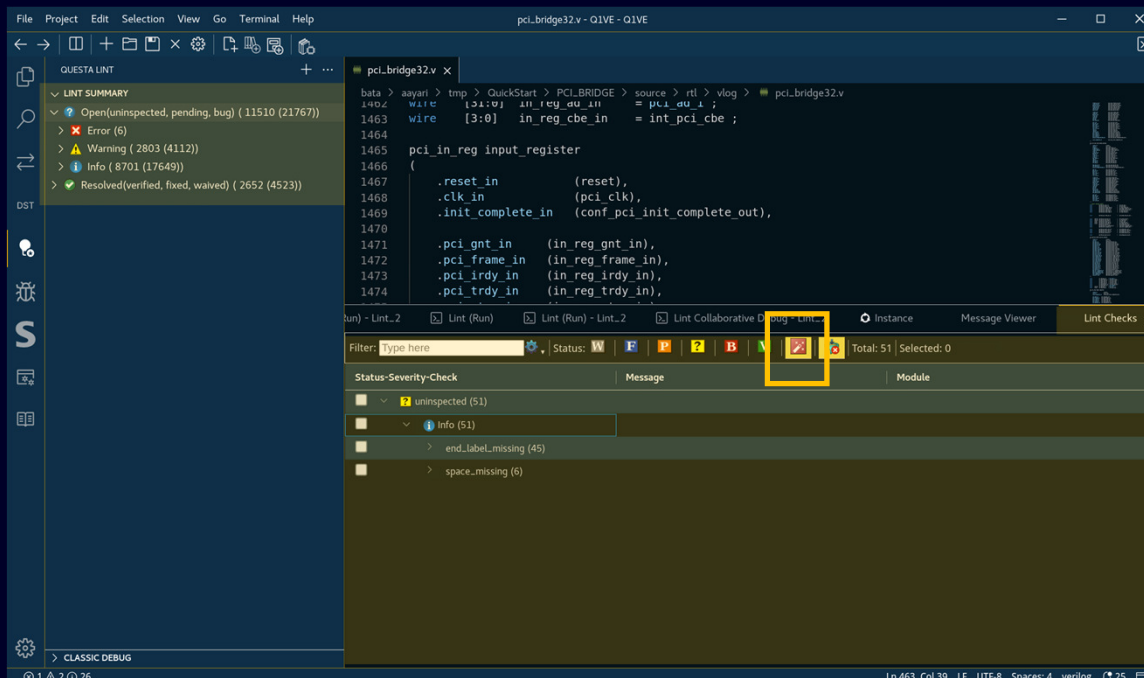
Run Lint analysis

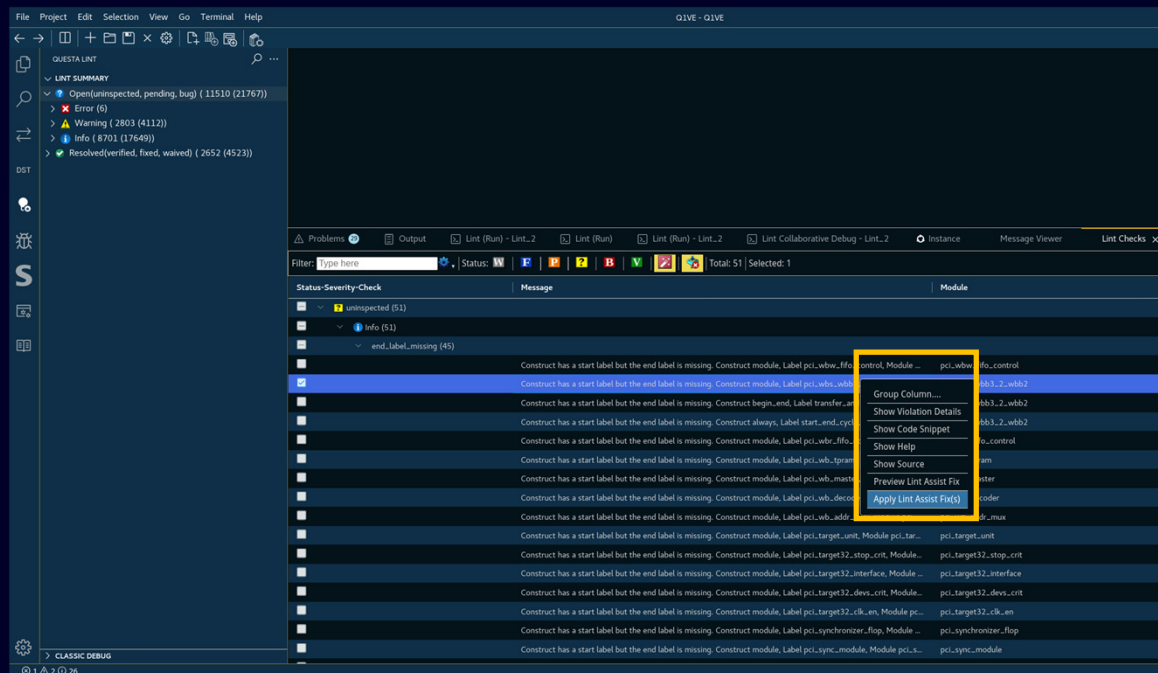Filter for auto fixable lint issues
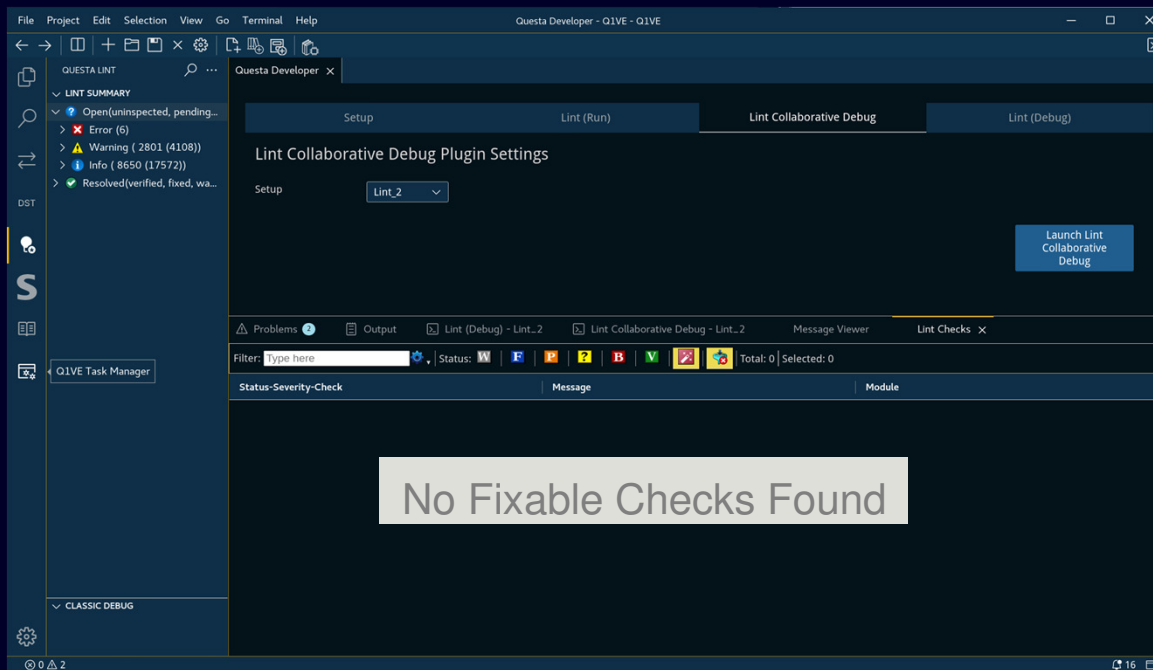
Preview suggested fix

Apply the fix

Re-run Lint

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Lint Assist AI: high-productivity path to high-quality RTL designs
Easily filter for auto-fixable lint issues

Run Lint analysis

Filter for auto fixable lint issues

Preview suggested fix

Apply the fix

Re-run Lint

SIEMENS
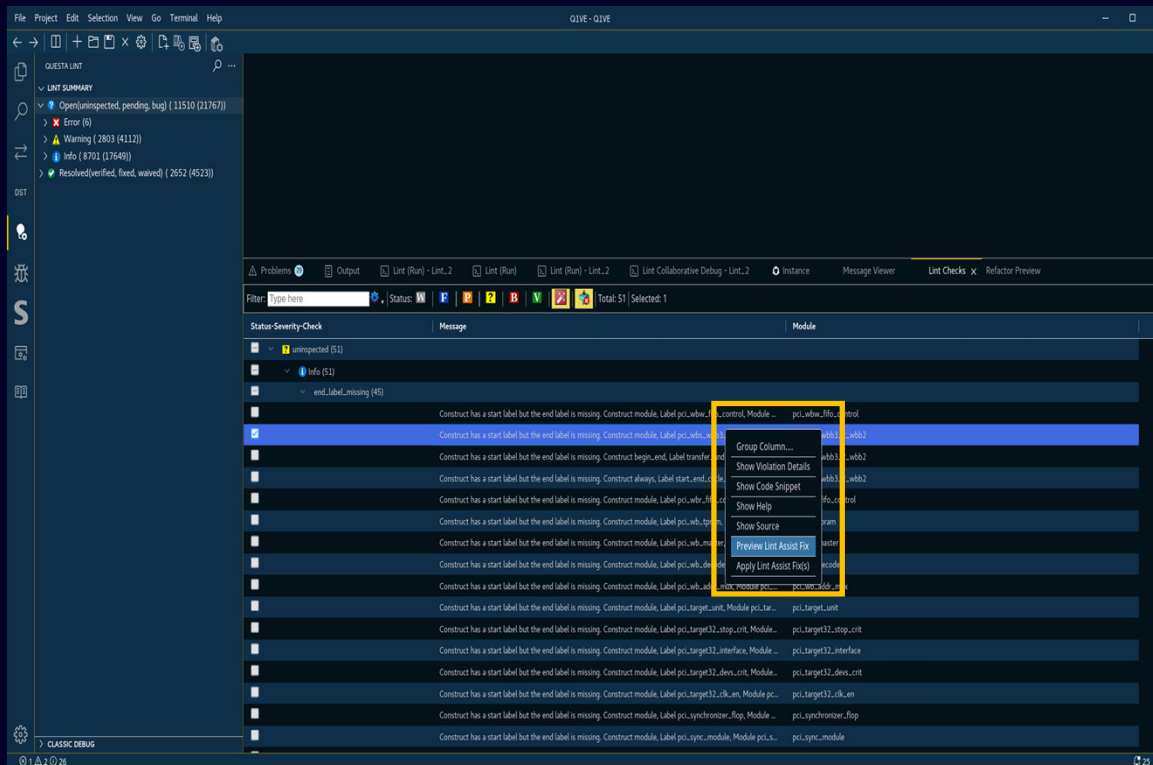
Lint Assist AI: high-productivity path to high-quality RTL designs
Suggested fix preview with side-by-side analysis enabled
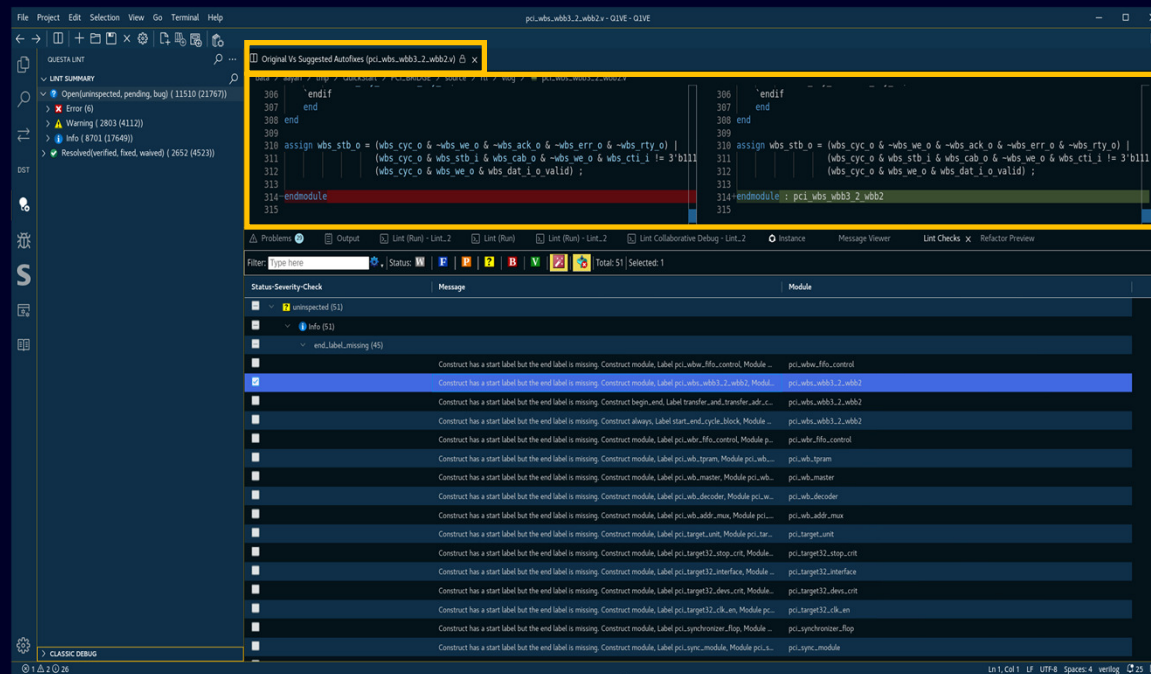
Run Lint analysis

Filter for auto fixable lint issues

Preview suggested fix

Apply the fix

Re-run Lint

SIEMENS

Lint Assist AI: high-productivity path to high-quality RTL designs
Easily filter for auto-fix lint checks and automated application with preview enabled

Run Lint analysis

Filter for auto fixable lint issues

Preview suggested fix

Apply the fix

Re-run Lint

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Lint Assist AI: high-productivity path to high-quality RTL designs
Re-run the lint setup with validation enabled with Equivalent RTL analysis
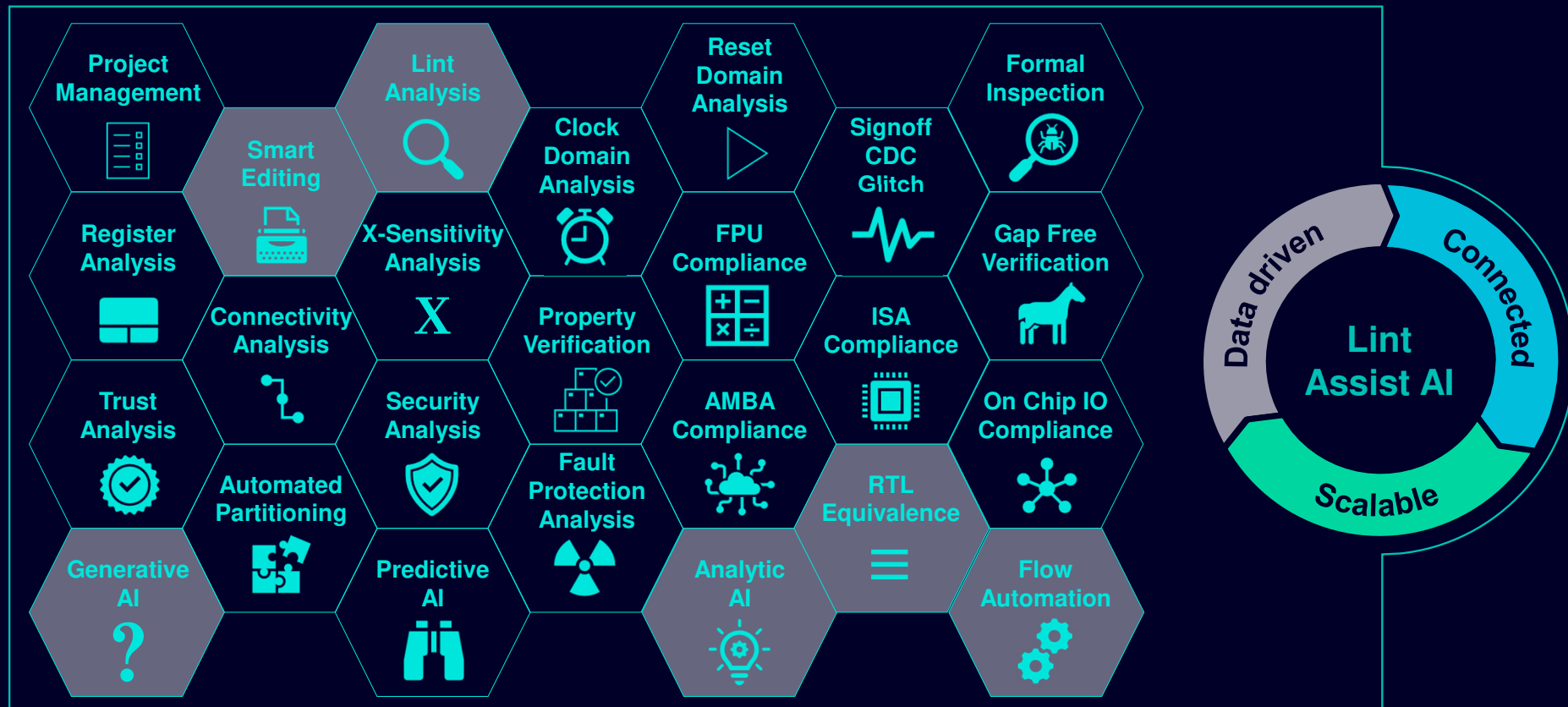

Run Lint analysis

Filter for auto fixable lint issues

Preview suggested fix
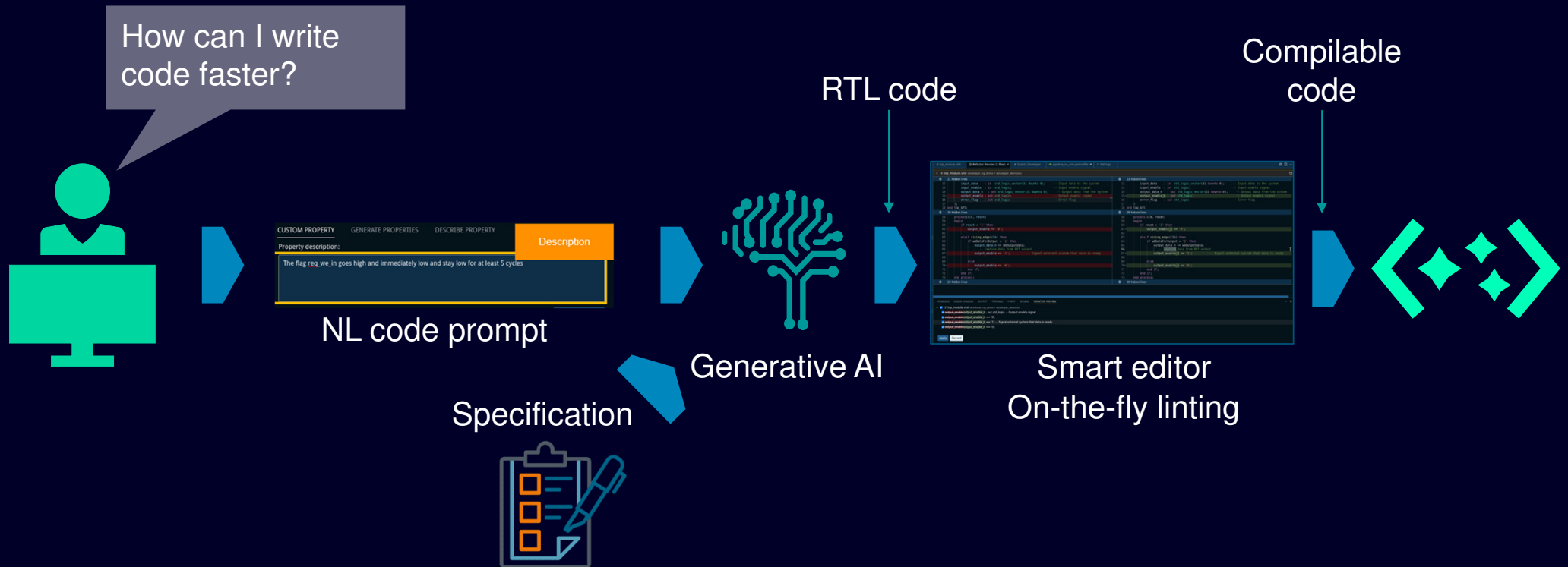
Apply the fix

Re-run Lint

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Questa One Lint Assist AI: example of synergistic integration
Building a flow from discrete analyses to solve issues is new ways

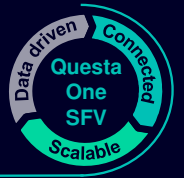Restricted | © Siemens 2025 | Siemens Digital Industries Software

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Questa One Code Assist AI: Fast path to code through Generative AI
## Create code and lint in a single, iterative flow in one environment

How can I write code faster?

NL code prompt

Specification

Generative AI

RTL code

Smart editor
On-the-fly linting

Compilable code

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AI-driven code development with Questa One SFV
Code Assist AI empowers code generation, optimization and verification

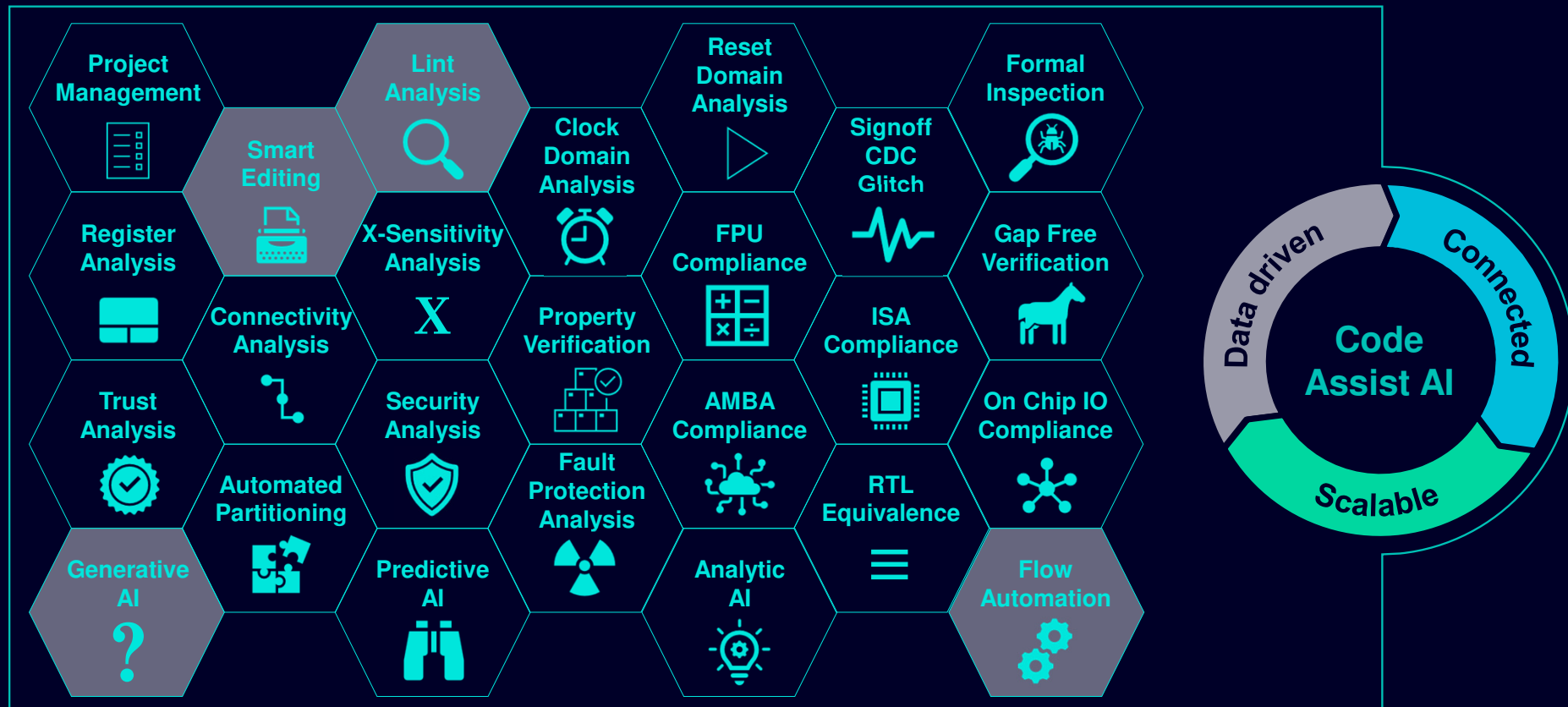**Questa Developer Smart Editor**

Code Assist AI*

* target with 25.3 release

Flows

Integrated Analyses
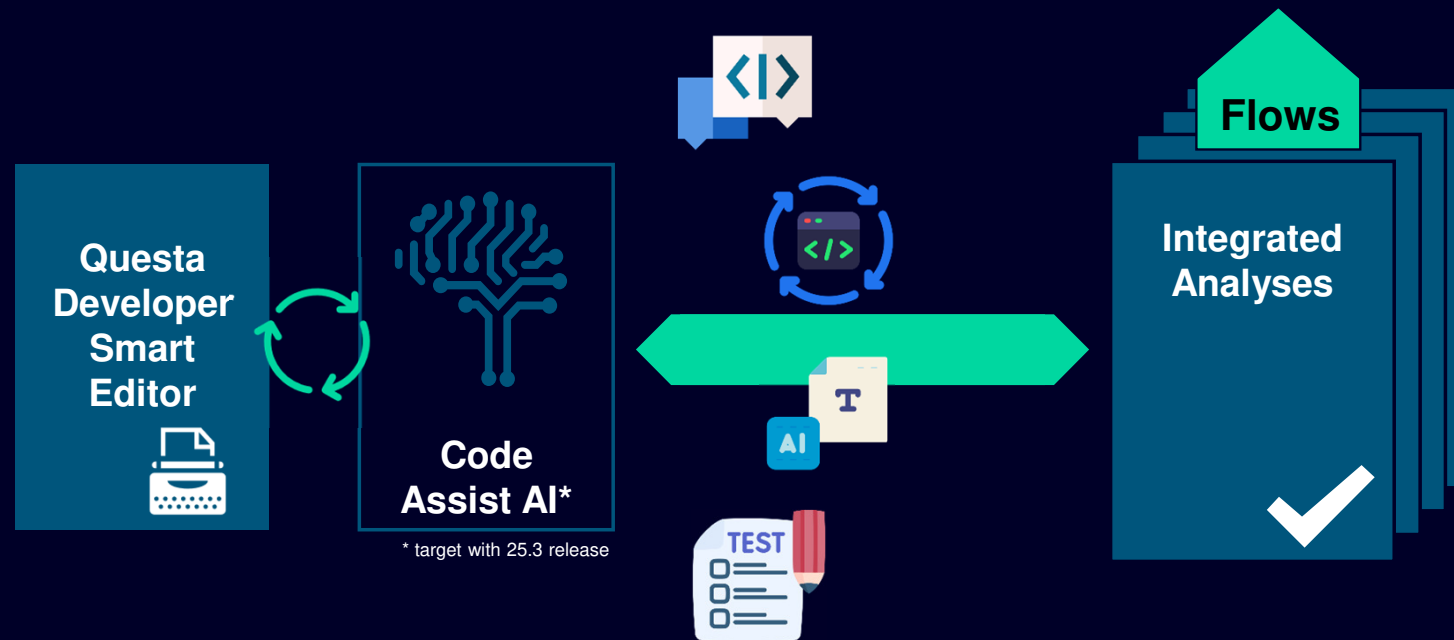
| **Automate** | **Optimize** | **Refactor** | **Correct** |

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Questa One Code Assist AI: example of synergistic integration
Building a flow from discrete analyses to solve issues is new ways

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Summary

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Questa One SFV delivers total user and team productivity
Transforming verification through static & formal integration with AI

Today's silicon development faces substantial headwinds
- Investing more in traditional verification methods is a demonstrated failure

The convergence of AI and static and formal technologies promises a next-gen solution
- Modern deployment of static & formal has marginalized its value

Questa One SFV uniquely delivers a solution purpose-built for next-generation problems
- Full utilization and availability with unlimited AI integration and automation is transformative

Questa One SFV is a transformative approach to verification that uniquely enables success amidst today's challenges

How can Siemens help you succeed?

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