SYNOPSYS®

The Era of Agentic Engineering

Verification Futures

1 July 2025

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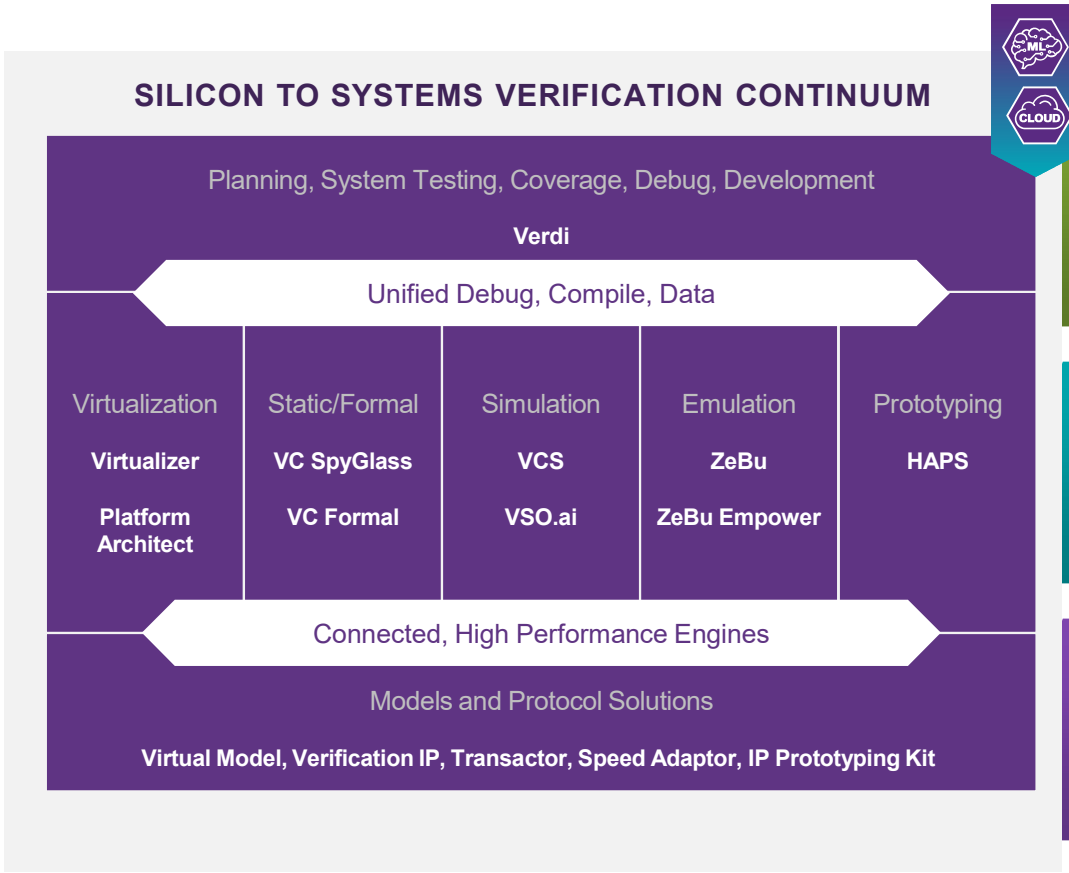
Synopsys Silicon to Systems Verification Continuum



Industry Leading Engines

Validate entire SoC with best server utilization & throughput

Fastest emulation for earlier SW bring-up

Pervasive Intelligence

Accelerating Coverage Closure

10X faster TAT w. Formal/Static tech

Next Gen Verdi Debug Productivity

Unified Platform

Transition seamlessly b/w simulation, emulation, & prototyping environment

Unified debug with Verdi

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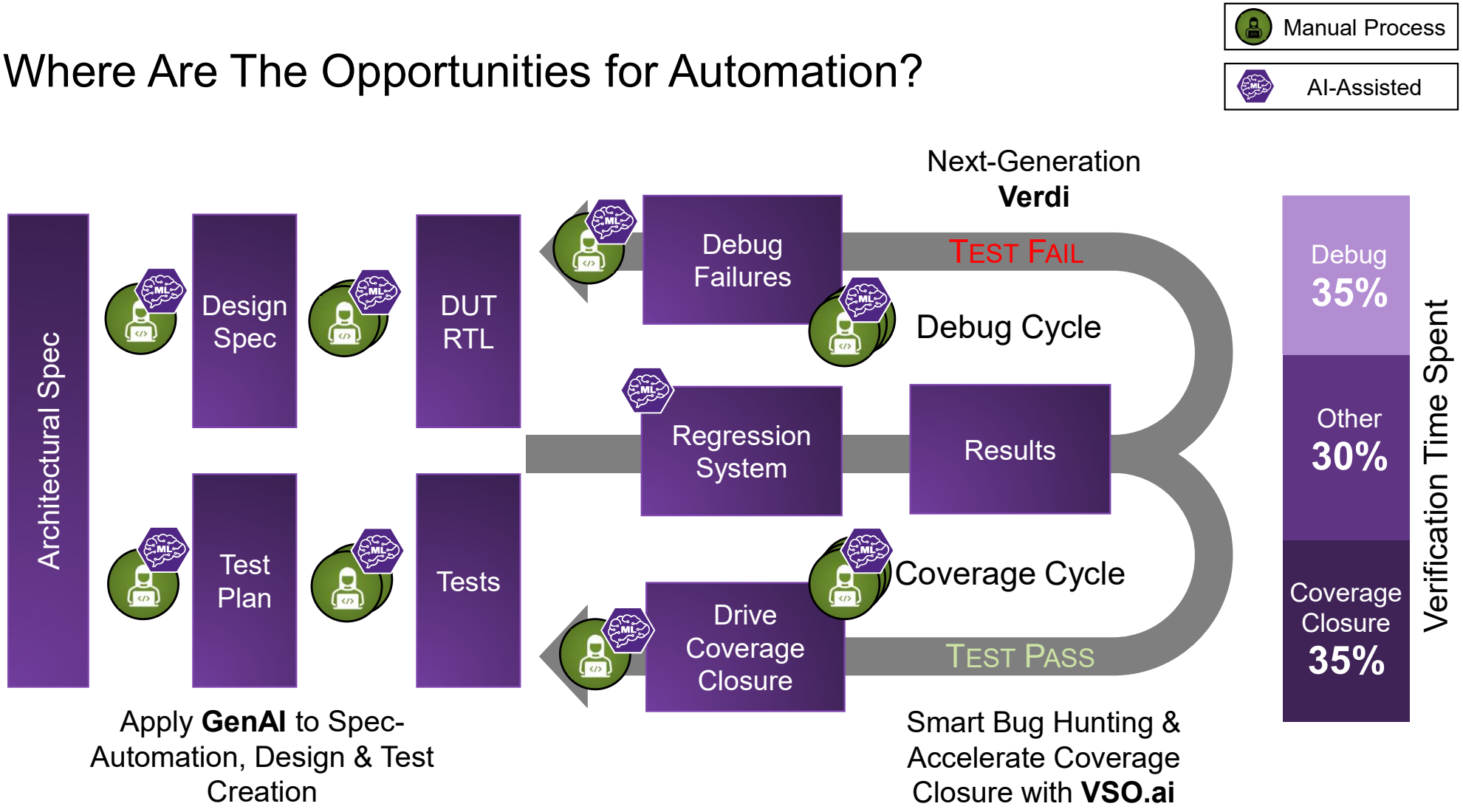
Where Are The Opportunities for Automation?



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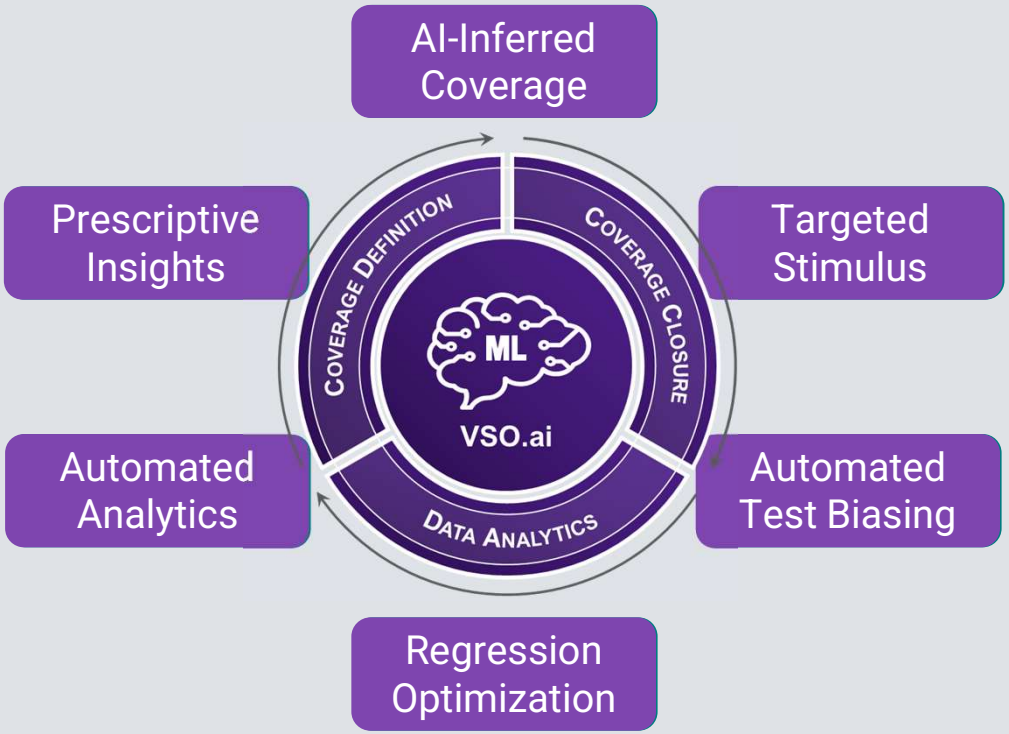
AI Driven Verification Space Optimization - VSO.ai

Faster, Higher Coverage Closure & Analytics



Better Coverage: *Coverage Inference Engine Helps to Define Coverage from Stimulus and RTL*

Productivity Boost: *Connectivity Engines & ML-Based Solver Target Hard to Hit Coverage*

Improved HW Utilization: *Regression Optimizer Ensures Highest ROI Tests Run First*

Higher Resource Efficiency: *Advanced Root Cause Analysis to Identify Unreachable Coverage*

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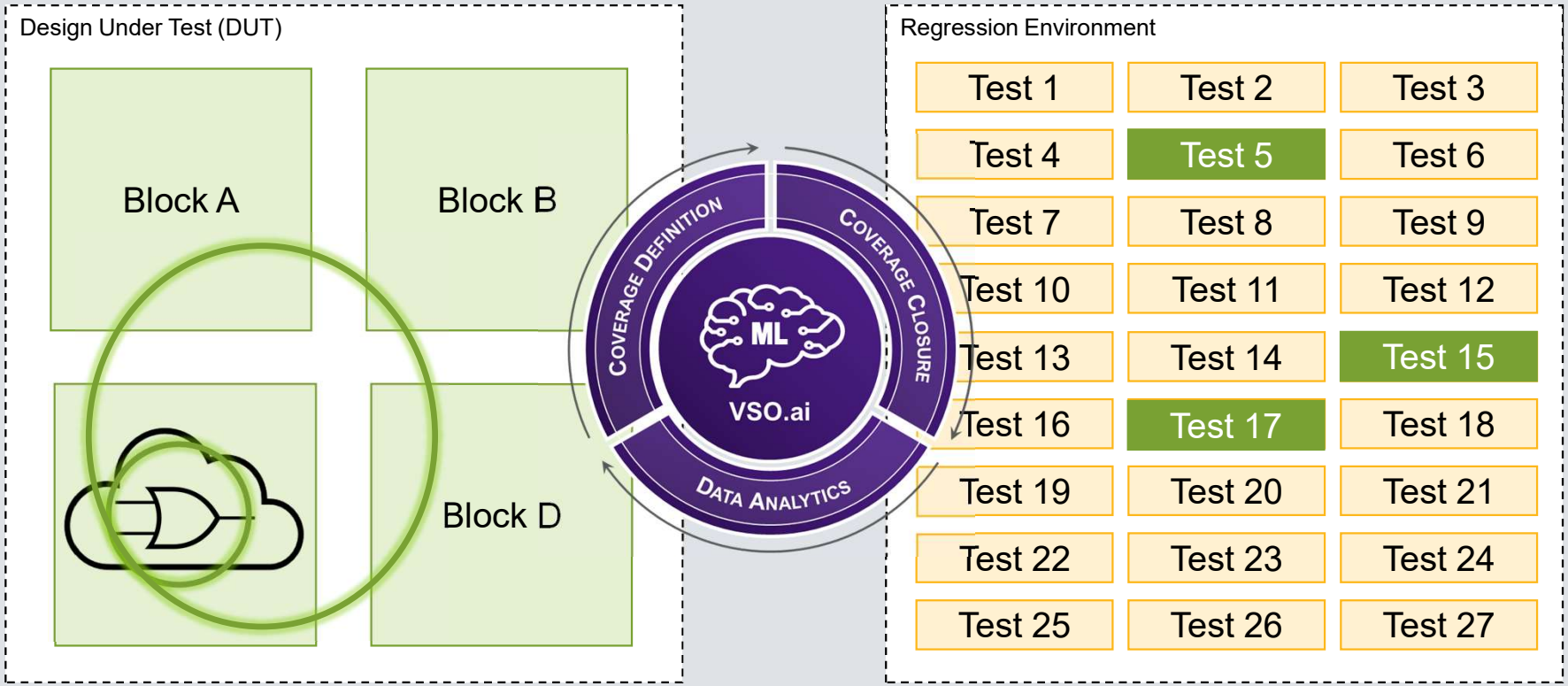
VSO.ai Change-Based Verification

Focus Regressions Only on Changes



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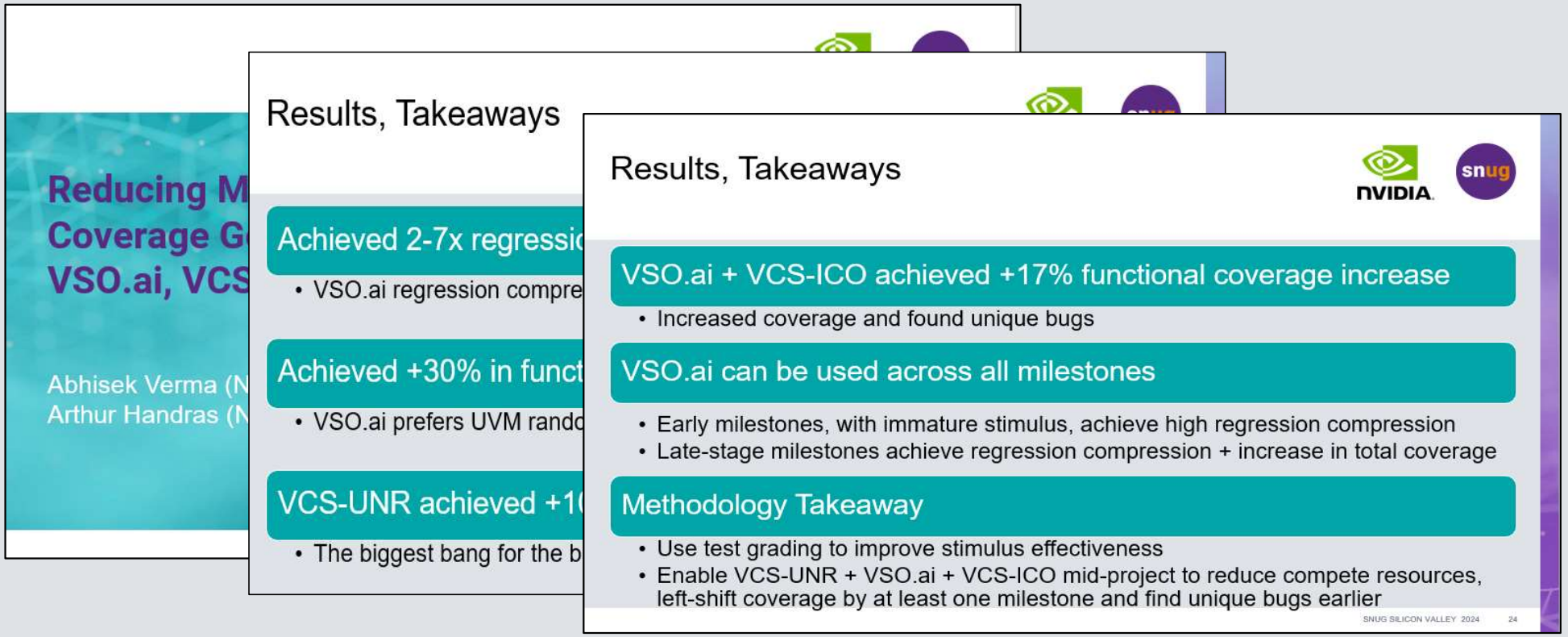
NVIDIA at SNUG SV 2024

Top-10 Best Presentation Award



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VSO.ai: Next Wave of Customer Successes

Faster Closure with Better Coverage

20%
Higher
Coverage
2X TAT

GPU

Mobile

11%
Higher
Coverage
3X TAT

6X
Faster
Coverage
Closure

Handset

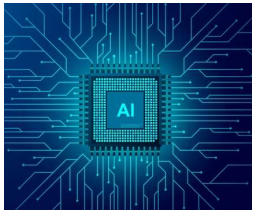
Cloud HW

3.7X TAT
5%
Coverage
Boost

1.8X TAT
4%
Higher
Coverage

Optical Semi

2.1X TAT
2%
Coverage
Boost



AI Chip

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Synopsys.ai : GenAI Vision and Applications for Chip Design

Assistive

Expert Guidance on Tools and Flows

Knowledge Assistant

Workflow Assistant

Run Assistant

Creative

Design Collateral Creation, Optimization

RTL Assistant

Verification Assistant

Agentic

Workflow Automation

Execution of simple to complex multi-step tasks

On-Prem / Cloud Enabled Optionality; Commercial and OSS LLM Supported

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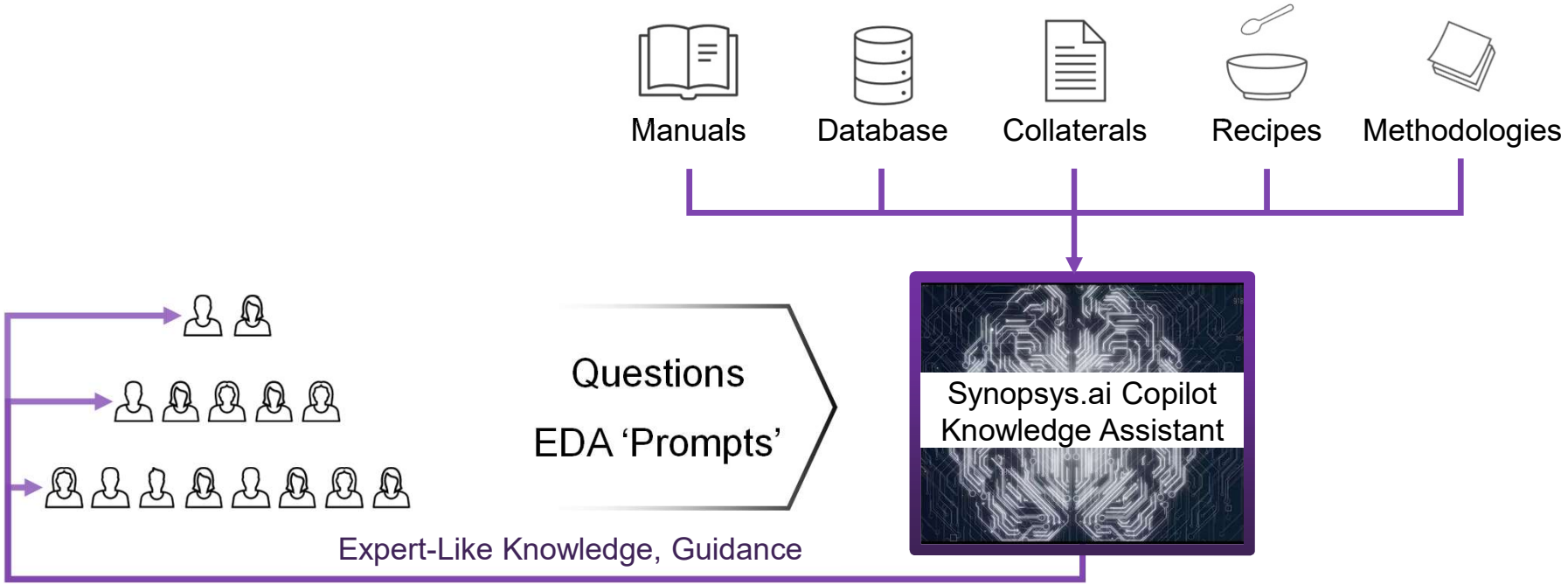
GenAI Assistants : Expert-Level Guidance, Faster Ramp



30% Faster Ramp Time For Engineers

25% Faster Closure of Tickets

2X Faster Response vs. Search Queries

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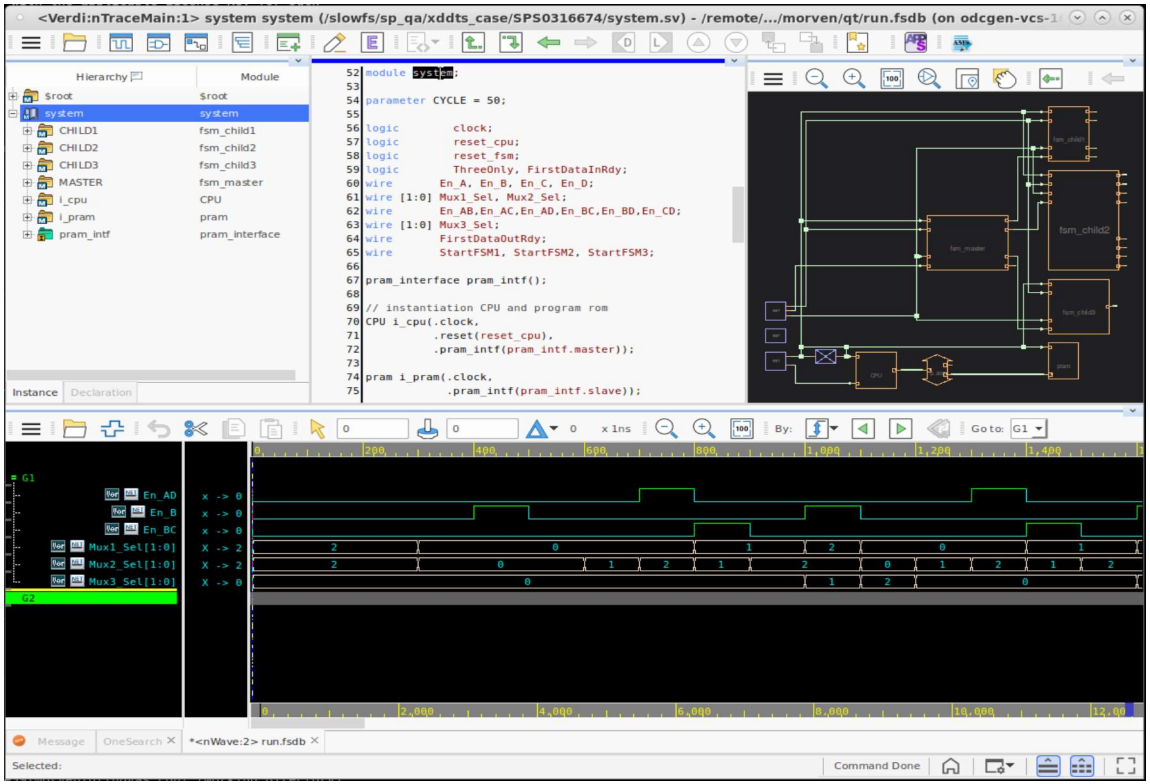
Opportunity for Conversational Debug

"Who checked in the latest RTL for module PCIe?"

"Why is the reset signal "X"?"

"Show me all the input signals to module IRQ"



"Give me all the registers impacted by signal REQ"

"How did I debug this issue last time?

"Which transaction caused the failure?"

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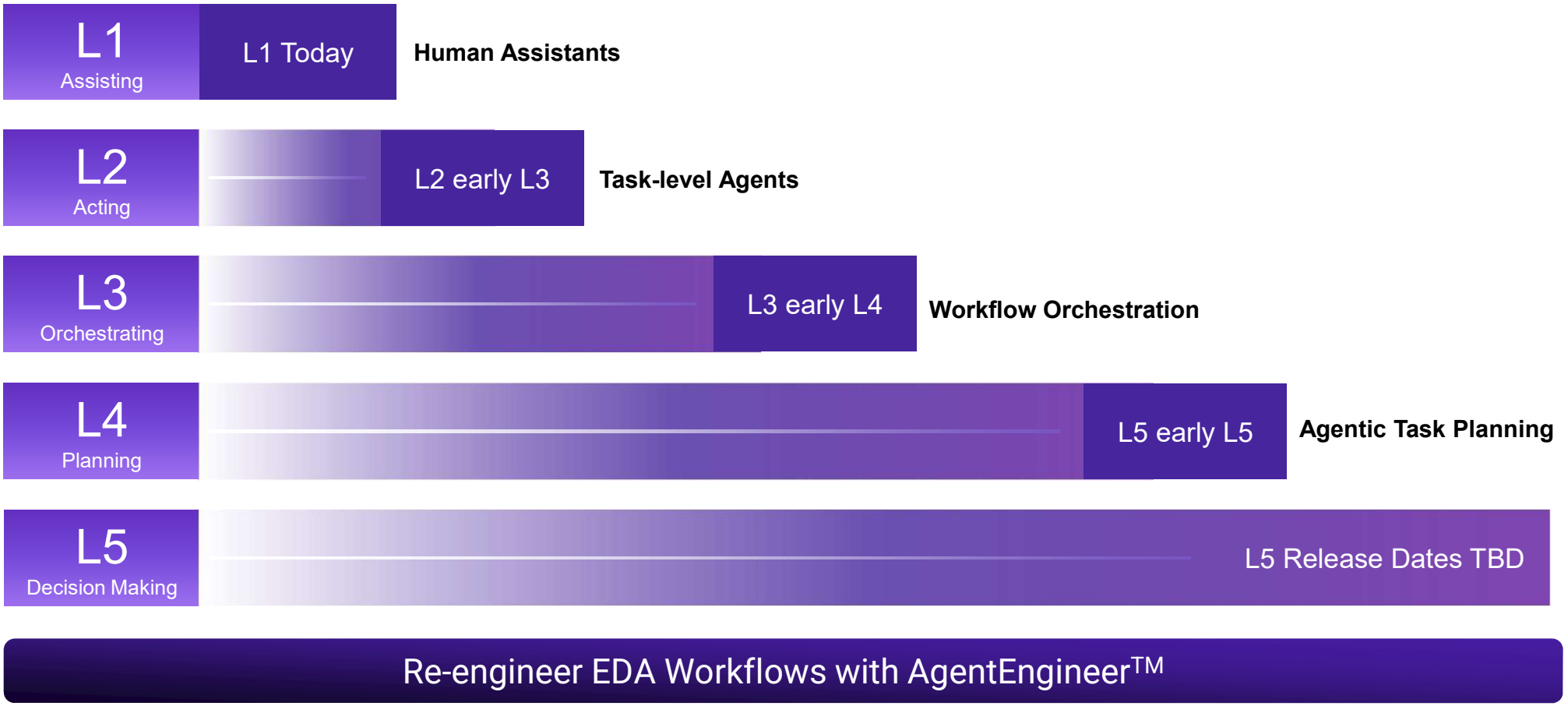
Vision for Agentic AI – From Copilot to Autopilot



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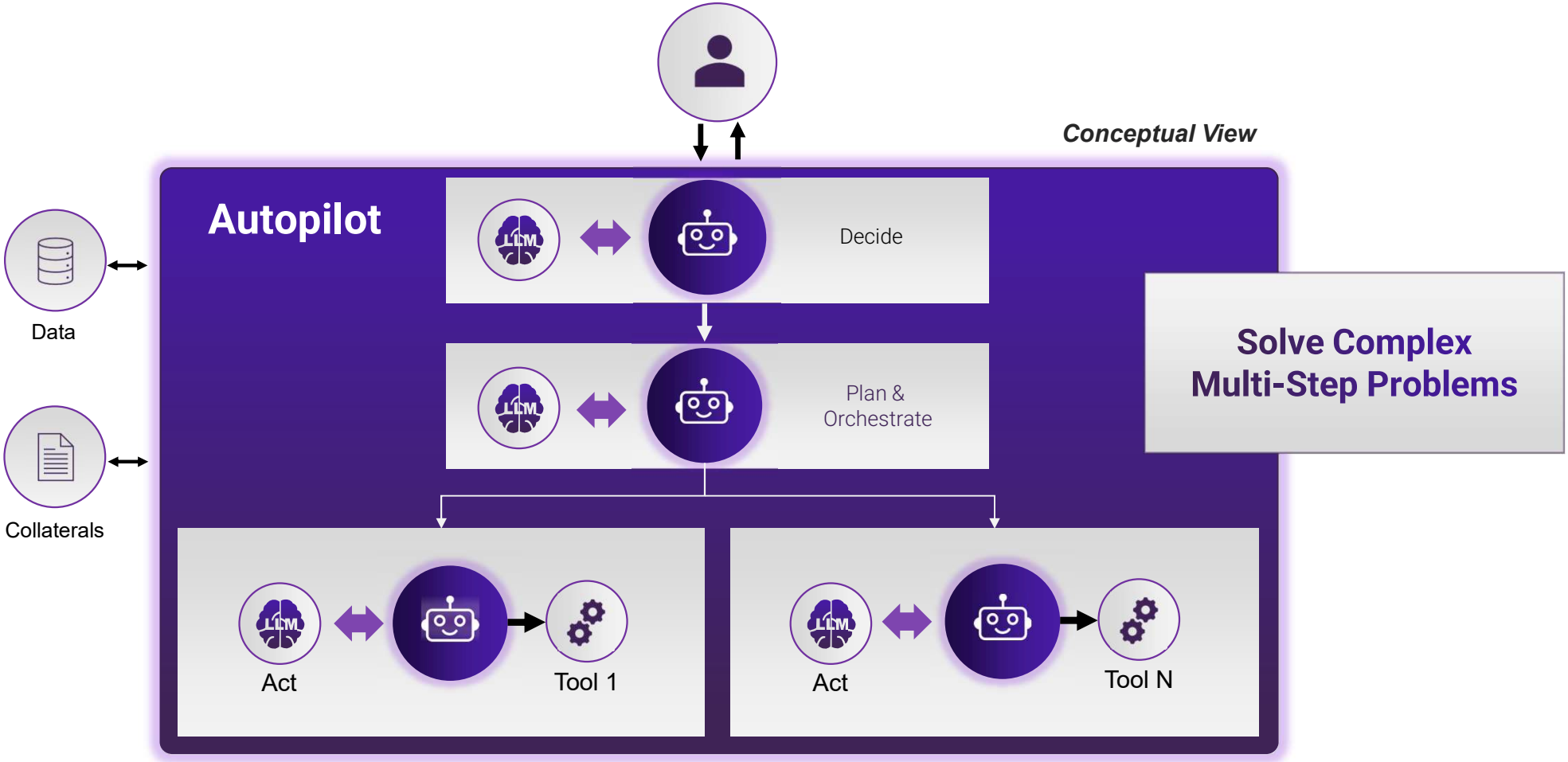
Agentic AI: Vision for LLM-Powered Multi-Agent EDA Framework



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