Unlock Silicon Flexibility

Design for the Future with Programmable Platforms

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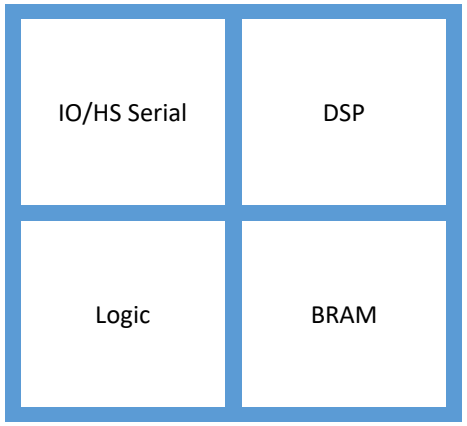
VP Sales

Current Programmable Logic Options

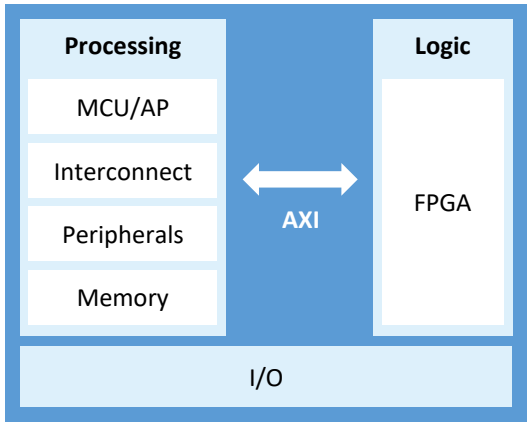
Generic FPGA Family

(Cyclone® x/MAX® x, Spartan™, Virtex™, pASIC®)



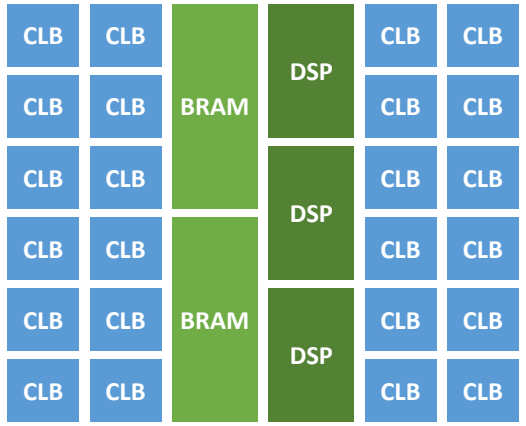
Programmable SoC

(Zynq™, Agilex™, EOS™...)



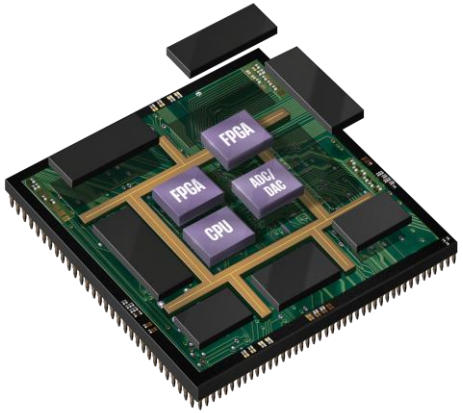
eFPGA IP

(Soft or Hard IP)



FPGA Chiplet

(Build to your requirement)



FPGA & Programmable SoC

FPGA families are becoming **tailored towards specific applications**

- Movement **from general-purpose logic to application-specific functions**
- Features are being added for areas **like AI inference, Automotive, Networking, 5G support, reconfigurable Hardware Acceleration**, and power optimization

This trend **affects size/density and cost**

- FPGAs are moving away from being commodity logic devices
- The **minimum feature and cost entry points are moving up**

Vendors are concentrating on specific areas

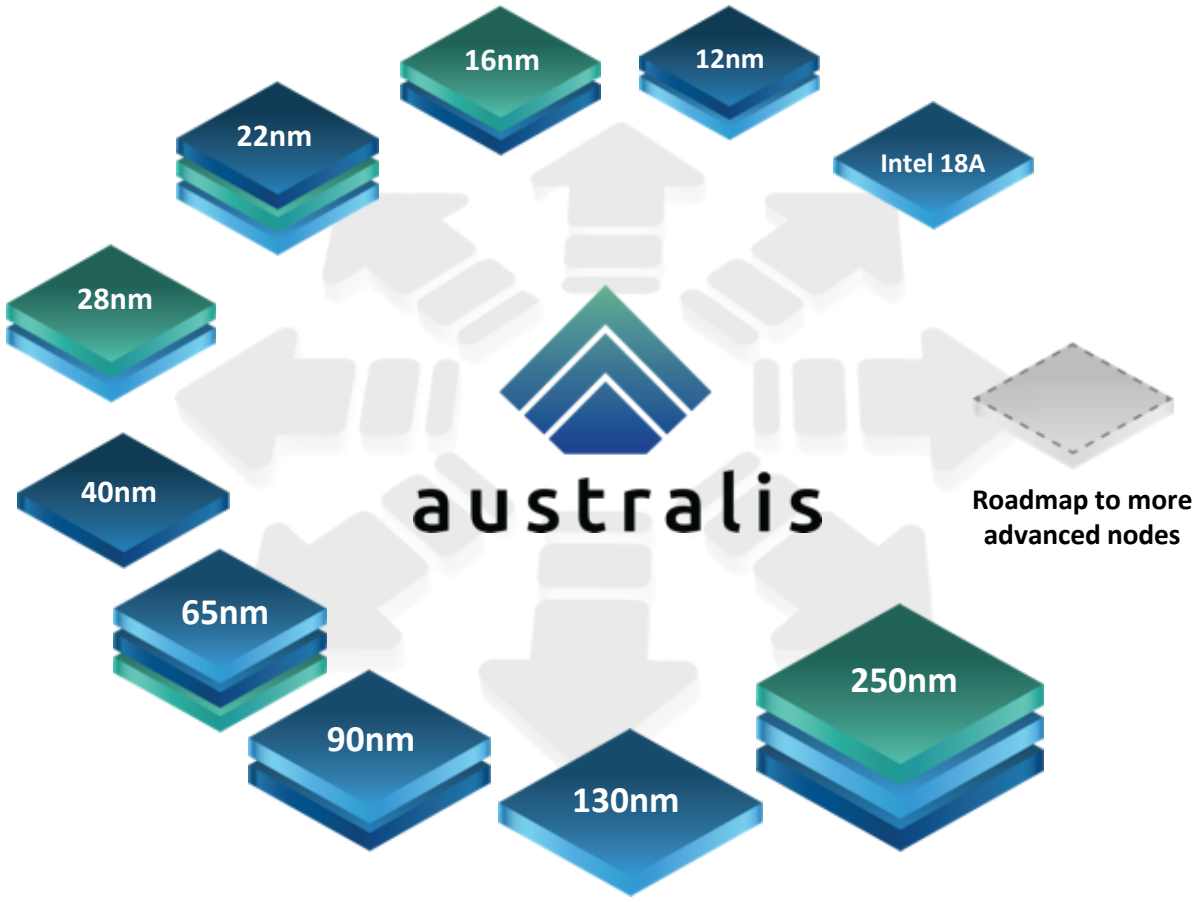
- **Low power & IoT edge, Military/Aerospace, and Data centers/5G/ Networking**

FPGA & Programmable SoC Trade off

Feature	FPGA	Programmable SoC
 **Logic Flexibility**	Full control of logic implementation	Fixed architecture, CPU + FPGA introduce limitations
 **Latency**	Low latency, better for real time & deterministic systems	Fixed architecture may add additional layers & increase latency
 **HW Acceleration/Parallel Processing**	More FPGA size options, enables greater parallelism and scalability	Limited by CPU & FPGA size & architecture, not as scalable.
 **Cost**	More reasonable	Potentially very high
 **Application match**	Integration and verification rely on vendor-specific wizards/tools and IP.	Dedicated features cut verification time and effort

As top FPGA suppliers move up in entry point, gap will be filled with new entrants & SoCs with embedded eFPGA

eFPGA: Embedded FPGA – Customize your SoC



eFPGA Ports to All Process Nodes/Foundries

- Easy-to integrate eFPGA using standard cell libraries (Hard or Soft IP versions)
- Scalable from commercial to automotive to rad hard designs with customizable features
- Support for different process nodes, VTs, transistor options, highly portable

GlobalFoundries™ Honeywell intel foundry SAMSUNG skywater tsmc UMC

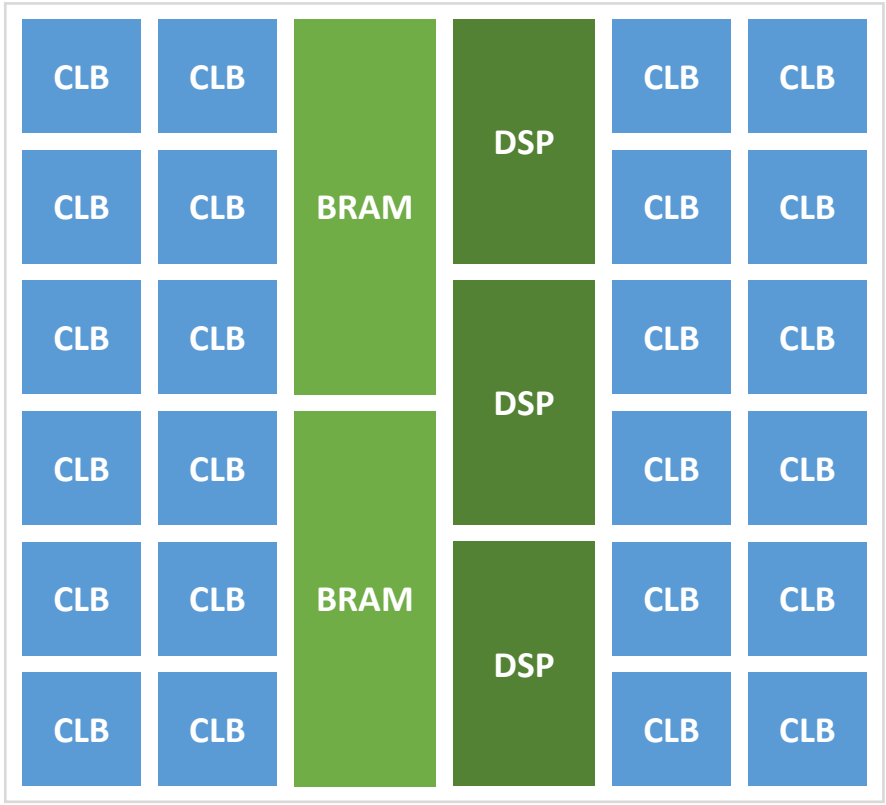
Customize your eFPGA IP Solution

Deliver efficient, reliable, and scalable reprogrammable logic

BENEFITS

Tightly couple your FPGA needs in your own SoC

- Define exact architecture and features
- Improve processing performance (customizable HW acceleration)
- Reduce system power
- Custom boot/Fast boot definable
- Choose FPGA technology, (SRAM, RERAM, MRAM, FLASH)
- Reduce system cost for volume applications
- Adding flexibility into an expensive SoC can increase device longevity



eFPGA Hard IP vs Soft IP

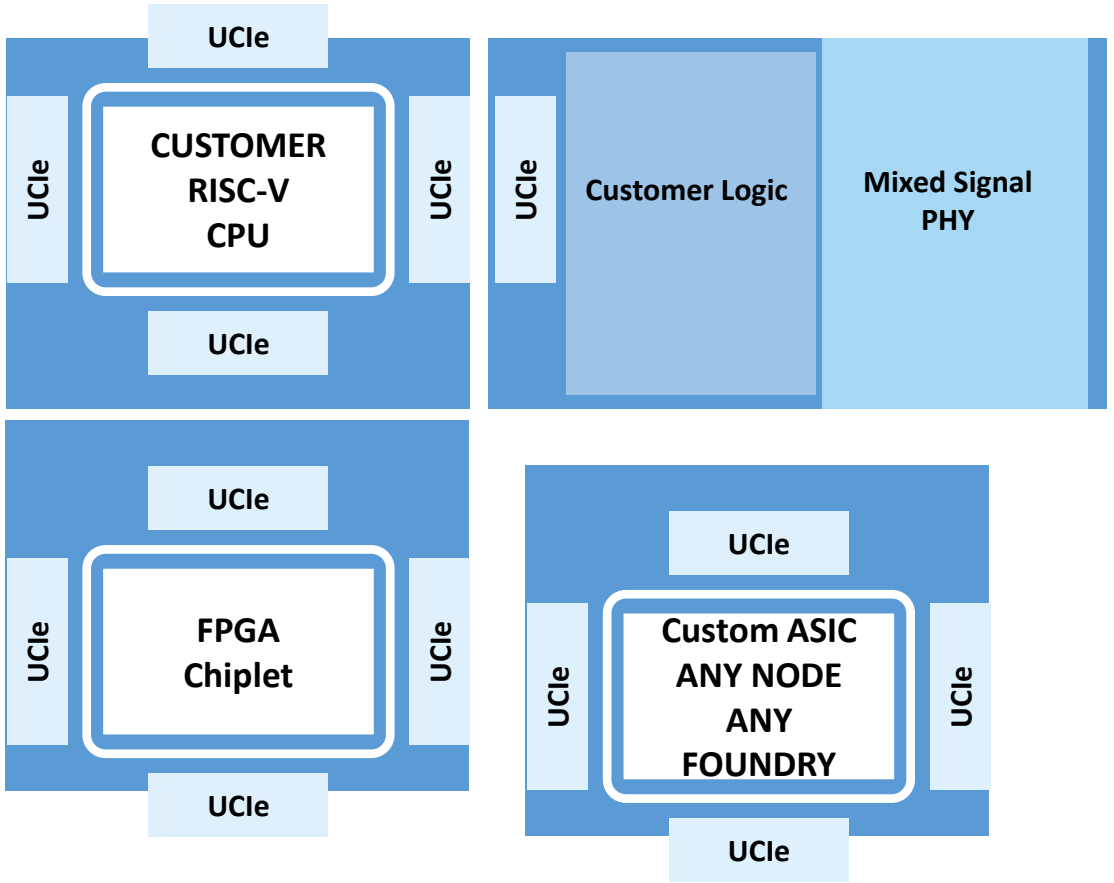
Feature	eFPGA Hard IP	eFPGA Soft IP
Portability	Fixed to a process node	Portable, (multiple uses) process independent
Format Delivered	GDSII database	RTL (Verilog/VHDL)
Integration Effort	Relatively low, plug and play!	High (careful P&R for timing closure)
Time-to-Market	Short (GDSII sign off)	Long (gain accurate, predictable timing)
Silicon Area	Larger than FPGA (less optimized)	Larger than FPGA (less optimized)
Timing & Power	Identified later in the design process	Identified later in the design process
Cost	Marginally higher than soft IP (less backend work)	Initial IP cost is lower, but additional work on P & R still required

FPGA Chiplet – The Ultimate Pick & Mix

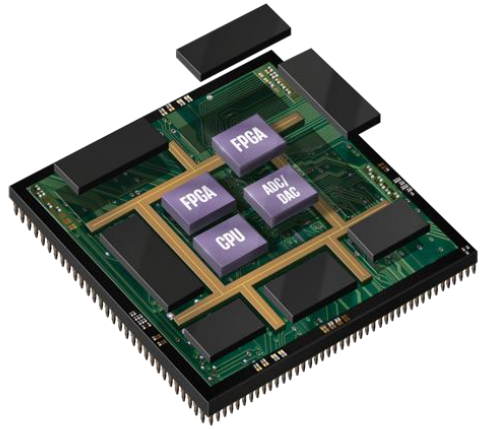
Chiplet Library

- eFPGA Chiplet
- PCIe Gen x
- Ethernet
- CPU
- Memory
- Analog
- Peripherals

Customer Chiplet (LVDS, BoW, UCI-e)



Final ASIC Multiple Chiplets



Chiplet Features

Feature	Chiplet
Connectivity	**LVDS, BoW, UCI-e** (Standard/Advanced/3D) Choice driven by **cost/performance/latency/package options/availability**
Interoperability	Complex, Interoperability not guaranteed even with same standard (early days and few chiplets on the market to test). UCI-e IP availability on lower geometries limiting
Scalability	High. Define **architecture, spin derivatives** quickly
Cost	Spin derivatives at low cost (**low Packaging NRE**). Unit cost higher due to complex packaging and test
Process Node	**Independent**, utilize best chiplets from best nodes
Package & Test	More complex and costly (2.5D & 3D packaging), Die 2 Die timing, DFT, verification & power delivery complex Complex pre & post package testing Complex interconnect testing Multi die waste with yield risk (one faulty die wastes multi die) Package cost can exceed multi die cost ($10-$20) can limit end application
Time to market	**Months to new SoC**, not years
Tool Chain	EDA tools not optimized for multi die designs
Future Outlook	**Chiplets are Inevitable**. Due to advanced node costs and difficulty integrating features (precision analog etc.). EO 2026 for wider availability.

QuickLogic Complete Programmable Logic Solutions

- **35+ Years of FPGA Experience**
- **NASDAQ listed in 1999 - QUIK**
- **Headquartered in San Jose, CA**
- **ISO-9001 Certified**

For more information, please contact
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Thank you!