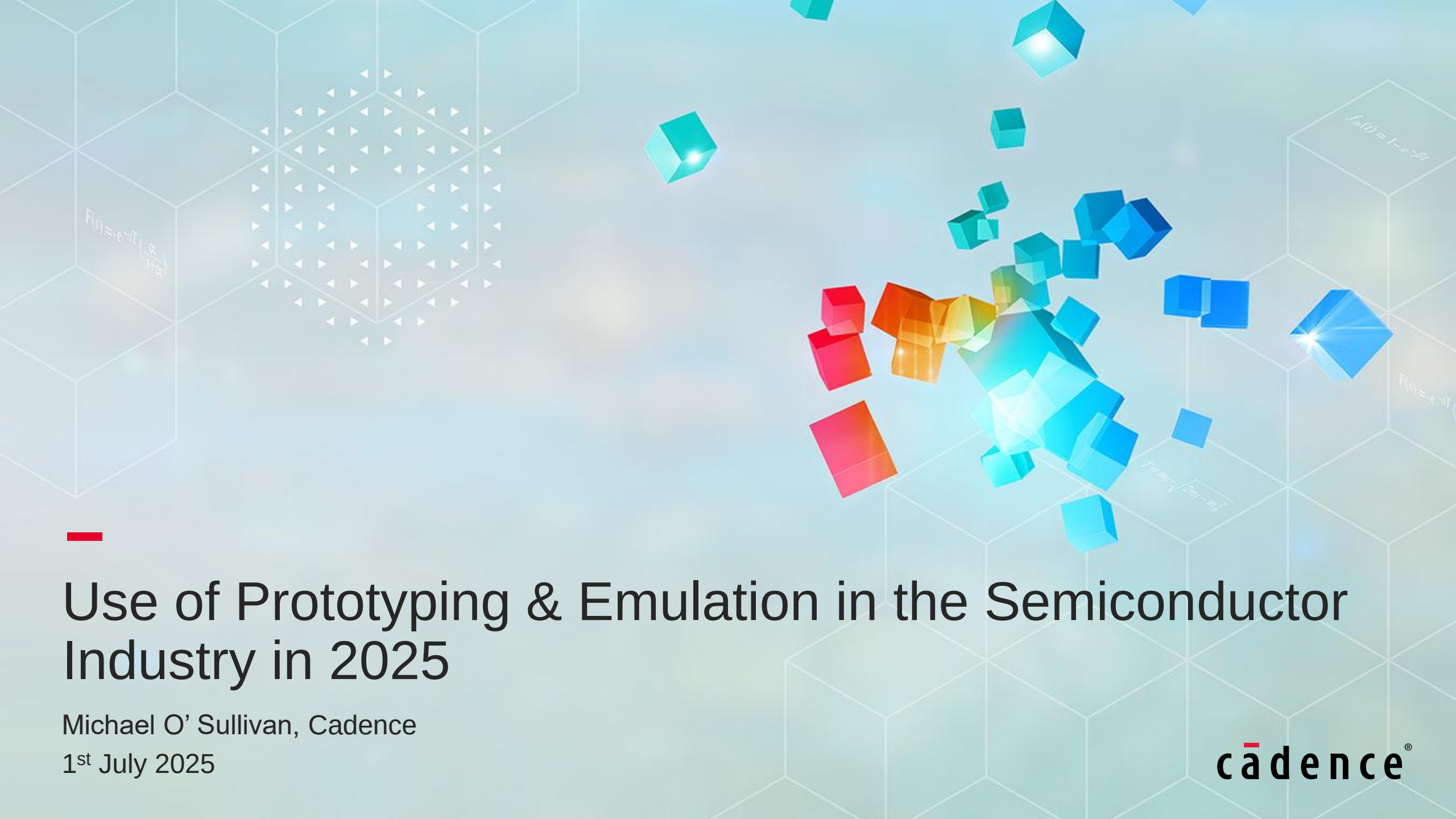


Use of Prototyping & Emulation in the Semiconductor Industry in 2025

Michael O' Sullivan, Cadence

1st July 2025

cadence®

Cadence

An AI Computational Software Leader

OUR MISSION is to innovate technology and productivity solutions for an AI-enabled world

OUR SOLUTIONS enable engineers and scientists to bring innovative new products to life

Hyperscale Data Centers and Communications

Transportation, Robotics, and Machines

AI-Enabled Sciences

Cadence at a Glance

An AI Computational Software Leader

CORPORATE

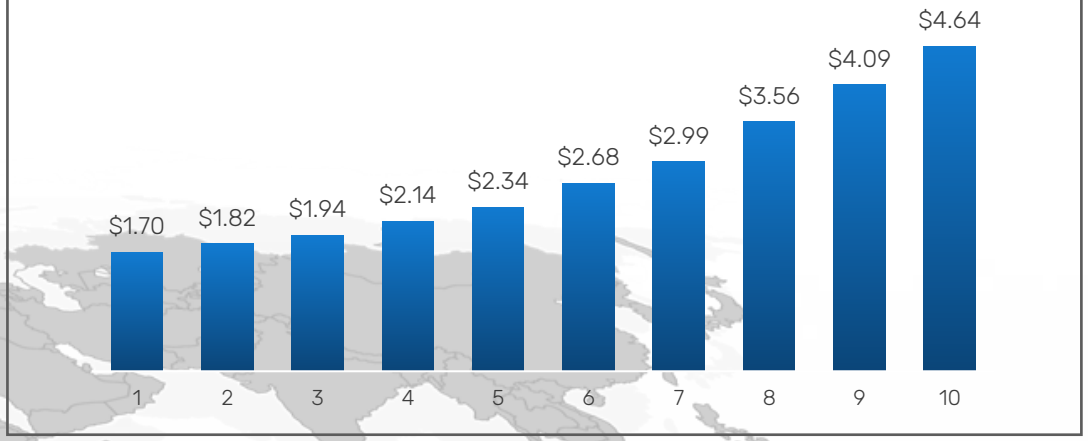
13,000+
Global Employees

35.3%
Revenue Invested in R&D

40
Global Development Centers

1600+
Patents Awarded

REVENUE ($B)



RECOGNITIONS

Wall Street Journal's Best Managed Companies 2025

Time's World's Best – Sustainable Growth Companies 2025

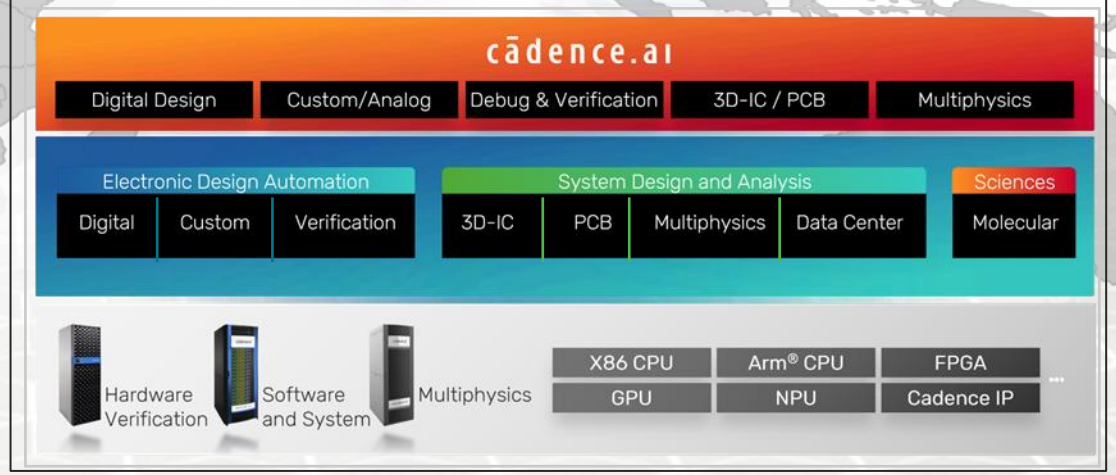
Newsweek's America's Most Responsible Companies 2025

Fortune's 100 Best Companies to Work For 2025

Fast Company's Most Innovative Companies 2024

Time's America's Best Mid-Sized Companies 2024

ACCELERATED DESIGN TECHNOLOGIES

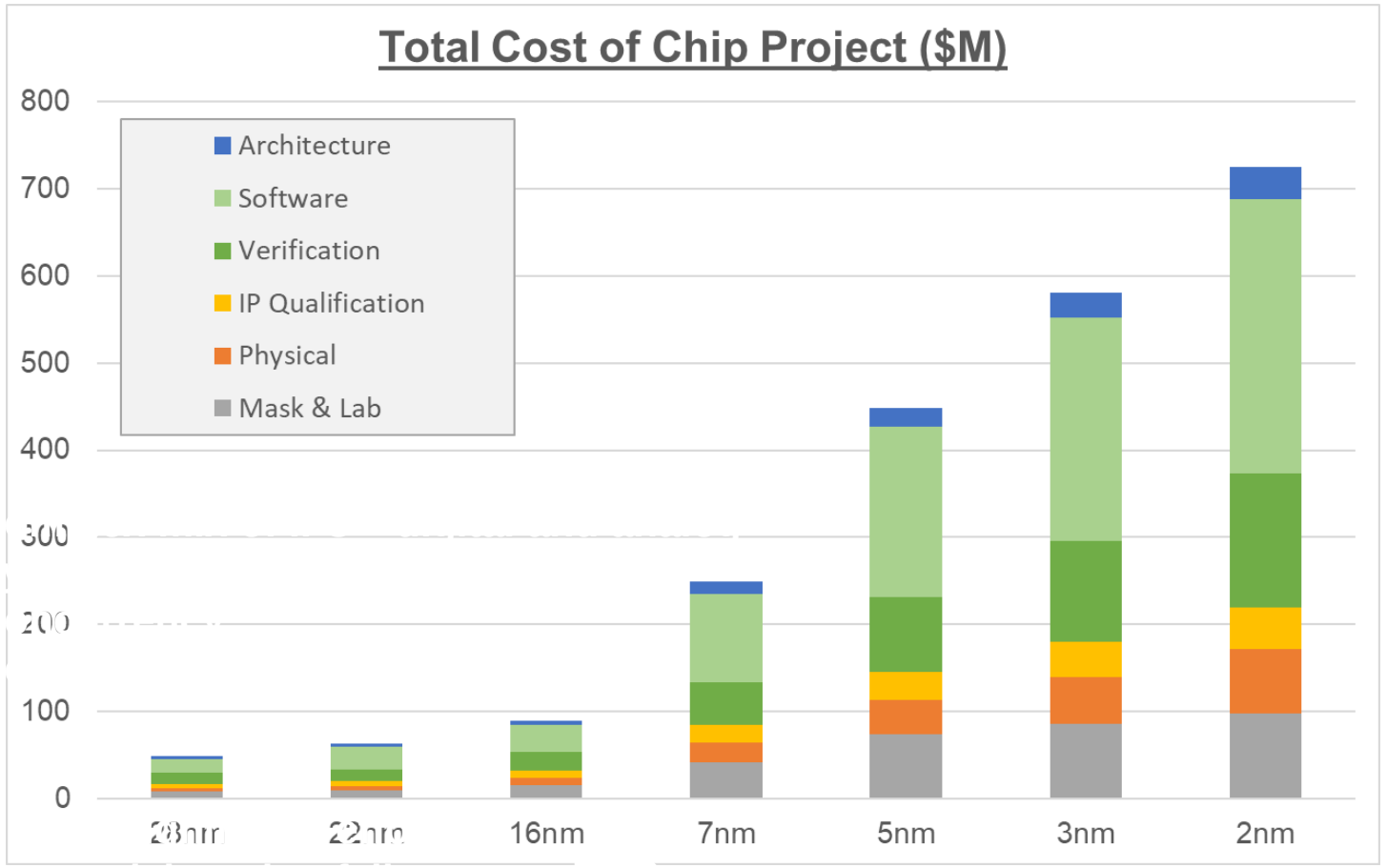


Source: Cadence Earnings Press Release, April 28, 2025
https://www.cadence.com/en_US/home/company/newsroom/press-releases/pr-ir/2025/cadence-reports-first-quarter-2025-financial-results.html

Agenda

- Use of emulation/prototyping in the semiconductor industry
- Cadence platforms for emulation/prototyping
- Summary

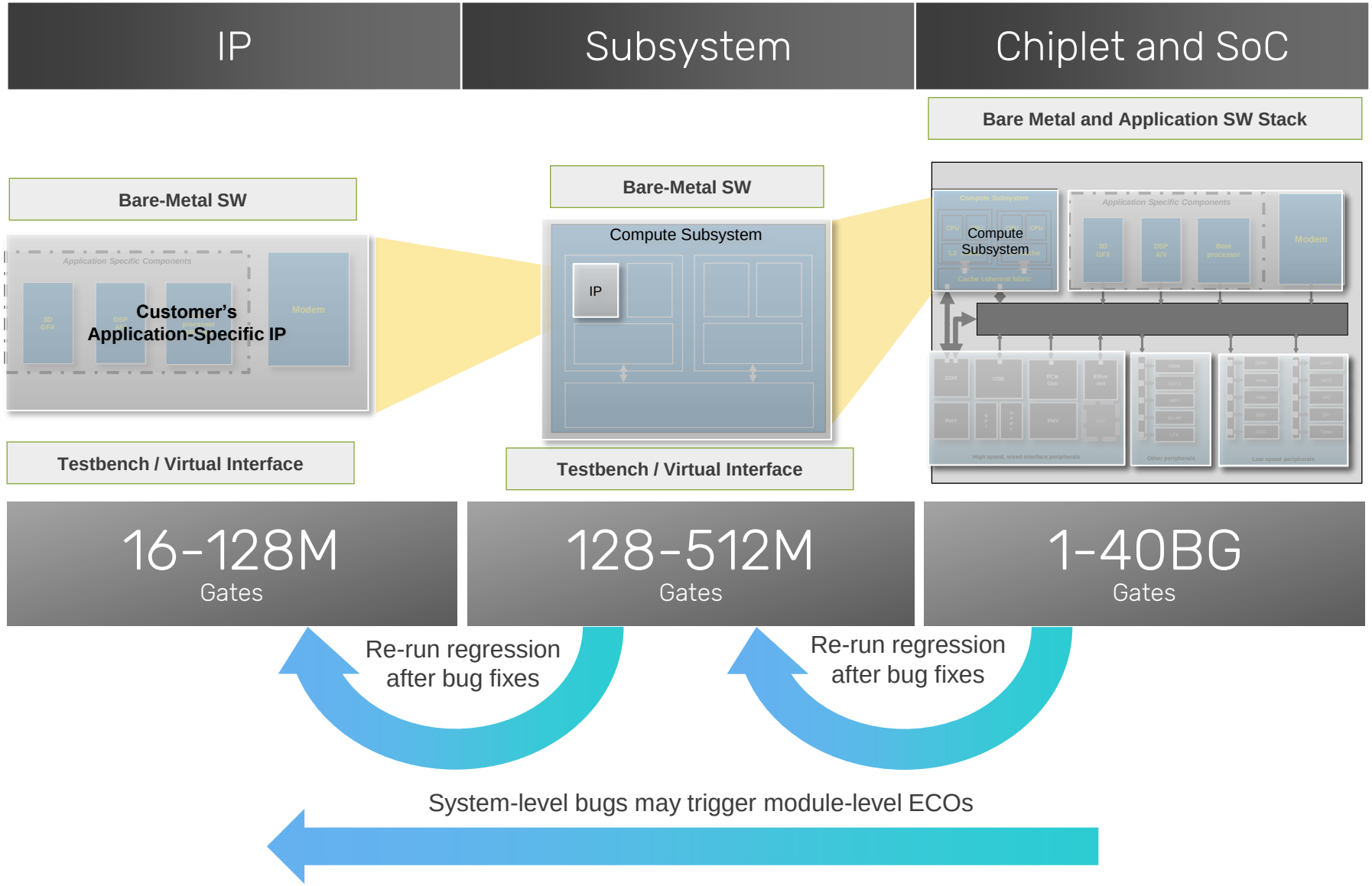
Software Verification Challenge



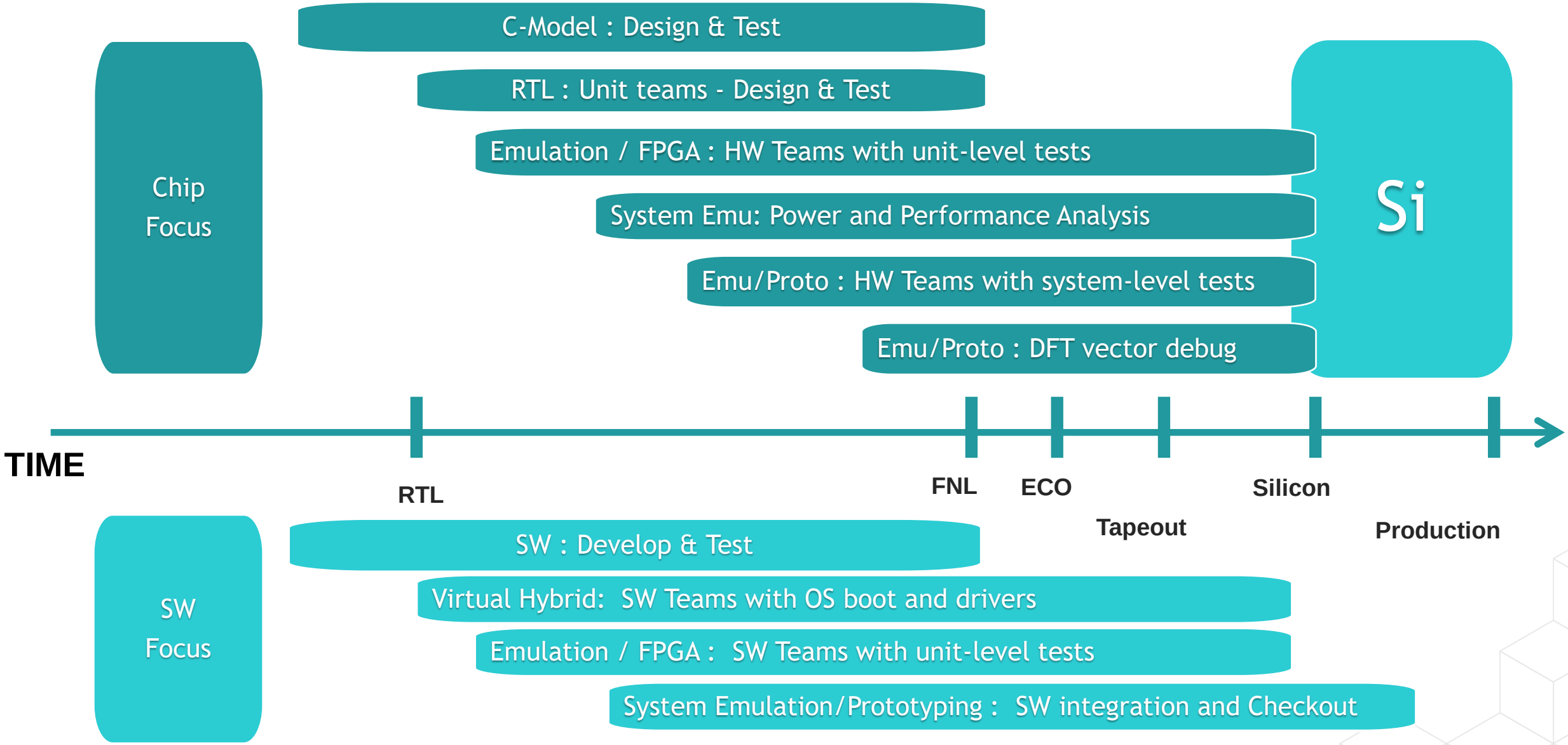
75%+ project costs in software and verification

IBS July 2022

Verification for Different Sizes of Payloads

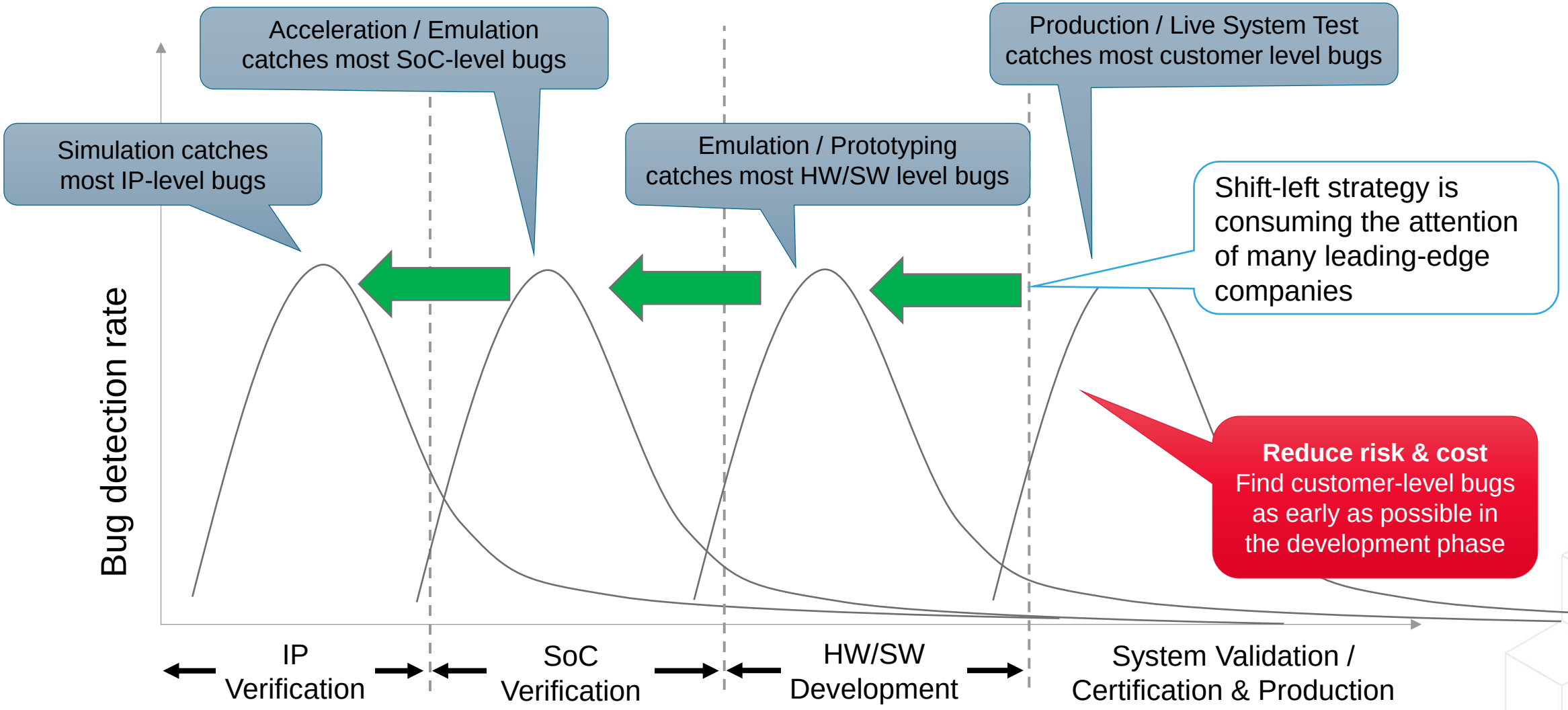


Emulation & Prototyping: D&V Methodology Example



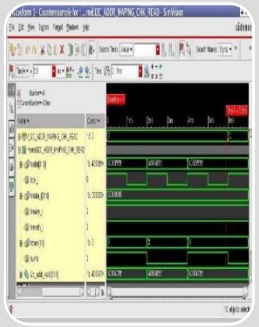
Challenge: more silicon and system development in less time

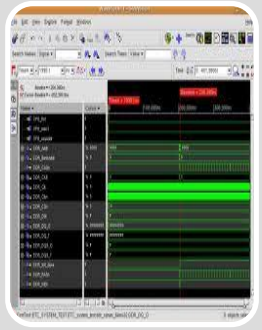
Bug detection still not as early as possible

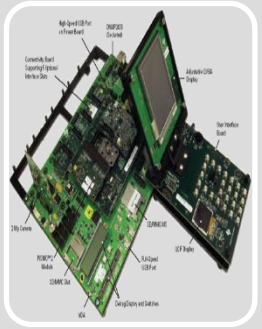


There is no “One Size Fits All”

Verification and software platforms need to interoperate







SDK OS Simulation

- Highest speed
- Earliest in the flow
- Ignore hardware

Virtual Platform

- Almost at speed
- Less accurate (or slower)
- Before RTL
- Great to debug (but less detail)
- Easy replication

Formal Analysis

- Non-scalable
- Exhaustive
- Early RTL
- Great for IP
- No SW execution

HDL Simulation

- KHz range
- Accurate
- Excellent HW debug
- Broadly available
- Mixed-abstractions
- Limited SW execution

Acceleration Emulation

- MHz Range
- RTL accurate
- After RTL is available
- Good to debug with full detail
- Expensive to replicate

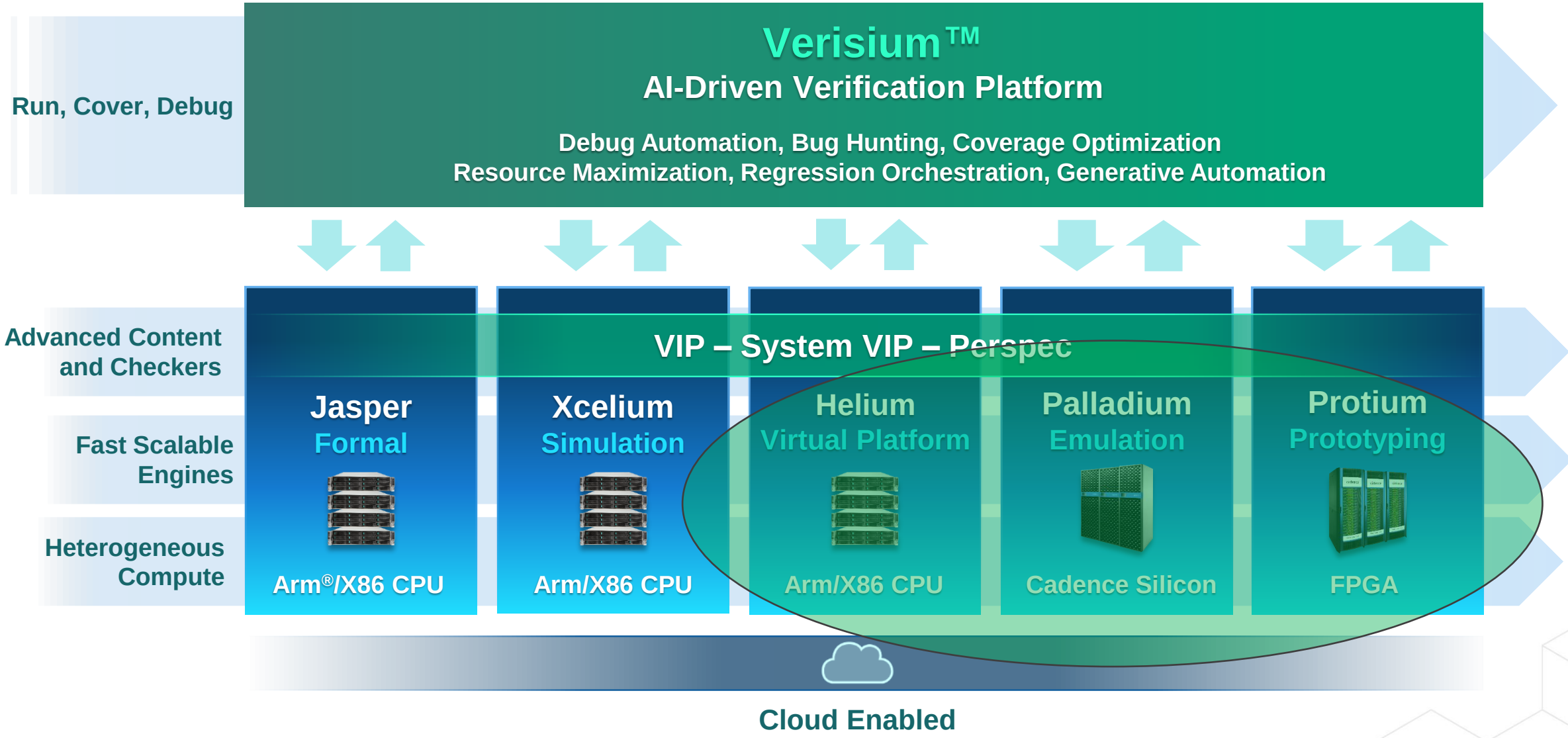
FPGA Prototype

- 10’s of MHz
- RTL accurate
- After stable RTL is available
- OK to debug
- More expensive than software to replicate

Prototyping Board

- Real time speed
- Fully accurate
- Post Silicon
- Difficult to debug
- Sometimes hard to replicate

Cadence AI-Driven Verification Full Flow



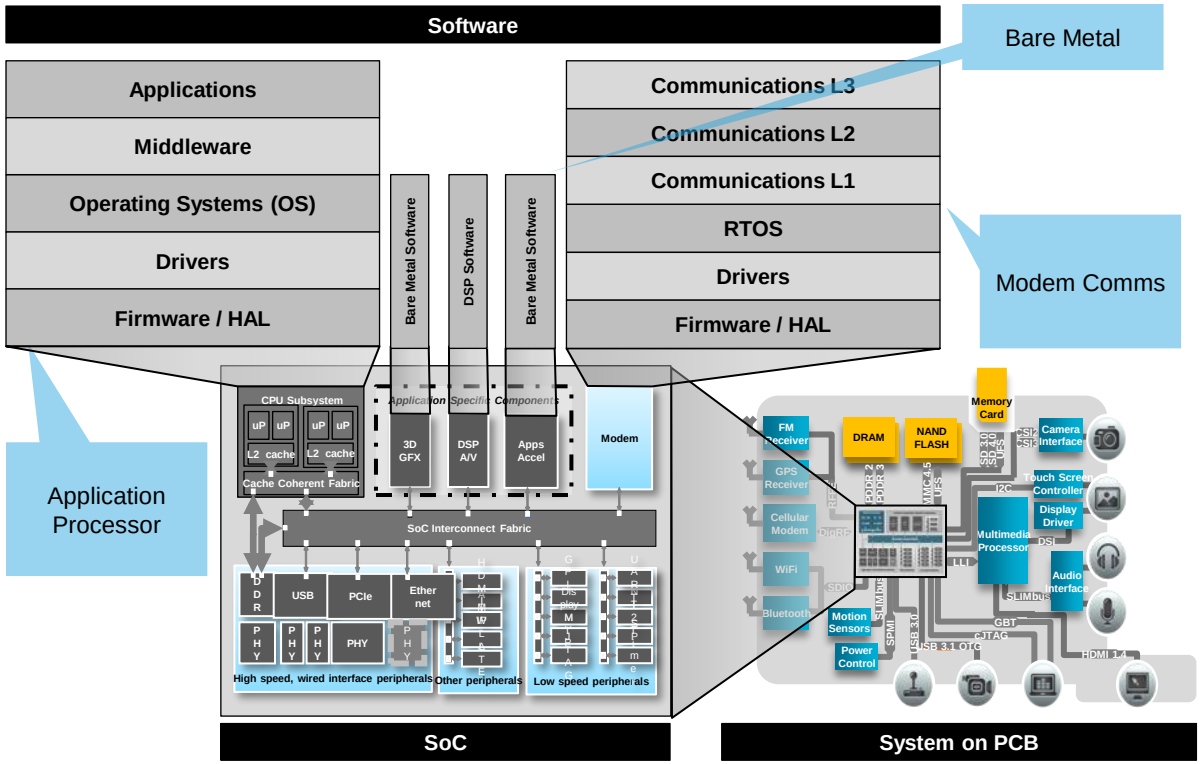
System and Chip Design Trends

Business challenges

- Time-to-market
- Development cost reduction

Technical challenges

- Multi-core design and verification complexity
- Integration of new IP, subsystems in derivatives
- Software stack development and bring-up
- Hardware-software convergence
- **More than 60% of effort in software**

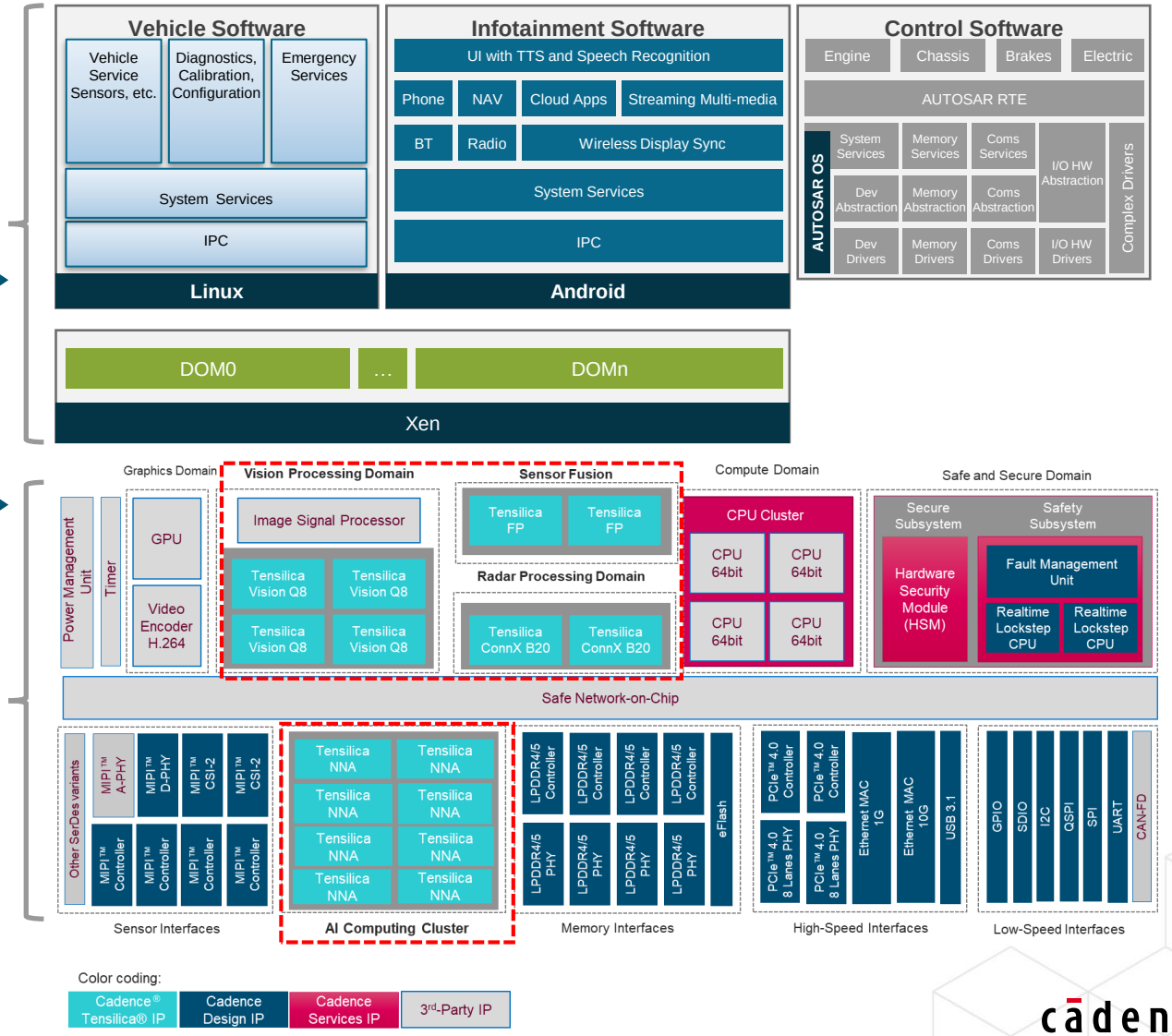


Design Trends Practical Result

Formerly separate projects must converge, software is a fundamental component

Software

Hardware



- Hardware is not complete until it works with the software and vice versa
- Teams cannot afford to work sequentially

Cadence Helium Digital Verification Process

Virtual Platforms

- Software development and verification ***in parallel with*** hardware development and verification
- Validated software simplifies verification

Hybrid Platforms

- Software development and verification ***foundationally integrated with*** hardware development and verification
- Start both before either are complete
- Accuracy and speed where you need them

Virtual Platforms

Transforming software development

Controllability, Observability, Repeatability

Instruction Accurate

- Target software runs without changes

Full programmers view

- Memory, registers, and interrupts

Loosely Timed

- Fast enough for OS Boot

Available Early

- 6-12 months before silicon

All in Software

- Run on standard x86 workstations

Hybrid Platforms

Transforming software-driven verification

Mixed Accuracy

- RTL for DUT
- TLM for context

Full Programmers' View

- Memory, registers, interrupts, and pins

Mixed Abstraction

- Fast enough for OS Boot
- Detailed enough verification

Available Early

- As soon as the DUT is ready

Integrated with Hardware

- Palladium® and Protium™ platforms for capability and performance

Balance of Speed and Accuracy

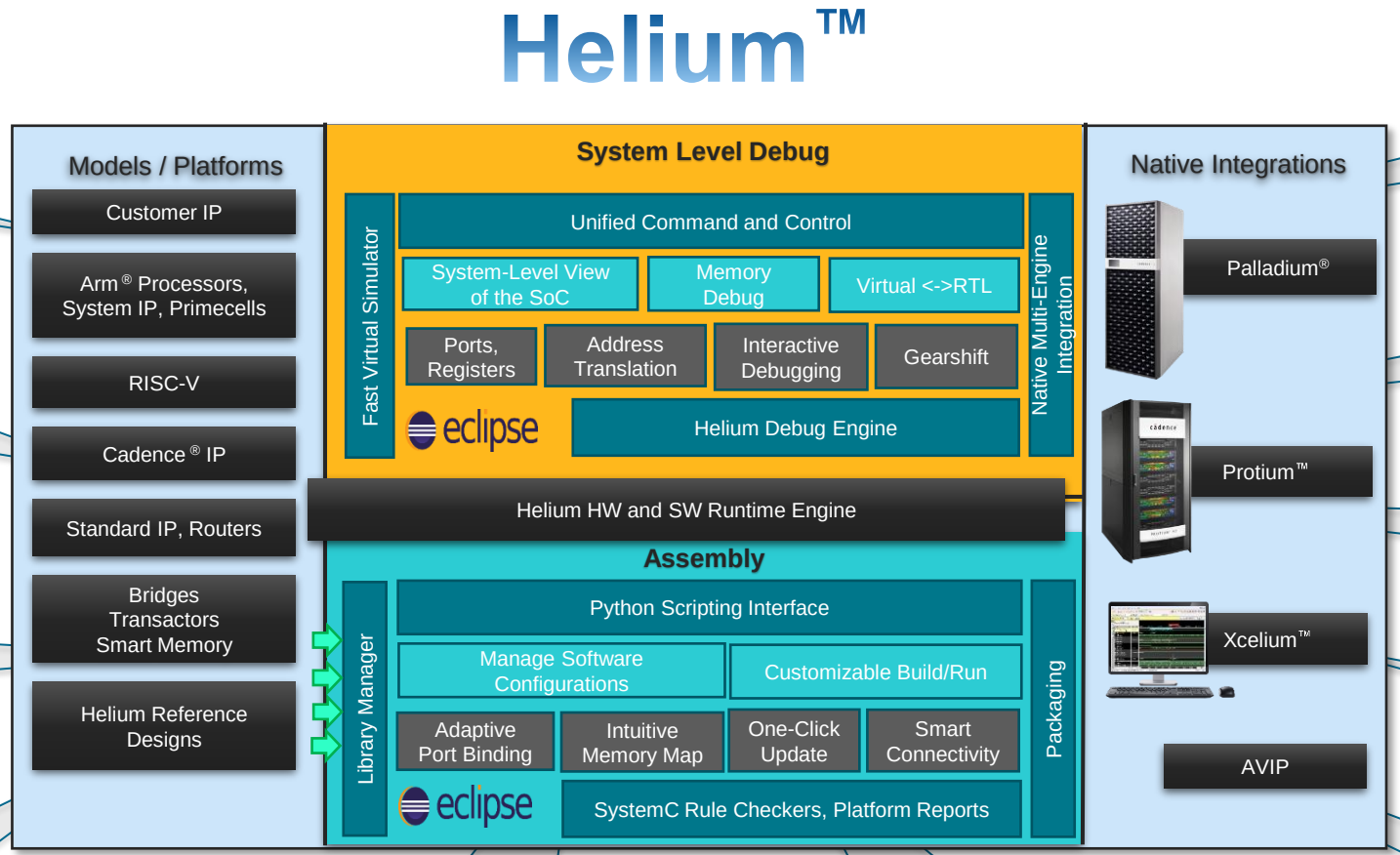
Helium Virtual and Hybrid Studio

The key to a flow that connects verification and software together

Comprehensive Model Library

Connect RTL with TLM to form hybrid platforms

Helium reference designs for quick SoC bring up



Uniform experience across a diverse ecosystem

Save/Restart across engines

Intuitive visualization and rapid prototyping features

Multiple engines RTL with common features

"Correct by construction" avoids common pitfalls in platform authoring

Load and debug the software stack across virtual and RTL cores

Single interface for inspection, control, and debug of software, models, and RTL

Helium and xeDebug UI work together to debug HW/SW issues

Cadence + VLAB Works

VLAB™ Virtual BSW Platform (VDM T3)

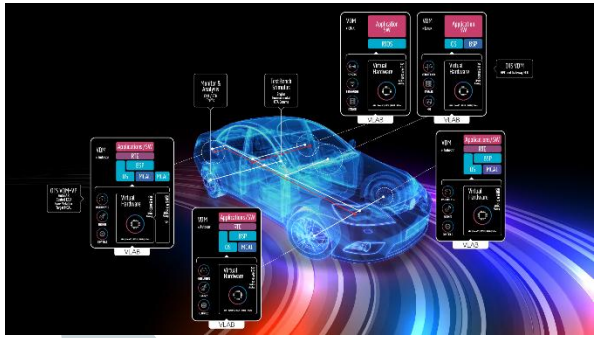
- Virtual ECU Level 2
- Digital Twin for Apps SW
- Software Debug, Test, Analysis
- Ultra-High performance
- Runs in Helium**

VLAB™ Virtual OS/BSP Platform (VDM T2)

- Virtual ECU Level 3
- Digital Twin for Apps and Base/MW SW
- Software Debug, Test, Analysis
- Ultra-High performance
- Runs in Helium**

VLAB™ Virtual Platform (VDM T1)

- Virtual ECU Level 4
- Digital Twin for Entire SW Stacks, including OS, BSP and Firmware
- Software Debug, Test, Analysis
- Ultra-High performance
- Assets shared with Helium**



Cadence / VLAB Vehicle Scale Digital Twin

- Vehicle to Virtual ECU to Software to RTL
- Mix and Match Digital Twin, software and hardware verification platforms as needed for use cases
- Path to VHILS, Vehicle Networks, FMI, and Automotive Toolchains and Environments
- Assets shared with software development test flow
- Assets shared with hardware development and verification flow

Software D&T Environment

Hardware V&V Environment

Helium™ Virtual Platform

- Pure virtual hardware platform
- Digital Twin for platform critical software and prep for verification use cases
- High performance SystemC
- Assets shared with Hybrid
- Assets shared with VLAB**

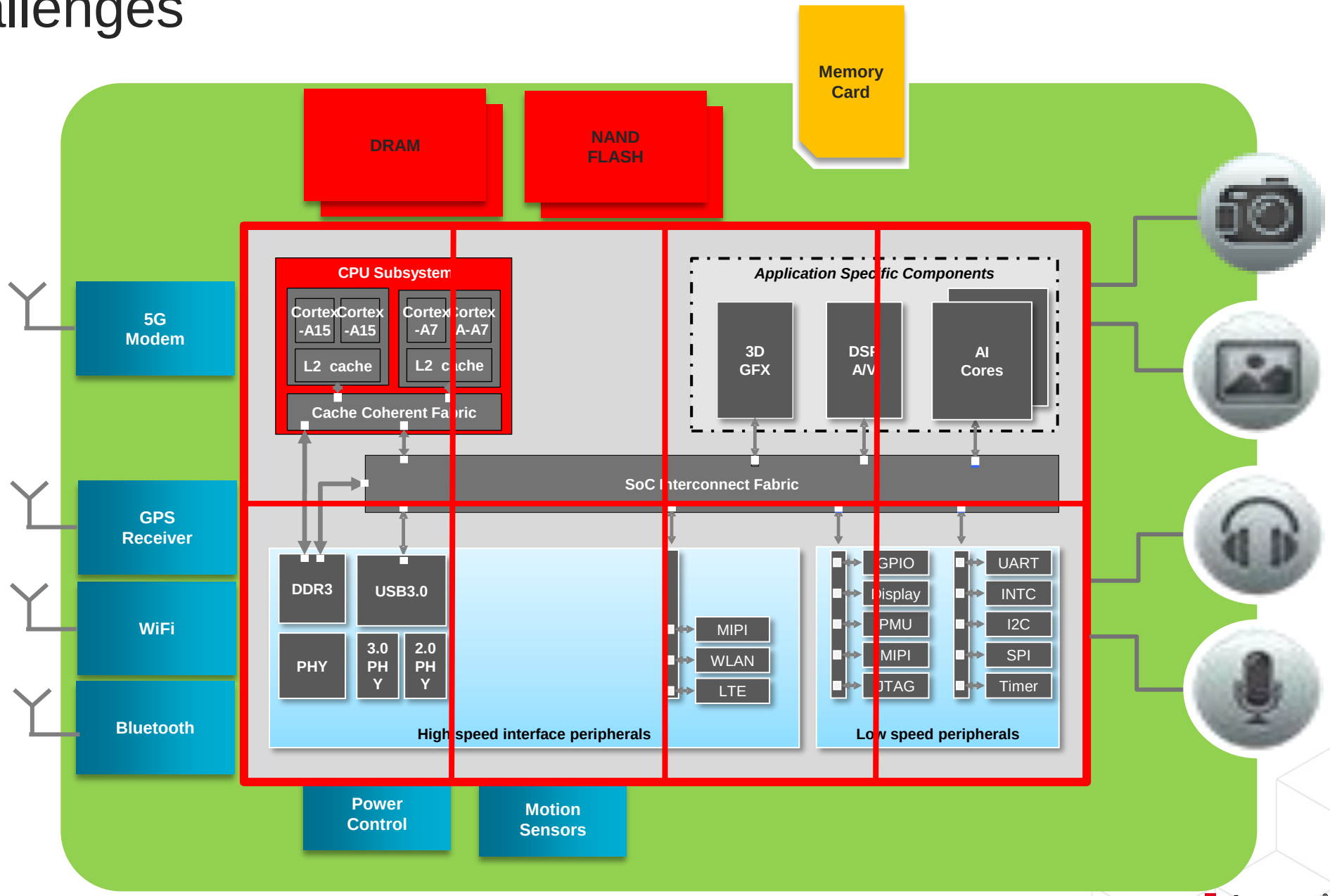
Helium™/Protium™ Prototyping Hybrid

- Highest performance RTL verification platform
- RTL regression and timing critical software use cases
- All virtual assets are part of Helium

Helium™/Palladium® Emulation Hybrid

Prototyping challenges

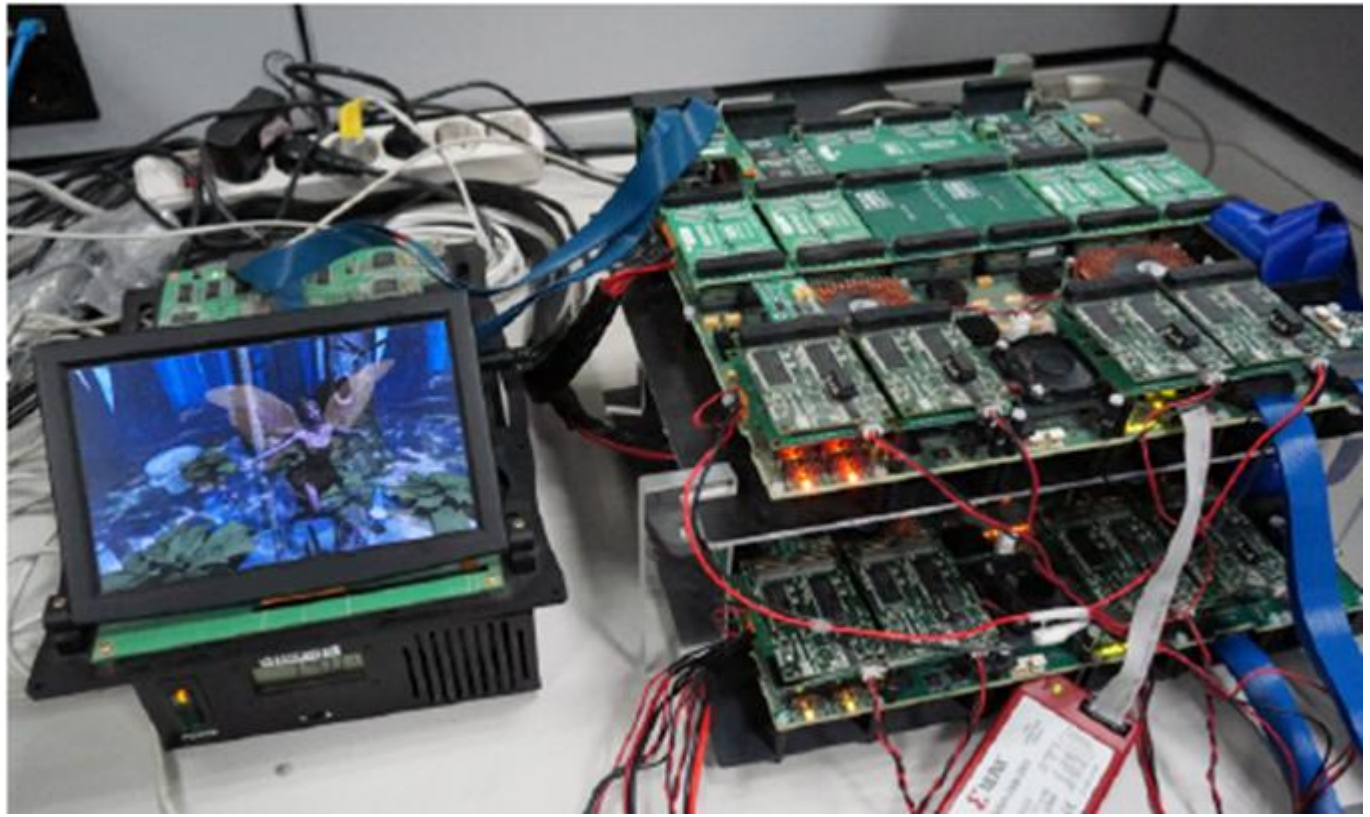
- Mapping ASIC clocking into FPGAs (RTL changes)
- Mapping ASIC memories into FPGAs (RTL changes)
- Interfaces that require speed-adaption (RTL changes)
- Design > 40MG (FPGAs partitioning)
- Debug HW+SW (Tools support)



So … Traditional prototyping is not suitable anymore

- Too many gates
- Too much memory
- Too many peripherals
- Too much software

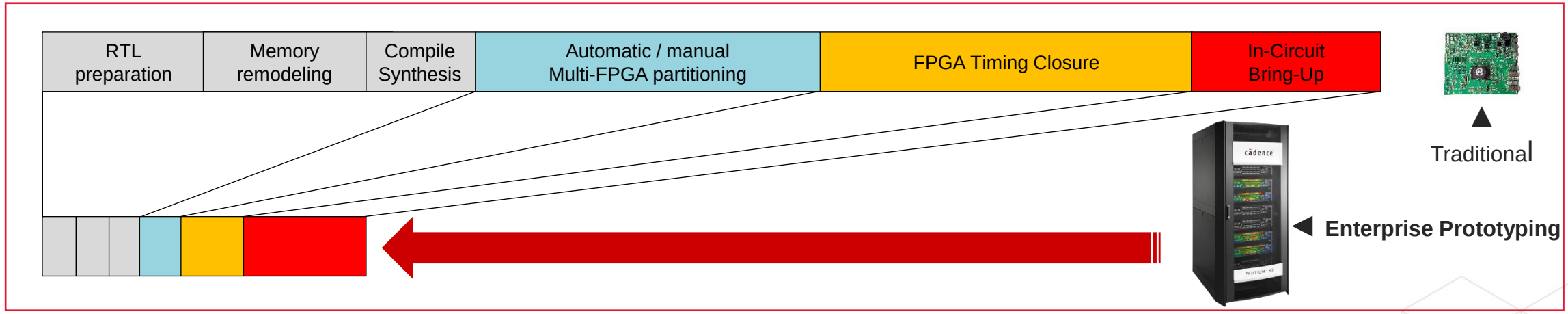
  …
- Not enough time
- Needs to be remotely accessible



And That Brings Us To Enterprise Prototyping … Addressing Those Challenges!!!

Compiler Automation takes the pain away from mapping to FPGA

- Takes ASIC RTL and with little or no modification maps it into FPGAs
  - Clocks, Memories
  - Fully automatic, multi-FPGA partitioning
  - FPGA timing closure
  - Fully integrated FPGA PnR
  - Speed Bridges, Virtual Bridges, Memory models



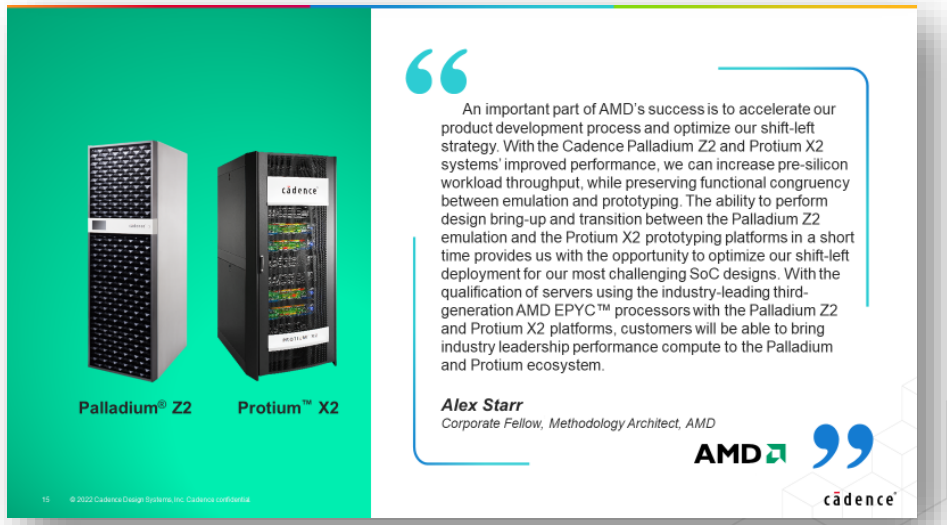
Cadence's Dynamic Duo

Palladium

- Compile Predictability → **9 of the top 10 Hyperscale Companies**
- Multi-BG Scalability → **12 of the top 15 Semiconductor Companies**
- HW Verification Throughput → **4 of the top 5 Smartphone / Mobile Application Processor Suppliers**

Protium

- High-Perf SW Validation → **6 of the top 10 Hyperscale Companies**
- Multi-BG Scalability → **9 of the top 15 Semiconductor Companies**
- Fast Bring-up via Congruency → **3 of the top 5 Smartphone / Mobile Application Processor Suppliers**



cadence

Dynamic Duo III Verification Platforms Benefits

Scalability, Congruency, High performance

Enterprise scalability:
16MG to 48BG
reduces cost of
ownership

Shared front-end,
fastest compile for
billion-gate designs

1.5X faster than
Palladium Z2
with at-speed debug

Palladium® Z3

Enterprise scalability:
40MG to 48BG
8X density reduces
datacenter costs

Fast bring-up time
with Palladium
congruency

1.5X faster than
Protium X2
3-5X faster than
Palladium Z3

Protium™ X3

Emulation Features and Applications

- Modular Compile: 8-hour TAT for any size design
- FullVision Debug: observe any signal with at-speed triggering
- Exclusive use models: 4-state and mixed-signal emulation, 95% accurate power analysis

Prototyping Features and Applications

- Modular Compile: 24-hour TAT for designs up to 20 BG
- FullVision Debug: observe any signal without recompile
- Shared Virtual and Physical interface and debug solutions with Palladium

Cadence Dynamic Duo III

Unified compile and virtual/physical interfaces

Palladium® Z3

Cadence® Z3
Emulation Processor

3-5X faster
Quick bring-up

Protium™ X3

AMD VP1902
Adaptive SoC

build → run → debug → build → run → debug → build → run → debug

#1 for total TAT

- 1.5x faster than Z2
- 2x more capacity per rack than Z2
- Scalable to 48BG
- Mixed-Signal and 4-state support
- Natively integrated power analysis

build → run → debug → run

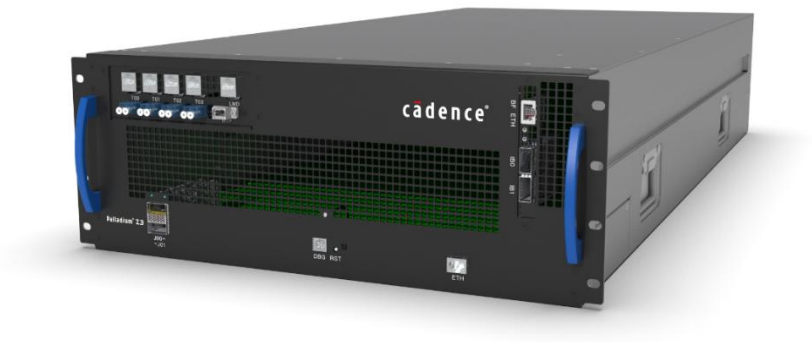
#1 for speed

- 1.5x faster than X2
- 3.3x more capacity per rack than X2
- Scalable to 48BG
- Unified compile & testbench link with Z3
- One shot compile technology

Hardware Debug Focus ← → Software Debug Focus

New! Palladium Z3 System Studio

- Standalone emulator with capacity of 128 million gates
  - No Cadence install required – unpack and go
  - Standalone 4U form factor
  - Air-cooled with front-to-back airflow
  - Powered from typical lab outlets: 110/220V 15/20A
- Supports up to 8 concurrent users per unit
- Supports up to 4 SpeedBridge ports
- Same software and flow as Enterprise Z3 rack system

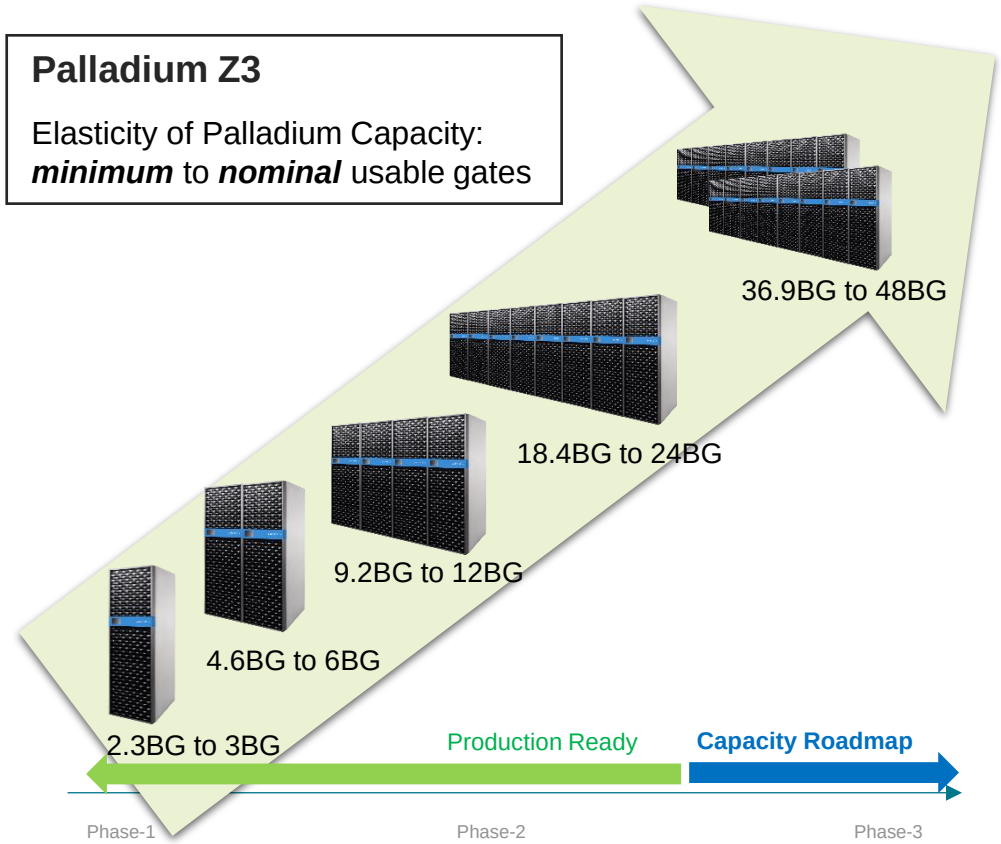


Palladium® Z3
Model: System Studio
Standalone 4U form factor

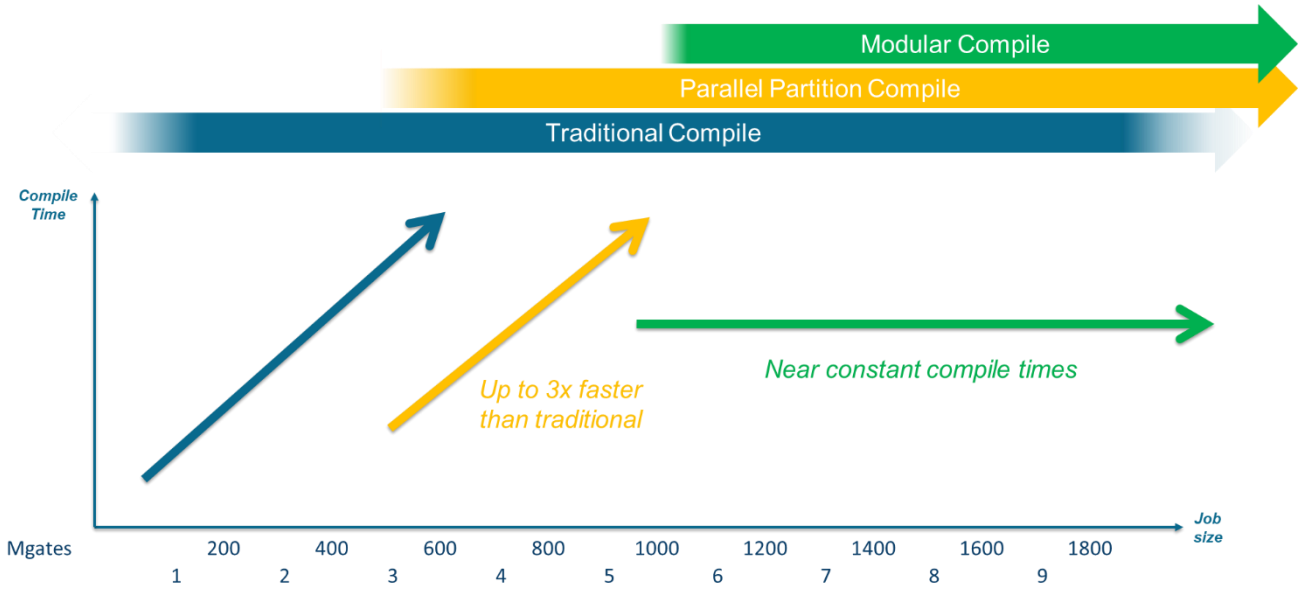
Scaling both **Capacity** and **Compiler** to accommodate rapid design growth

Palladium Z3

Elasticity of Palladium Capacity:
minimum to ***nominal*** usable gates



- Z3 capacity scaling to 48BG with user-control granularity of 16MG increments
- Capacity utilization at 100% guaranteed due to processor-based mapping technology



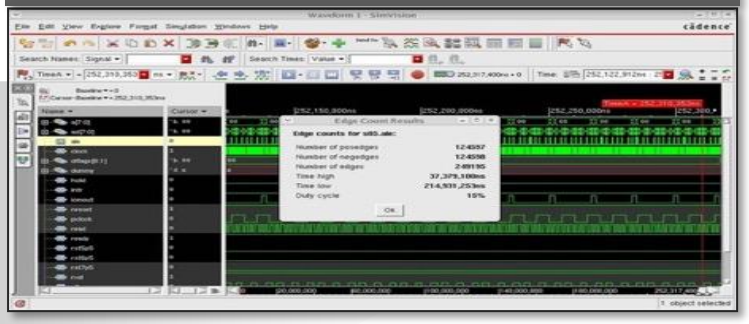
- Modular Compile enables nearly constant compile times based on massively parallelized processor-based compiler with no timing closure required
- Design performance is 100% predictable after compilation

Dynamic Duo III Debug Productivity

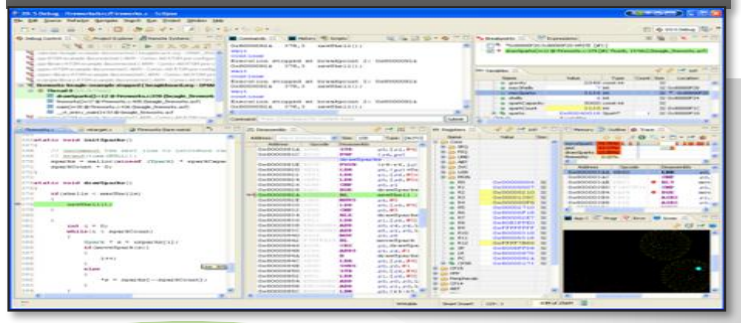
Palladium® Hardware-Focused Debug

Protium™ Software-Focused Debug

Hardware Debug: RTL

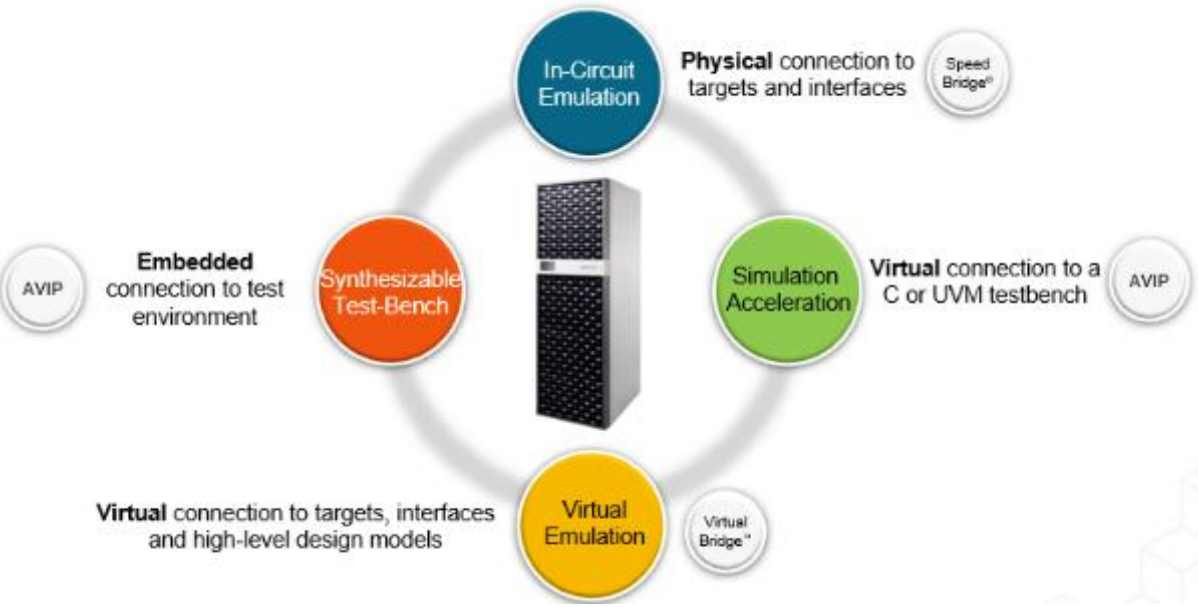


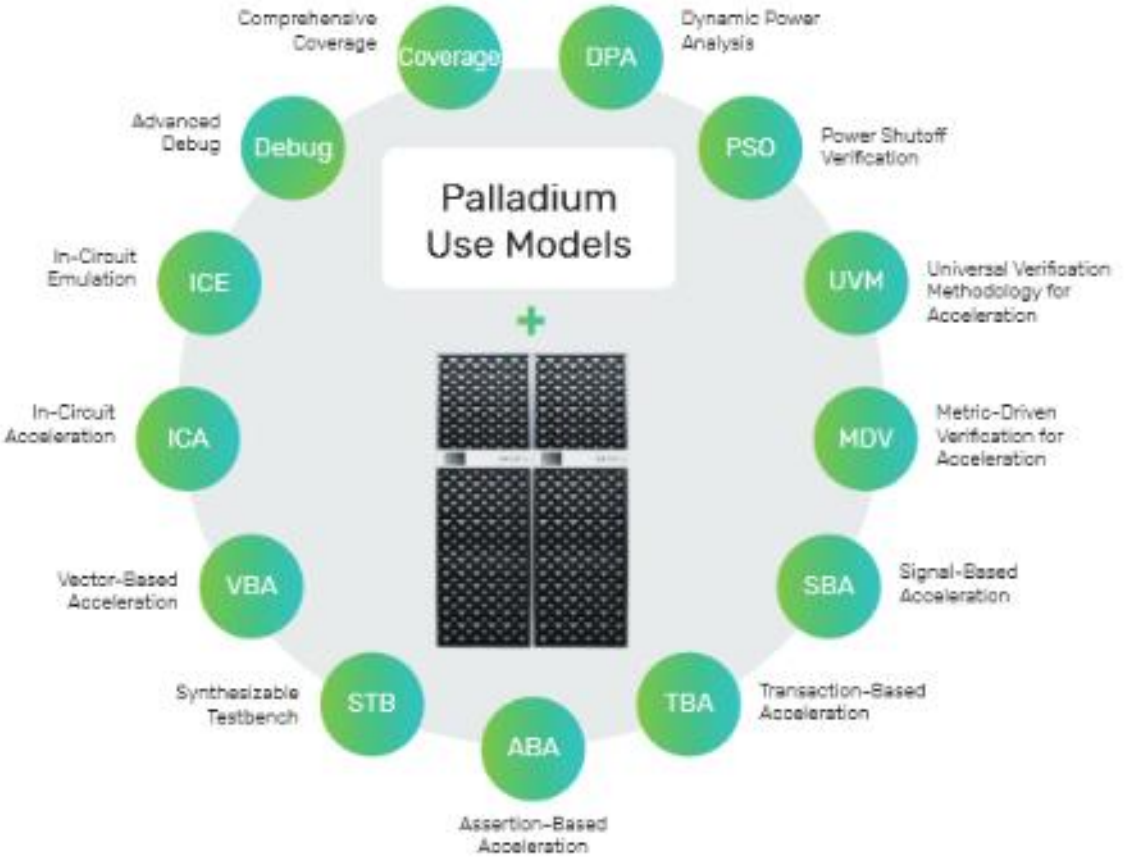
Software Debug: C Code



- FullVision Waveforms
- At-Speed Streaming Probes
- Code and Functional Coverage
- Dynamic Probes
- Dynamic RTL and SDL
- Save and Restore
- Force and Release
- Assertions
- Record and Replay
- Memory Backdoor Read/Write
- FullVision Waveforms w/o predefining probes
- At-Speed System Probes
- High-Speed I/O Probes
- Lightweight Assertions

The Many Use Cases of Palladium® Emulation





HW Product Portfolio and Solutions

Consumer | Hyperscale | Mobile | Communications | Automotive | Aero/Defense | Industrial | Life Sciences

Vertical Solutions

Solutions and Apps

Memory Model Portfolio	SpeedBridge®/ EDK	Job Scheduler	Fault Emulation	4-state Emulation
VirtualBridge™ / AVIP	Virtual Test and Virtual Debug	Helium™ Virtual and Hybrid Platform	Power Analysis 3.0	DMS-RNM Emulation

HW Platforms

Palladium® Z3

build → run → debug → build → run → debug

Cloud Enabled

3-5X faster
Quicker bring-up

Protium™ X3

build → run → debug

Acceleration Engines

Summary

- Software becoming even more important
  - The scope and scale are growing exponentially
  - Timelines are shrinking
- Modern Software Engineering Practices Are Required
  - Cloud-based development environments
  - Automated and continuous integration and regression
- Use the different platforms at different stages of the project
  - Virtual Prototyping
  - Emulation
  - Enterprise Prototyping

Cadence AI-Driven Verification Full Flow