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VISC

Versatile Intrinsic Structured Computing

In-Line Accelerator for AI, Maths and Cryptography

Boom in 'Always-on' Real-Time Edge Processing applications is driving demand for Performance with Security

VISC solves the challenges of Real-Time Algorithmic Processing for Edge AI

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RISC-V: Innovating Within an Established Architecture

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Boom in 'Always-on' Edge Real-Time Processing applications is driving demand for Performance with Security

VISC solves the challenges of Real-Time Algorithmic Processing for Edge AI:

- Novel Pre-Pipeline Technology – Processor Independent
- Enables Maximum Efficiency and Simultaneous Execute
- Best Maths per Watt per Dollar
- Patent filed

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We always need more processing performance!

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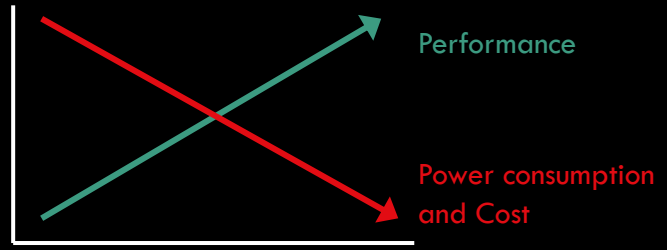
Processor requirement persist:

- More performance
- Lower power consumption
- Lower cost



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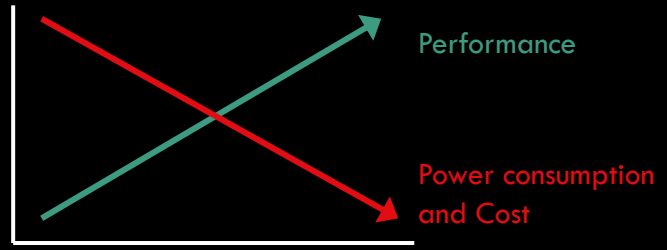

Traditional solution – chase Moore's Law:

- Clock the processor faster to get performance (but increases power consumption)
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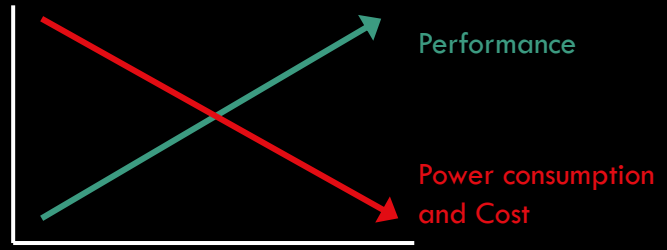

Traditional solution – chase Moore's Law:

- Clock the processor faster to get performance (but increases power consumption)
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Now Moore's Law has hit physical limitations and/or prohibitive costs – Other ways of performance/Power improvement are needed:

- Accelerators

Performance demands will continue to increase –
Smart solutions required

Traditional acceleration vs. VISC acceleration

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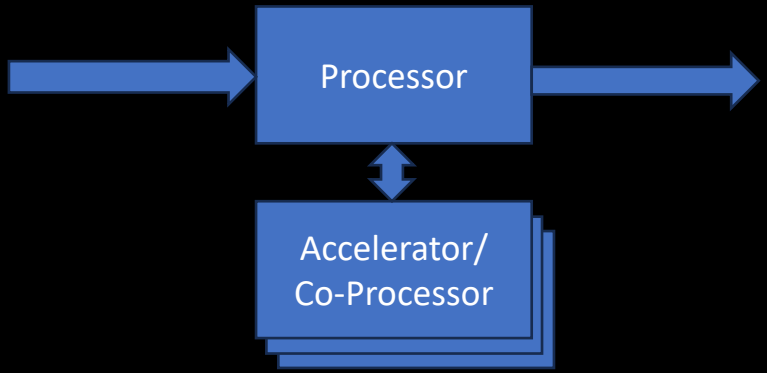
Traditional co-processor acceleration:



- Processor inefficiency is unchanged
- Processor burden is increased by co-processor management
- Accelerators are specific to functionality:
  - Large silicon overhead
  - Inefficient accelerator usage
- Wasted silicon area- cost inefficient

Traditional acceleration vs. VISC acceleration

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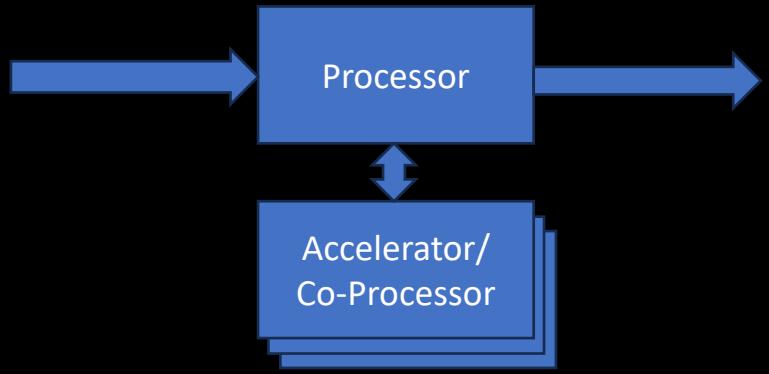

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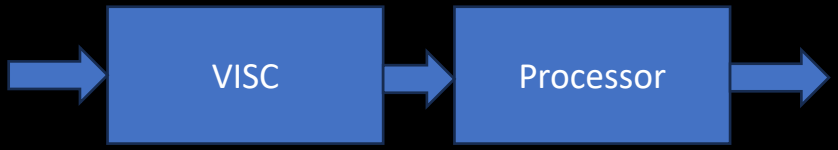
VISC In-Line Acceleration (VILA):



Accelerate All Repetitive Real-time Mathematical Computation

- VILA makes processor execution highly efficient – optimises performance
- Processor unburdened by accelerator – optimises performance
- Minimises clock cycles and memory accesses – optimises power usage
- Efficient use of silicon – optimises cost

Target for VISC is PPAS (Power, Performance, Area, Security) Optimisation

Why technical/commercial disruption happens

1980s

Memec
FAE

NS32000 32bit advanced microprocessor

Market dominated by Intel x86 and Motorola 68000

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CPU implemented to guarantee ‘Right First Time’ - Millions sold

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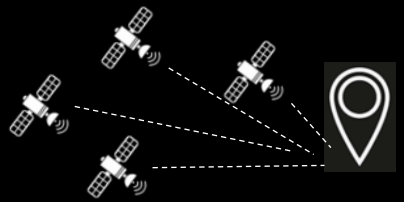

Multi-channel complex spatial computation needed for anti-jamming/spoofing – with picosecond phase accuracy between CPU cores

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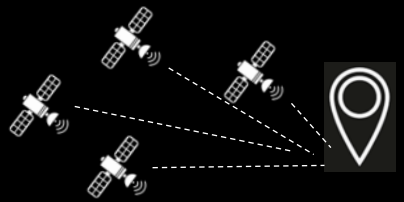

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2020s

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Open-source …
RISC-V

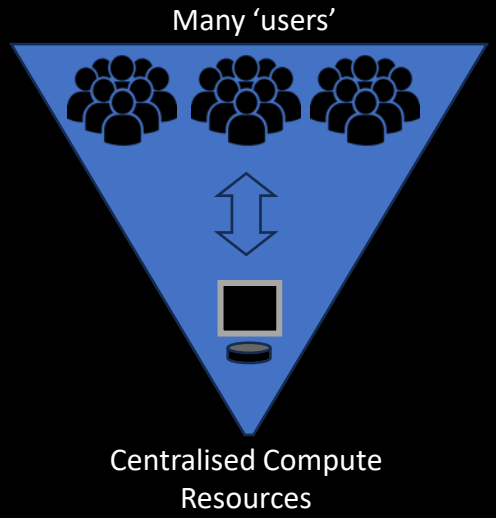
Right price
Right openness
Inadequate native performance

Innovation opportunity!

Inspiration, Contextualisation, Non-linear thinking … Customer NEED

RED Semiconductor - Focusing on AI at the Edge

Generative AI



Chip market dominated by incumbents

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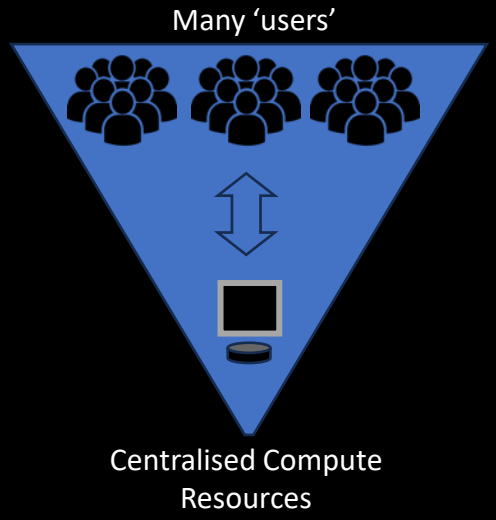
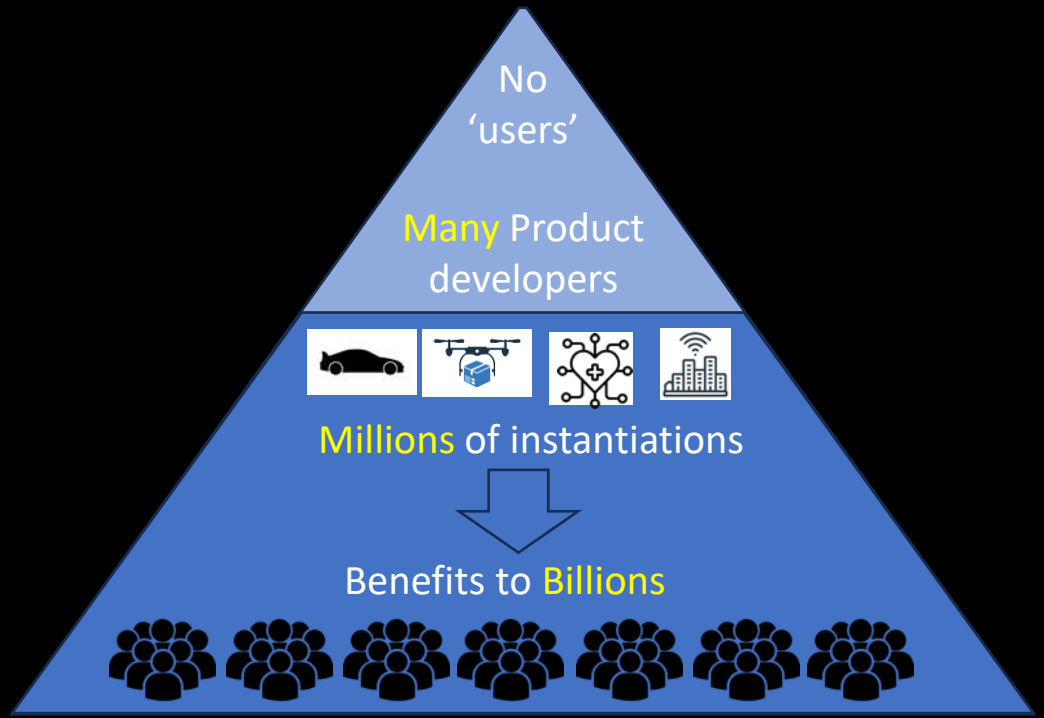


Chip market dominated by incumbents

Edge AI

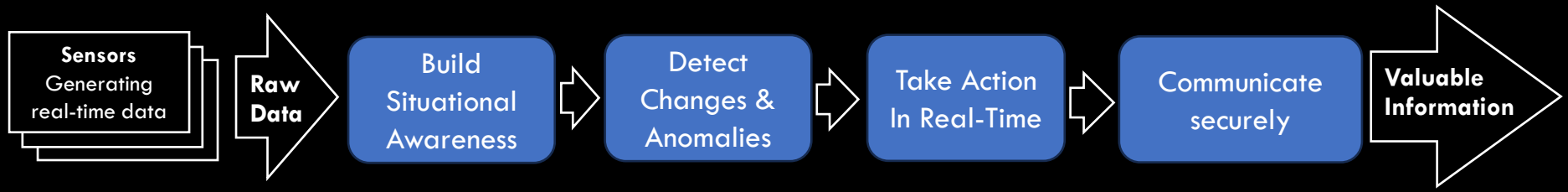


Need for startup innovation

AI at the Edge demands affordable real-time processing of complex data with low power consumption - And it must be secure.

RED's Markets and Applications

Typical Edge Processing demands:



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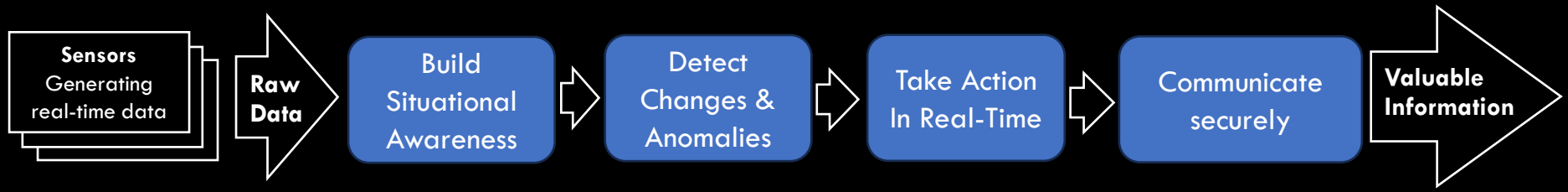

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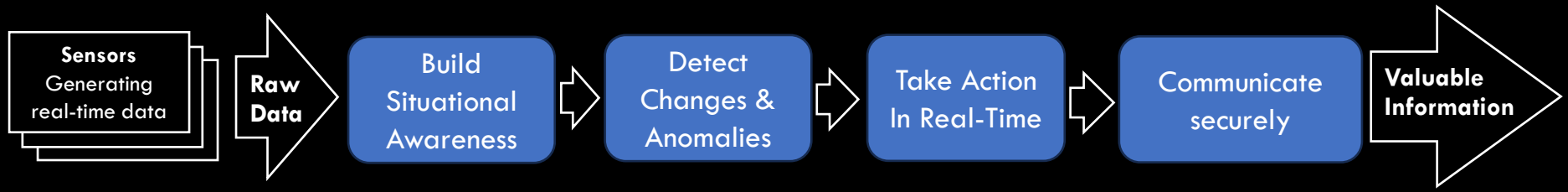
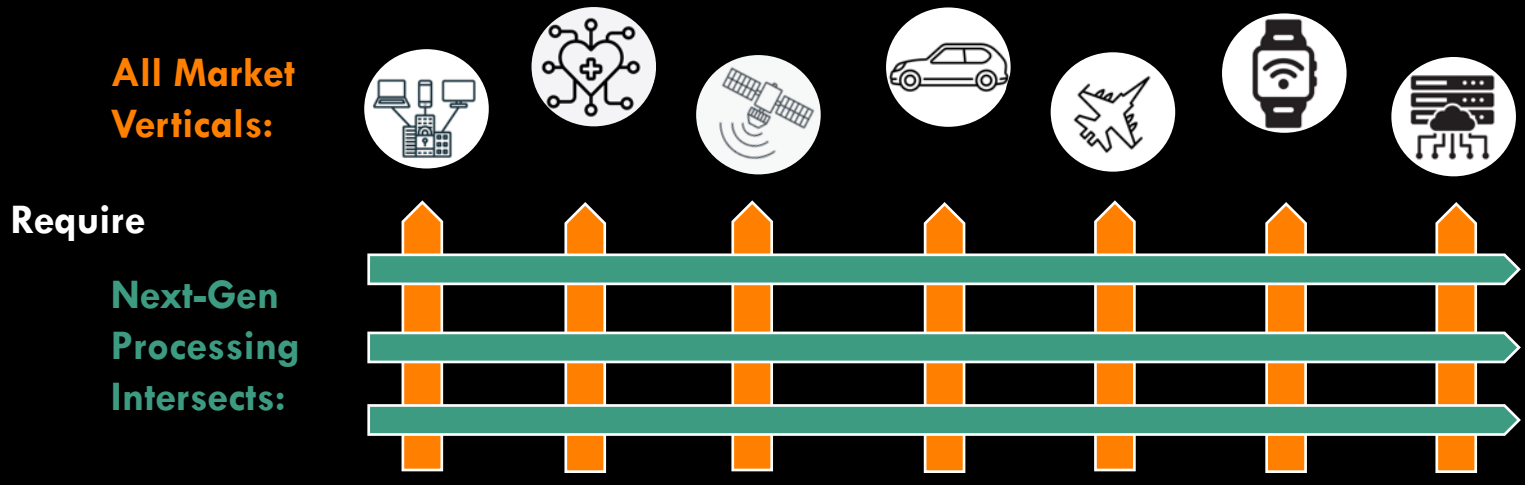


Applies to all market sectors:



Ubiquitous demand for Improved PPA+S

Edge AI – Innovation driven by application need

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Application	Trend
• Transportation	• Safety; Driver Assist; Autonomy…
• HealthCare	• Early Diagnosis; Automated treatment…
• Industry	• ‘Lights-out’ operation (automation and autonomy)…
• Defence	• Intelligence; Readiness; Autonomy…
• Built Environment	• Smart cities; energy security…

Lives saved; Economic productivity grow; Security improved; People thrive

How is RED solving the problem with VISC?

- **What is VISC? – Maths**-oriented Processor accelerator – for markets that need AI, Cryptography, Autonomous Systems computation.

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- **Technical differentiation? –** Comprehensive patent applied for.

VISC's key to real-time execution is processor instruction and data-flow efficiency

How can a startup innovate CPU architecture?

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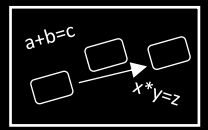
Innovation => Verification flow

Concept



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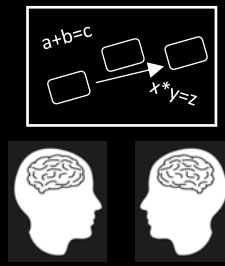
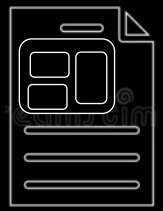
Concept

Functional description





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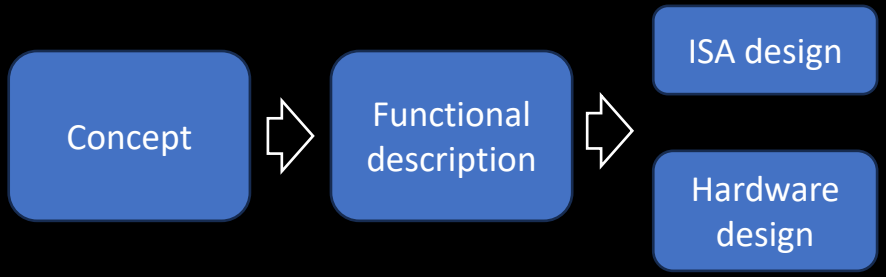

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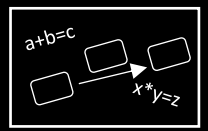

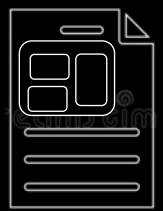

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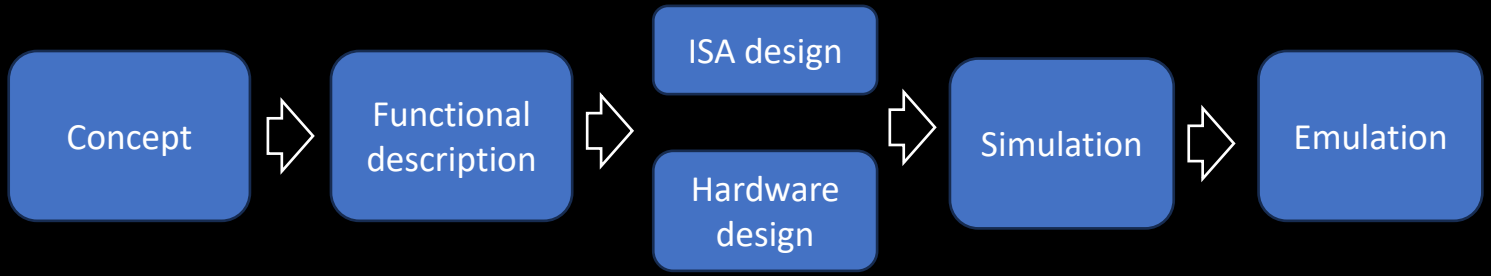
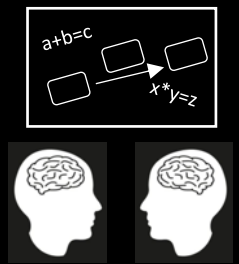
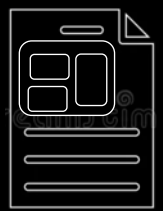
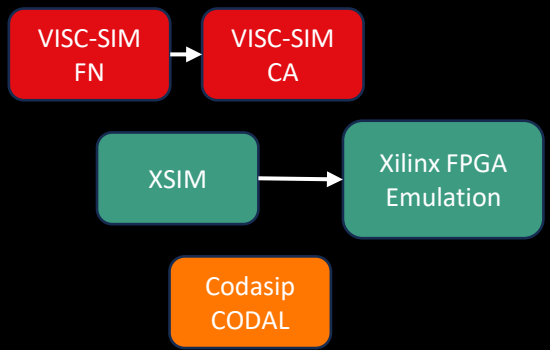






1. Open-source tools
2. Hand crafted sim
3. Industry standard sim
4. Partner architecture sim



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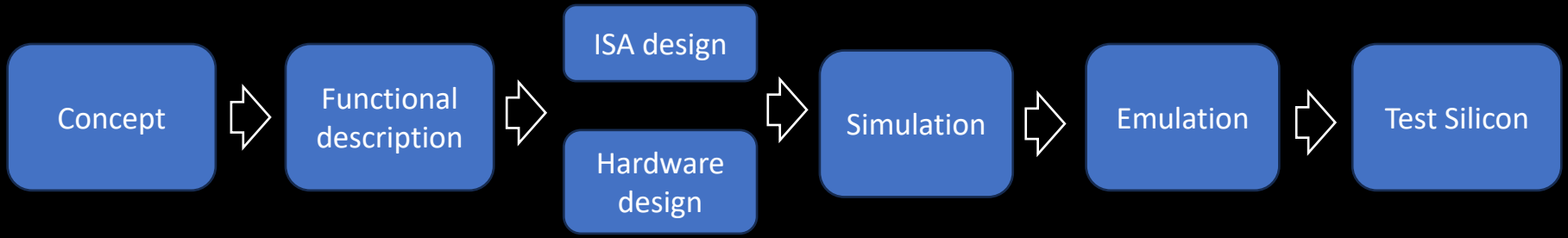

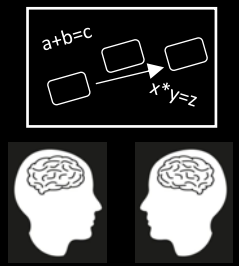

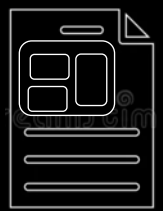

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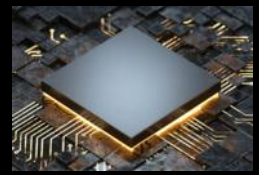

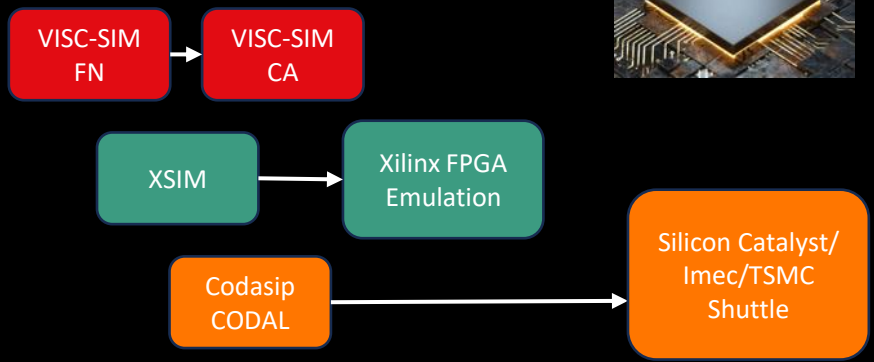

Initial use of open-source tools – leading to industry-standard toolchain

VISC performance – early benchmarks

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Benchmark: 4 x 4 Matrix Multiply (10 repeats)

	Instructions written/compiled	Instructions fetched	Instructions executed	Data memory accesses	Clock cycles to execute
RISC-V	31	3210	321	96	4536
VISC + RISC-V	**10**	**14**	**115**	**48**	**1194**
Performance Multiple	**3x**	**200x**	**2x**	**2x**	**4x**

One-third of the code to write and debug with VISC

Fraction of memory accesses gives huge power saving

400% performance boost with VISC

Big performance gains with only 15% silicon area increase

VISC future performance roadmap

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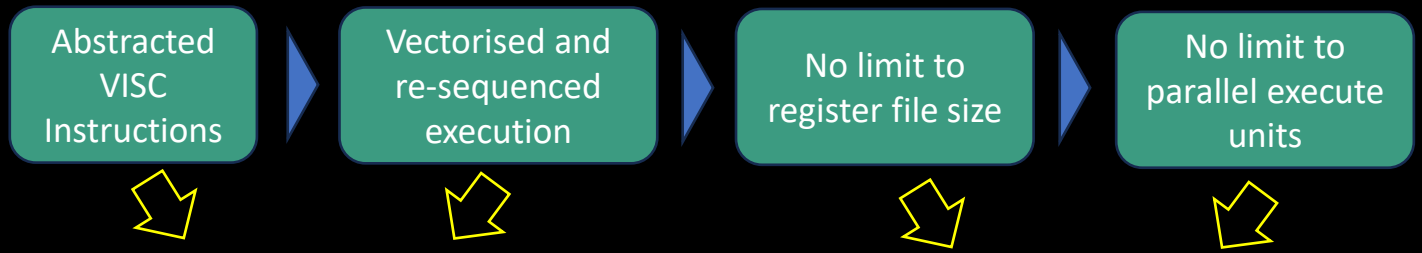
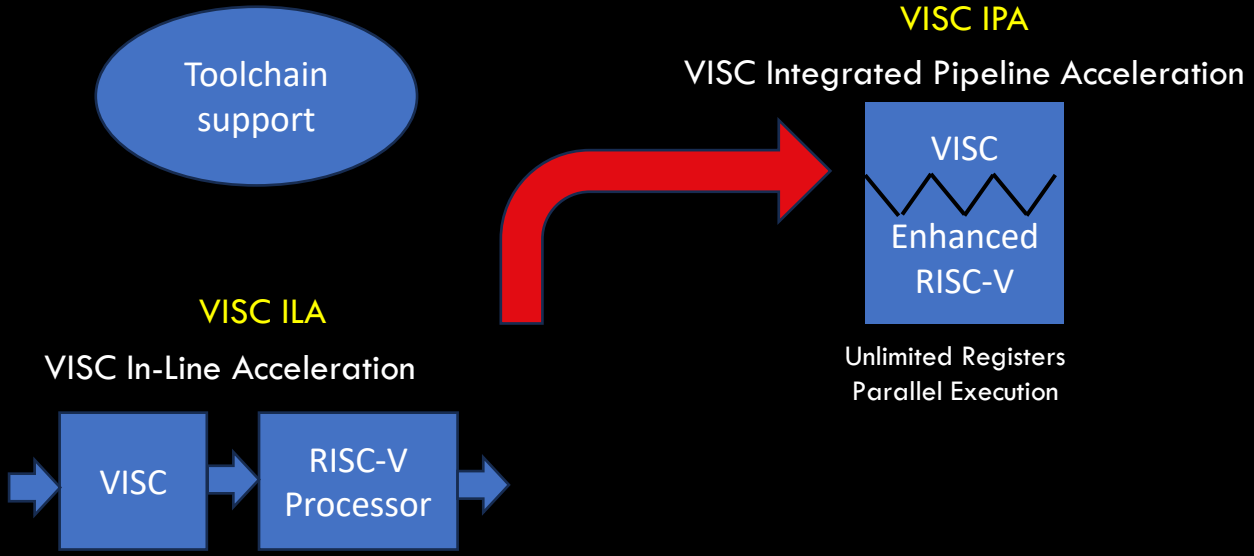


Development Phase	VISC Accelerator Front-end		VISC Integrated into CPU core	
Timescale	NOW	2025/6	2026	2027/28
	MVP (Basic VISC features)	Enhanced VISC features	Extended Registers in RISC-V core	Parallel execute Units in RISC-V core + additional VISC features
Run-time Performance Multiplier for design phase	4-10x	5-10x	2-5x	Unlimited by architecture
Total Run-Time Performance Multiplier	**5-10x**	**25-100x**	**50-500x**	**Unlimited**

VISC enables RISC-V core developers to add symbiotic features for optimal performance

VISC Roadmap and optionality



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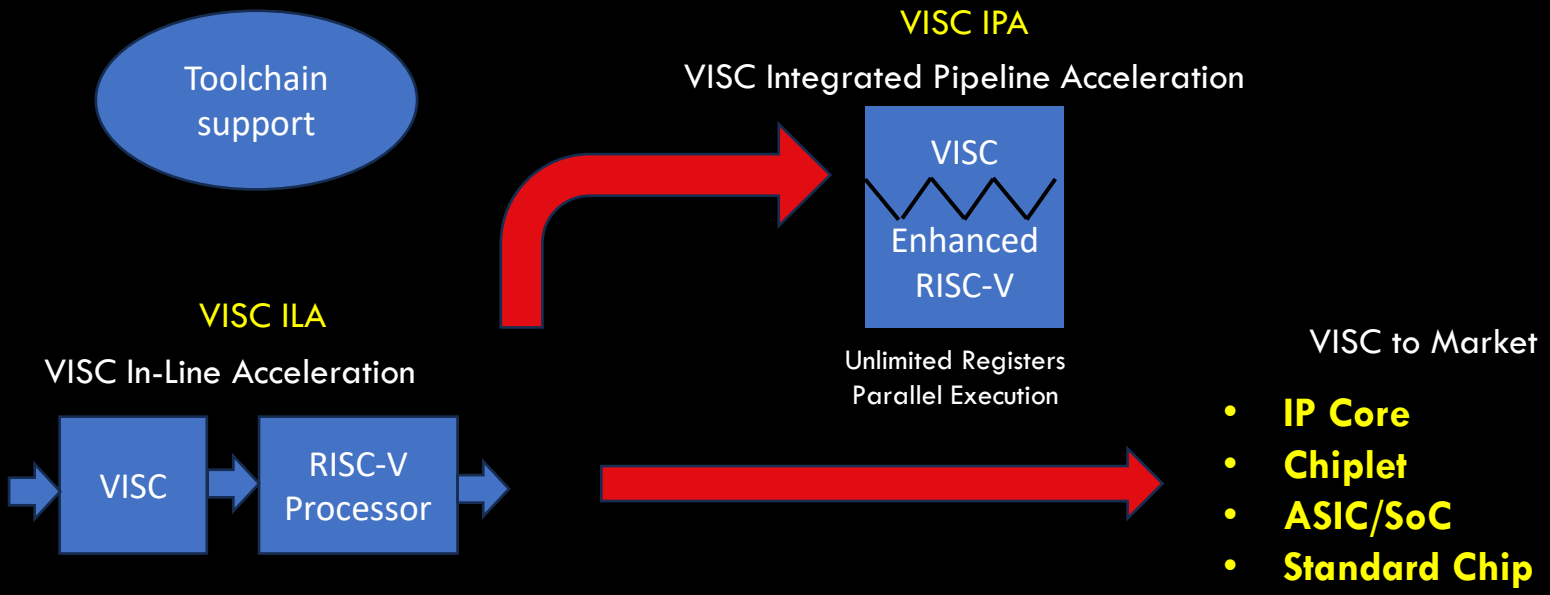

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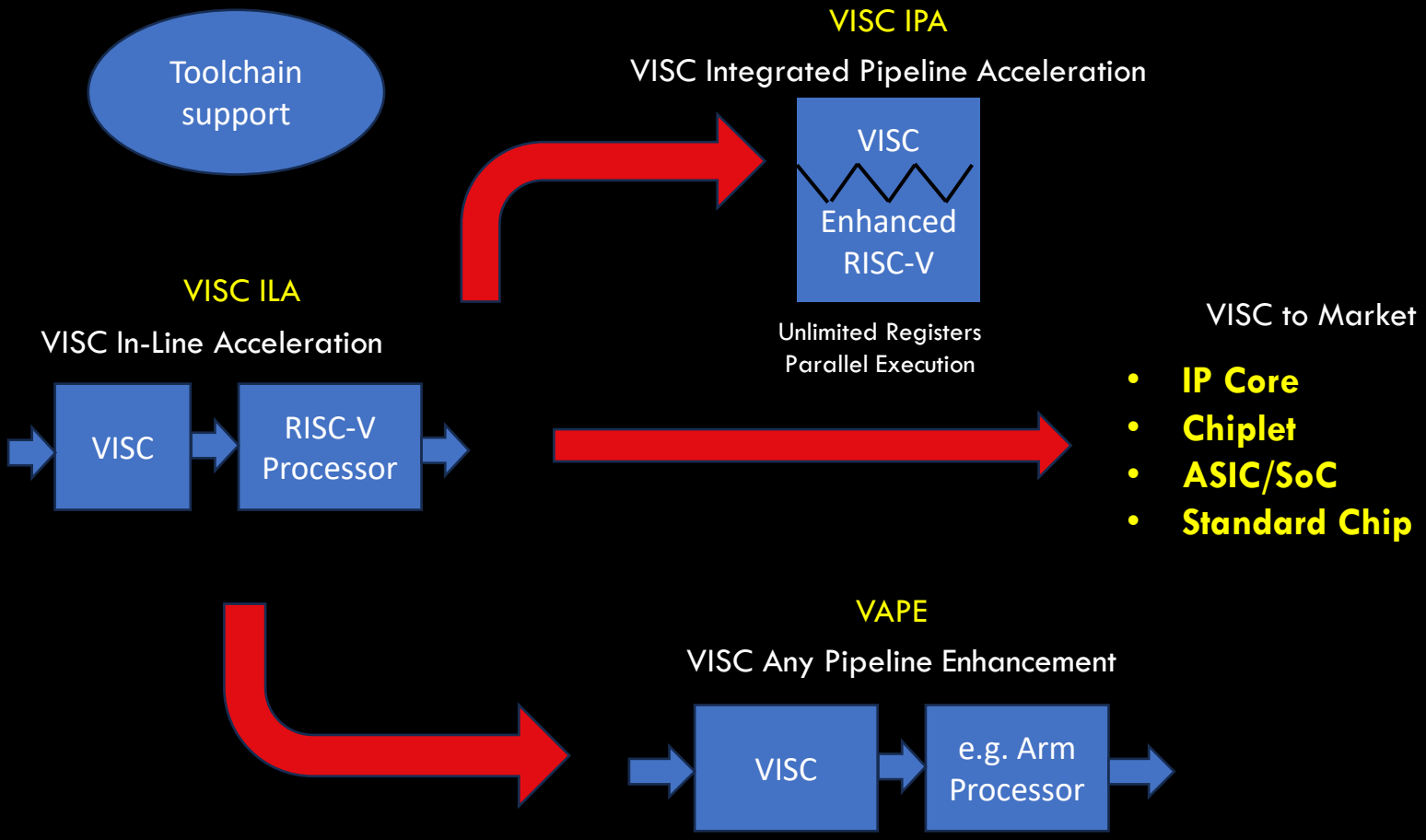

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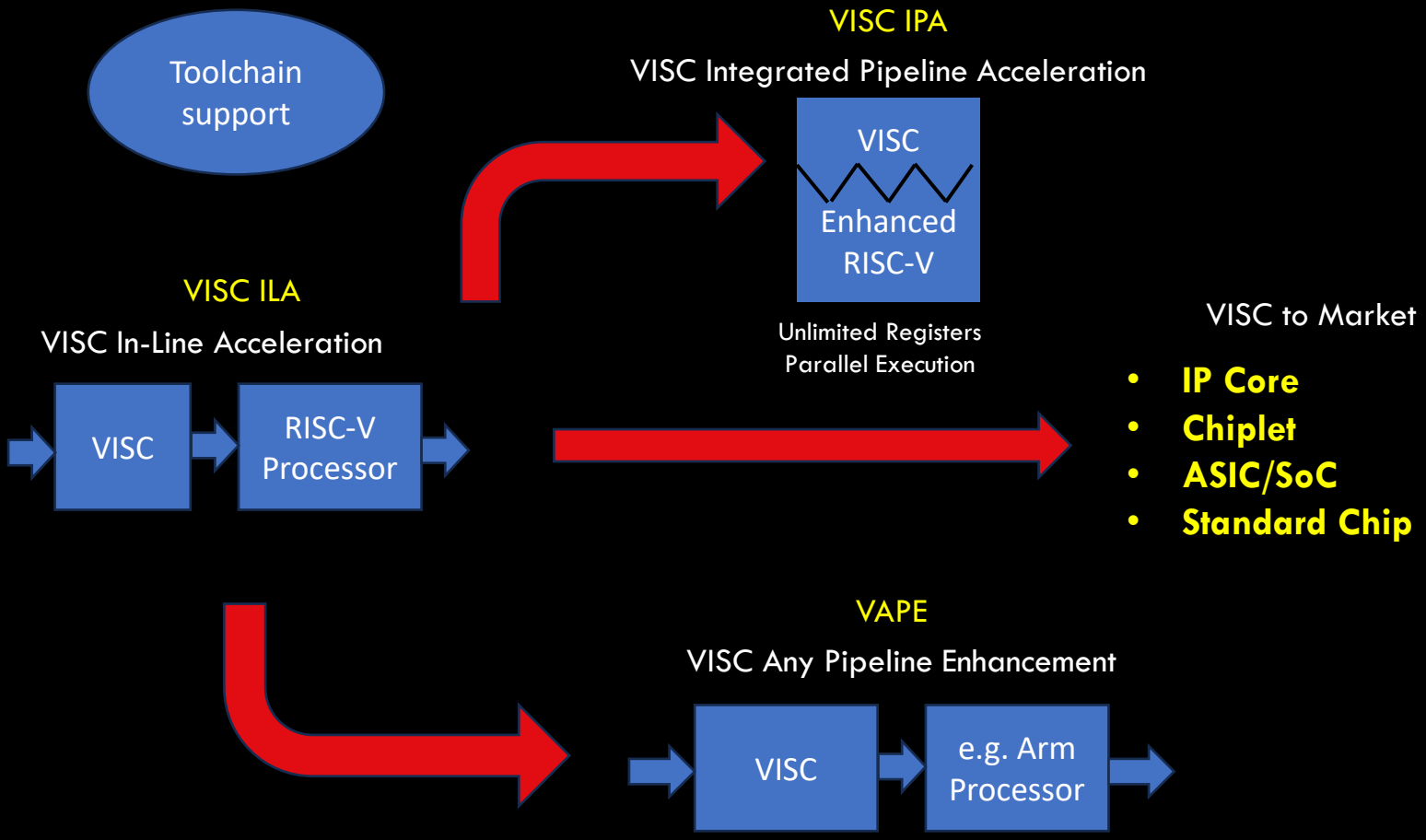

Versatility in Toolchain => Alignment with Industry Standard Tools and Customer Workflow

VISC case study – Health-tech

Blood cell labeling and analysis for cancer detection and therapy

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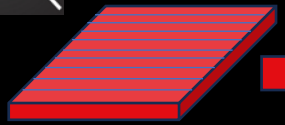
Lead customer application in development now…

Blood sample - >10 billion cells

Microfluidics sensors



Electrical and optical detection techniques (developed by partner)

Signal Conditioning

ADC

Massive noisy Data set IN

10-50 target cells must be identified/labeled

VISC - AI

- Multiple channels/parallel processing
- Error detection/correction
- Pattern detection/Anomaly rejection
- Needle-in-haystack artefact finding
- Real-time diagnostics/therapeutics
- Early FPGA development:
  - Algorithm refinement
  - Functional verification
  - Execution speed assessment
- 1st training model for cancer therapeutics; subsequent training models for other diseases/conditions

Objective outcome:

VISC-based product:

- **Fast to market**
- **Diagnoses made**
- **Therapies optimised**
- **Lives saved**

R&D Project funded by:

UKRI UK Research and Innovation

Lessons learnt and applied

- Don't let back-end verification concerns stifle front-end innovation
- Align innovation with market need, not incumbent trend
- Focus first on functional verification
- Design-in get-outs for unanticipated bugs, and timing
- Re-focus on timing verification when technology gets close to customer adoption
- Partnerships are key – Product/Market Fit; Design flow; Layout and Verification; silicon testing, application code development
- Startups can impact the domains of long-term incumbents with innovative thinking (innovate technology, and business model)
- VISC will positively impact AI and Edge processing

RED semiconductor

VISC

Versatile Intrinsic Structured Computing

The Powerful RISC-V AI CPU and Maths Accelerator

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