An AI-Assisted Connection Weight Prediction for Regression Testing of Integrated Circuits

Author(s): **Abishaan Ravikumar[1], Xiaohan Yang[2], Rajendra Prasad[2], Alexander Rast[1] & Abusaleh Jabir[1]**

[1]Oxford Brookes University, Oxford, United Kingdom
[2]Infineon Technologies, Bristol, United Kingdom

Speaker: **Abishaan Ravikumar**
Advanced Reliable Computer Systems Group
School of Engineering, Computing, and Mathematics
Oxford Brookes University, UK

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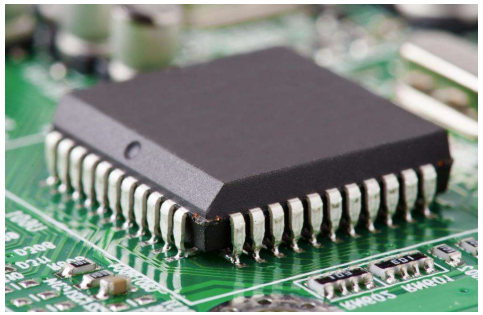
MOTIVATION

- Integrated Circuits (ICs) combine logic and electronic components in a single unit to perform programmed functions.
- IC verification is the activity that determines the correctness of the design.
- IC verification is extremely resource-intensive.
- Costs of tests and verifications are significantly increasing with increased design complexity.
- As a result, in a highly complex system it is not possible to tests the entire design with the test set each time any modification is made to the design.
- For this we need **Regression Testing**!



MOTIVATION (CONT)

> *In 1994, the Pentium FDIV bug occurred due to an error in Intel's division algorithm (FPU), causing incorrect results in specific cases. Intel missed this in their testing, leading to a costly chip replacement process of about $475 million.* *

- Early and timely bug detection in ICs — ensures its functional correctness, design reliability, and quality.
- The complexity of integrated circuit design is determined by factors such as transistor count, functionality, interconnect density, and design architecture.

* Encyclopedia Pub. "The Intel Pentium FDIV Bug." *Encyclopedia Pub*, https://encyclopedia.pub/entry/32969#:~:text=This%20flaw%20in%20the%20Pentium,about%2061%20parts%20per%20million. Accessed 6 Oct. 2024.

WHAT THE CLIENT GETS

TriCore™ architecture

TriCore™ architecture overview and key features

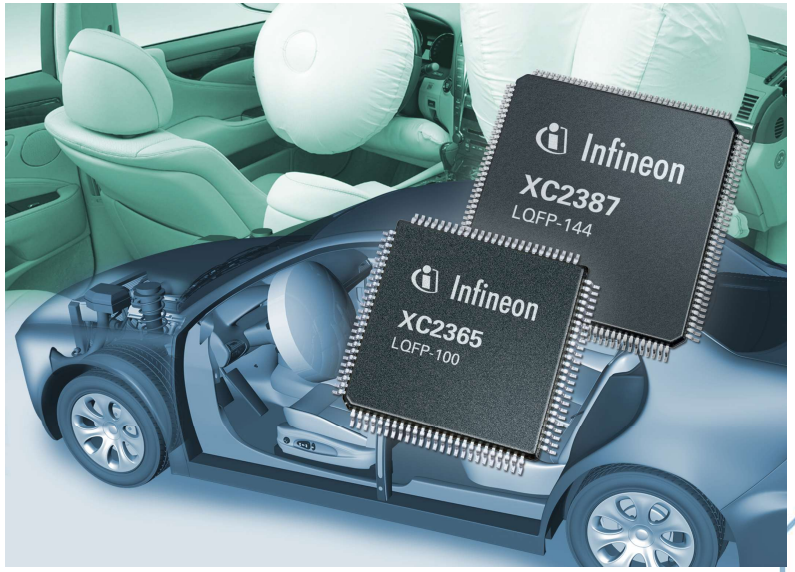
TriCore™ is the first unified, single-core, 32-bit microcontroller DSP architecture optimized for real-time embedded systems. TriCore™ Instruction Set Architecture (ISA) combines the real-time capability of a microcontroller, computational power of a DSP, and high performance/price features of a RISC load or store architecture in a compact re-programmable core.

The architecture supports both 16-bit and 32-bit instruction formats.

Key features of TriCore™ ISA:

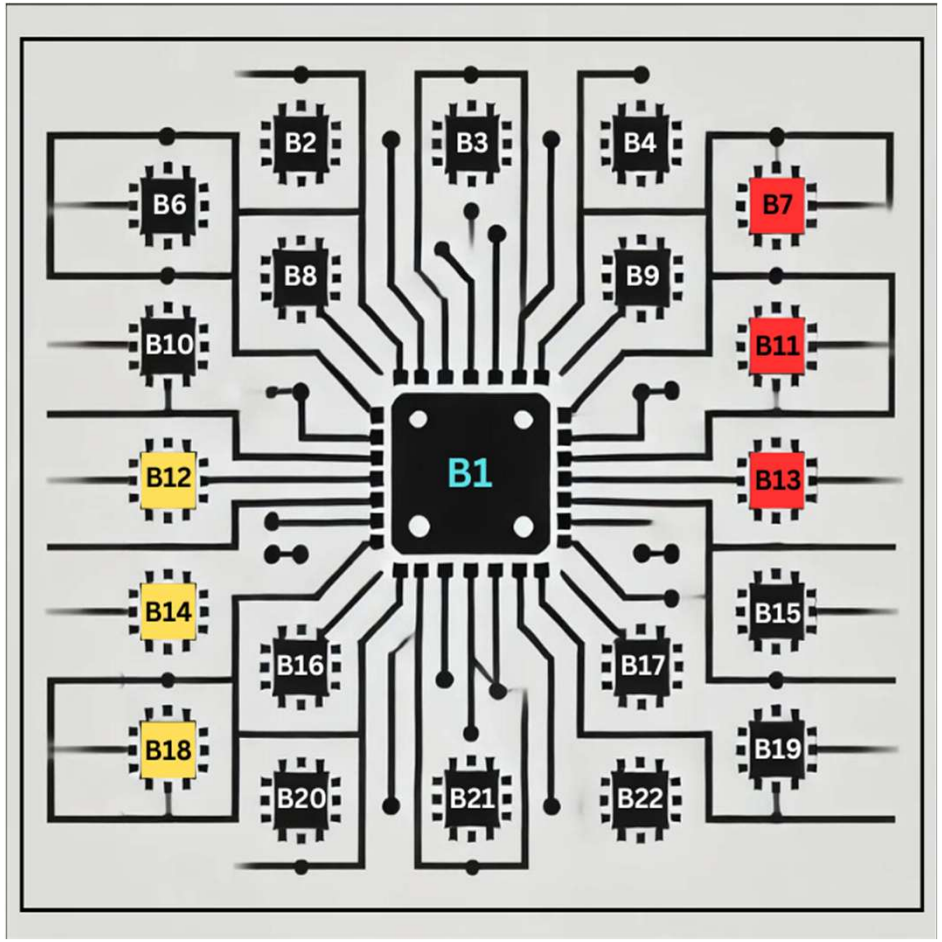
- 4 GB of address space
- 16-/32-bit instructions for reduced code size
- Branch instructions (using branch prediction)
- Low interrupt latency with fast automatic content switch using wide pathway to on-chip memory
- Zero overhead loop capabilities
- Dual, single-clock-cycle, 16x 16-bit multiply-accumulate unit (with optional saturation)
- Optional Floating-Point Unit (FPU) and Memory Management Unit (MMU)
- Extensive bit-handling capabilities
- Single Instruction Multiple Data (SIMD) packed data operations (2x 16-bit or 4x 8-bit operands)
- Flexible interrupt prioritization scheme
- Byte and bit addressing
- Memory protection and debug support

Explore how TriCore™ is the ideal platform for automotive applications.



https://www.infineon.com/cms/en/product/microcontroller/32-bit-tricore-microcontroller/?term=tricore&view=kwr&intc=searchkwr*

A PRACTICAL DESIGN



Modified Blocks under test.

Blocks connected to blocks under test.

THE CHALLENGE

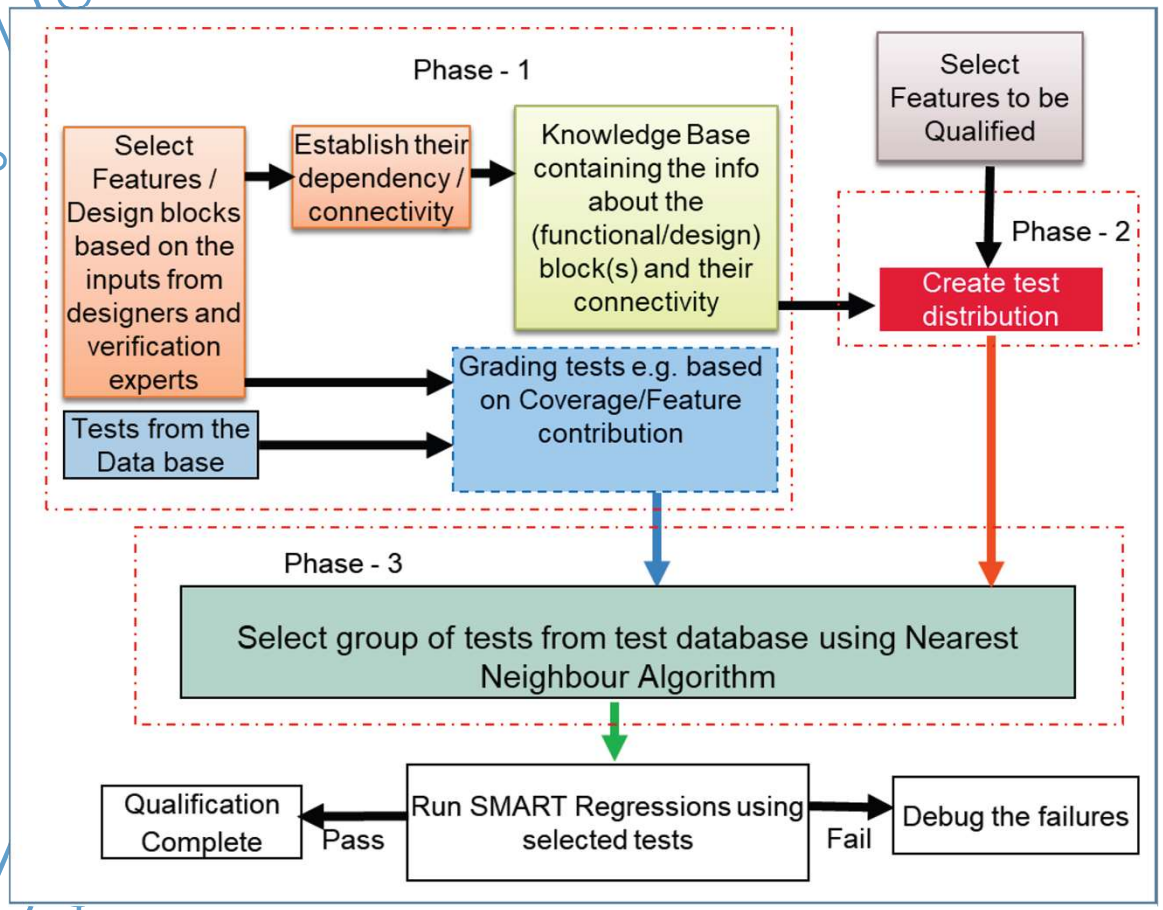
- Verifying IC designs involves subjecting millions of test scenarios, depending on complexity.
- How do we select a small number of tests from a very large test pool for very fast targeted testing of the design changes ?

RELATED WORK

- Simulation-based verification provides a robust framework for testing designs across diverse scenarios*.
- Regression Testing verifies circuits incrementally, focusing on sections of the circuit that have been modified or undergone design changes.

* Y. Li, W. Wu, L. Hou, and H. Cheng, “A study on the assertion-based verification of digital ic,” in 2009 Second International Conference onInformation and Computing Science, vol. 2, 2009, pp. 25–28

SMART REGRESSION TESTING



- SMART regression leverages the Nearest Neighbours algorithm for test selection.
- Test selection based on geographical closeness between design blocks.
- It requires accurate measure of connection strength between interconnected blocks known as “connection weights.”
- We propose an AI assisted method for predicting connection weights between design blocks.

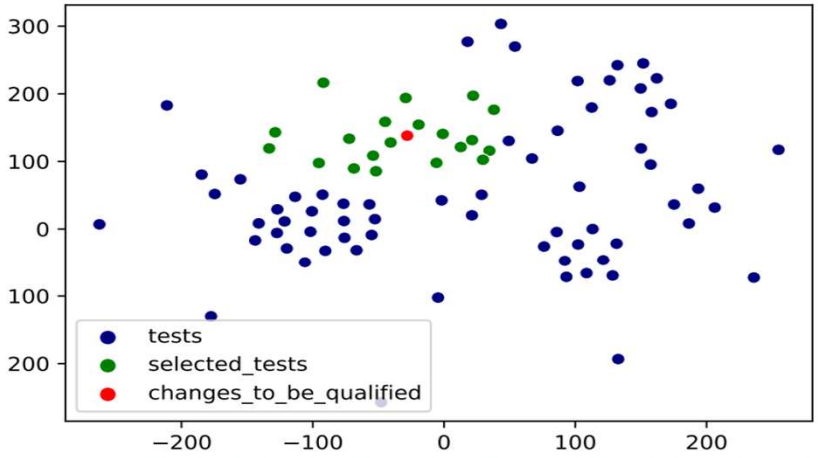
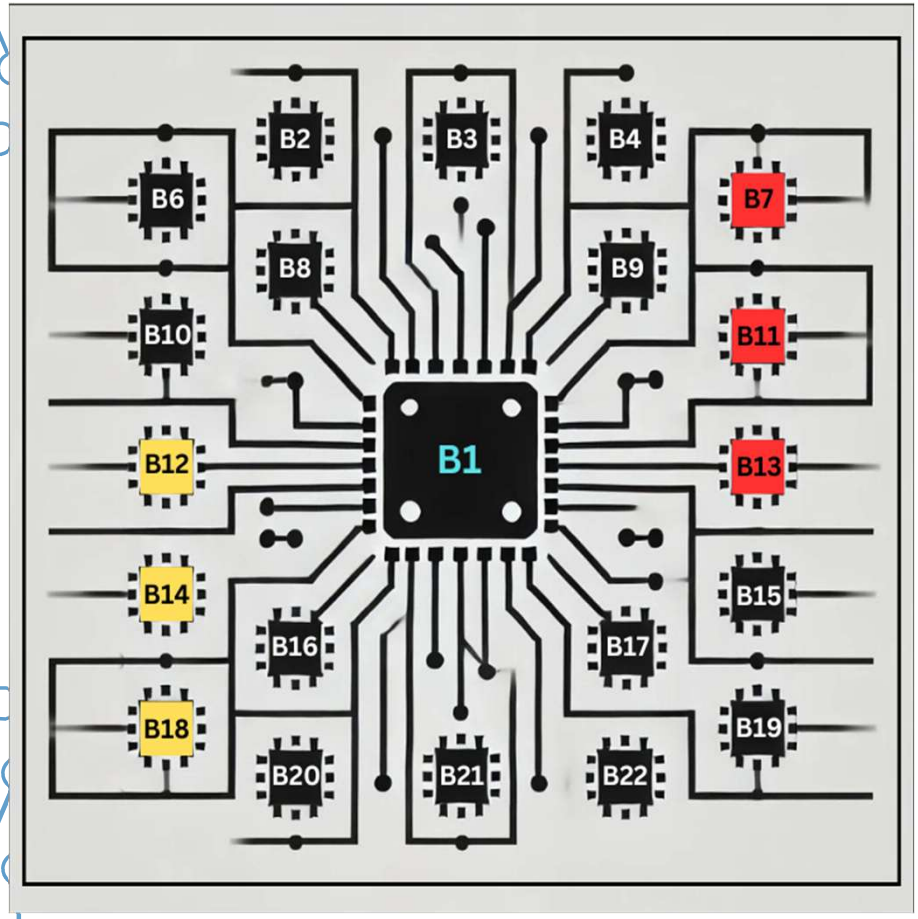


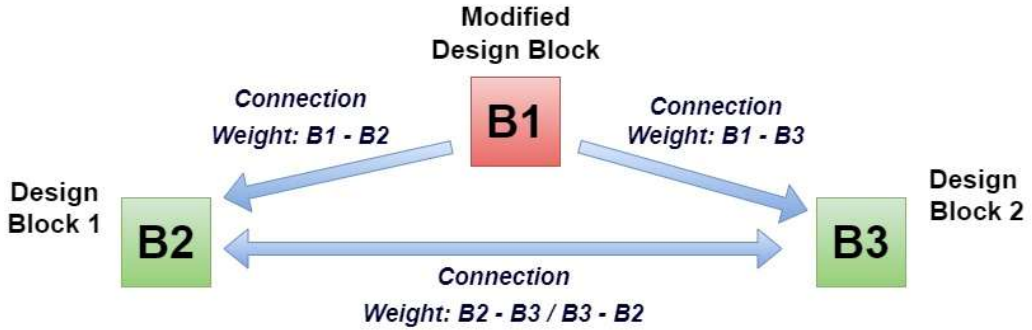
Fig. 2: Tests Selection Based on Nearest Neighbour Algorithm from the tests mapped in multi-dimensional space

TEST SCENARIO & CONNECTION WEIGHT



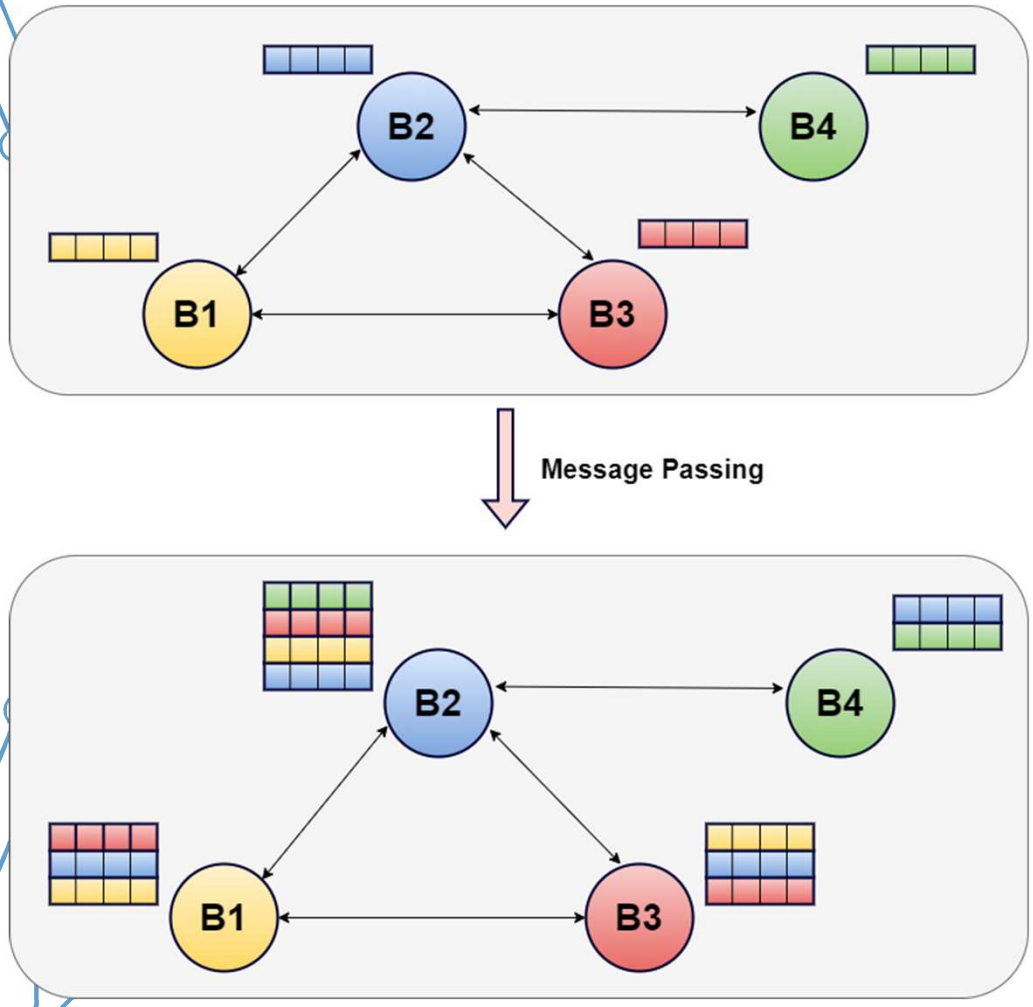
Blocks under test.

Blocks connected to blocks under test.



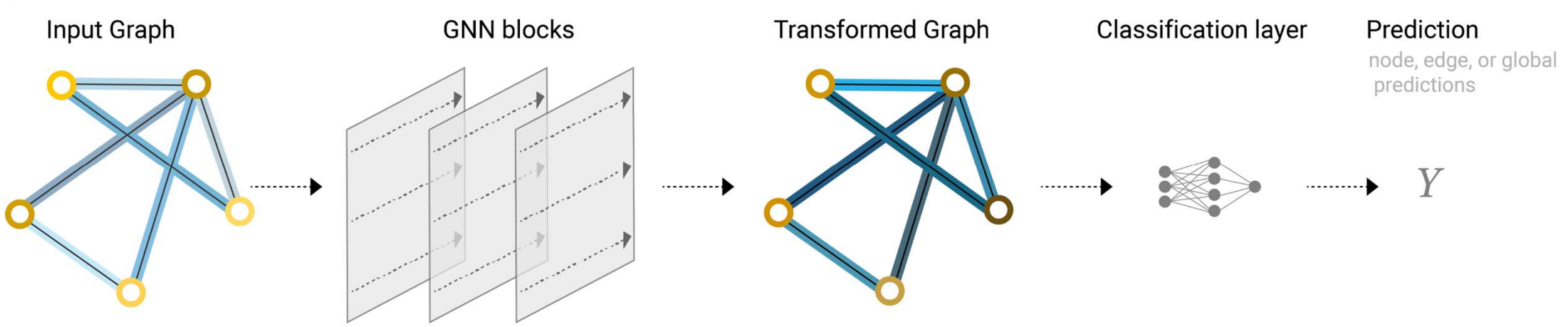
- For a regression test scenario, the tests need to be distributed within all the connected blocks.
- Test distributions are influenced by "*connection weights.*"
- Connection weights lie between **0** and **1**.

GRAPH NEURAL NETWORK FOR WEIGHT PREDICTION

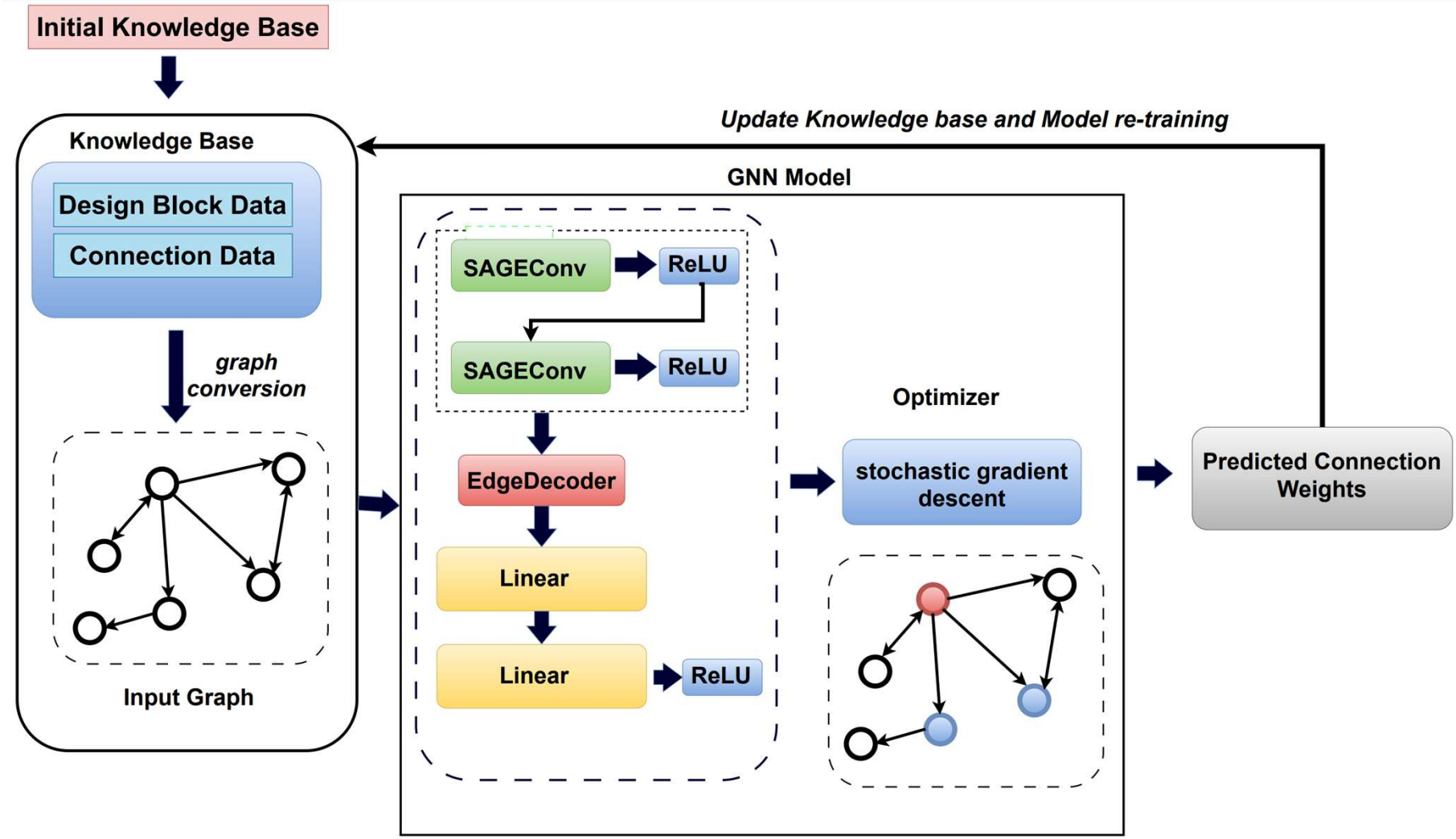


- GNN operates on graph data structures.
- The novel approach replaces the manual method of updating the knowledge bases for regression testing.
- The message-passing neural network collects features from adjacent nodes to improve node representation within the graph.

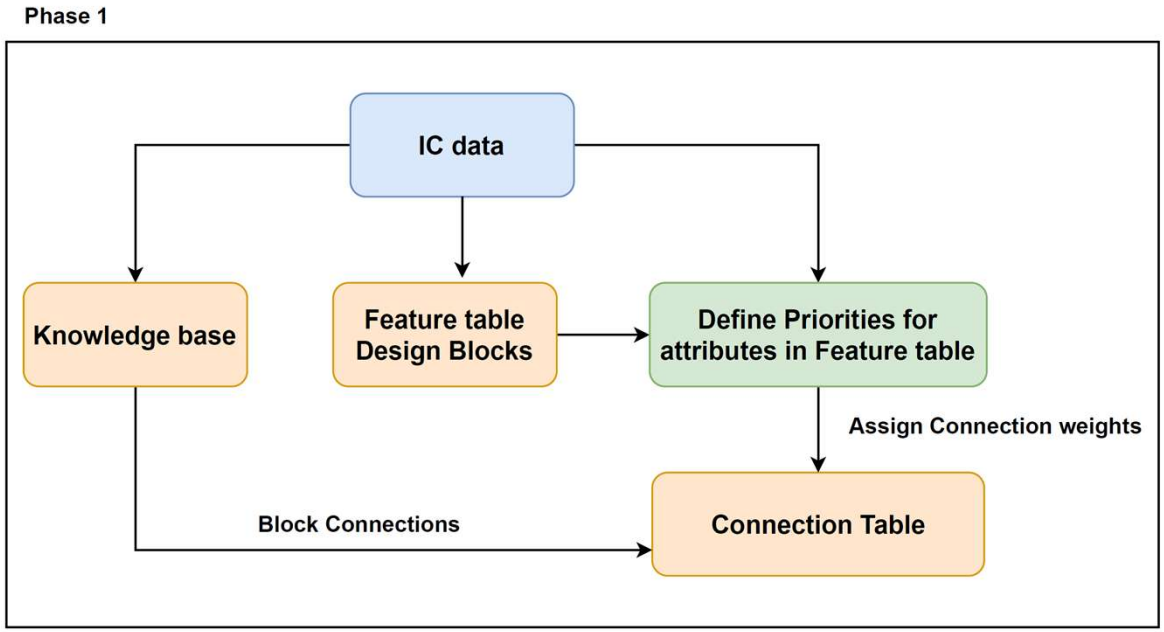
PROPOSED APPROACH FOR WEIGHT PREDICTION



PROPOSED APPROACH FOR WEIGHT PREDICTION



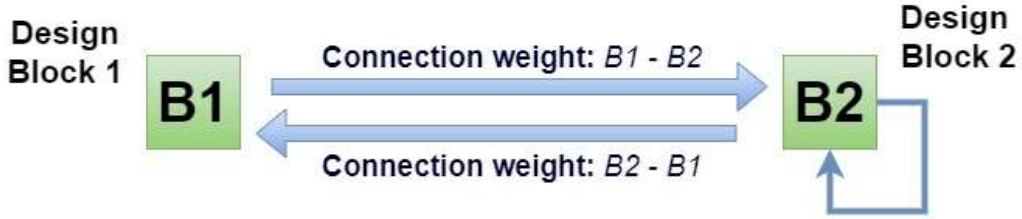
DATA PREPARATION FOR TRAINING & VALIDATION



- The objective is to create feature table and establish connections for the IC design under test.
- This is then used to train the GNN model which predicts the connection weights for test selection.

ATTRIBUTES FOR CONNECTION WEIGHT PREDICTION

- The number of incoming and outgoing connections.
- The number of cover points. i.e. critical points in a design that's need to be tested.
- Whether a block is self-contained or not, shows the existence of connection to itself.
- Block's intrinsic weight, indicating its priority with respect to the rest of the connected blocks.



$\{ \quad CP \qquad SF \qquad In \quad Out \qquad IW \ \}$

Blocks	Cover points	Self-Contained	In	Out	Intrinsic weight
B1	78	0	6	10	0.64
B2	450	1	4	6	0.50

PRIORITY OF FEATURE TABLE ATTRIBUTES

	$\{ CP_P$	SF_P	In_P	Out_P	$IW_P \}$
Attributes	Cover points	Self-Contained	In	Out	I.weight
Priority %	20%	25%	10%	30%	15%

"Determine priority score (PS) of each block based on the following equation."

$$PS = \frac{CP \cdot CP_P + SF \cdot SF_P}{100} + \frac{In \cdot In_P + Out \cdot Out_P + IW \cdot IW_P}{100}$$

Blocks	Priority Score (PS)
B1	7.84
B2	4.59
B3	2.41
B4	6.26

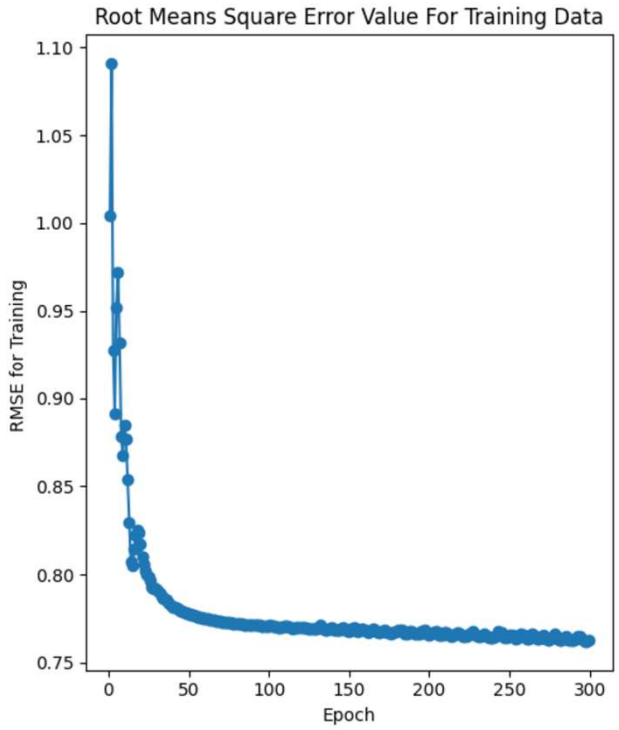
CONNECTION WEIGHT DERIVATION

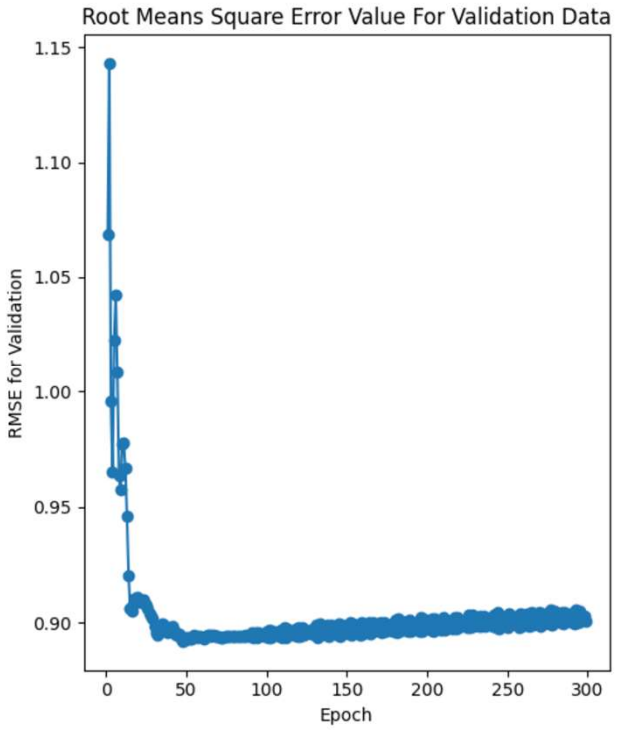
$$C_W = \frac{PS_{SB}}{L \cdot (PS_{SB} + PS_{TB})}.$$

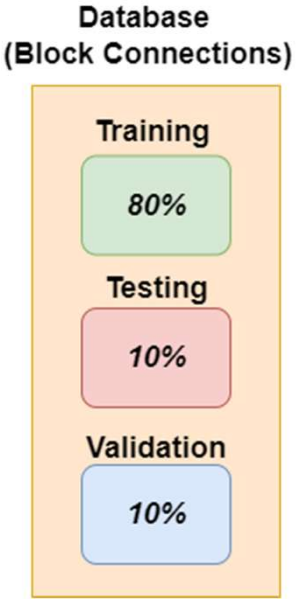
$\{ PS_{SB}$	PS_{TB}	L	$C_W \}$
Source Block	Target Block	Level	Connection Weight
B1	B2	1	0.1740
B1	B3	1	0.2776
...	...	...	...
...	...	...	...
B2	B3	3	0.5517
B3	B2	3	0.9201

MODEL EVALUATION

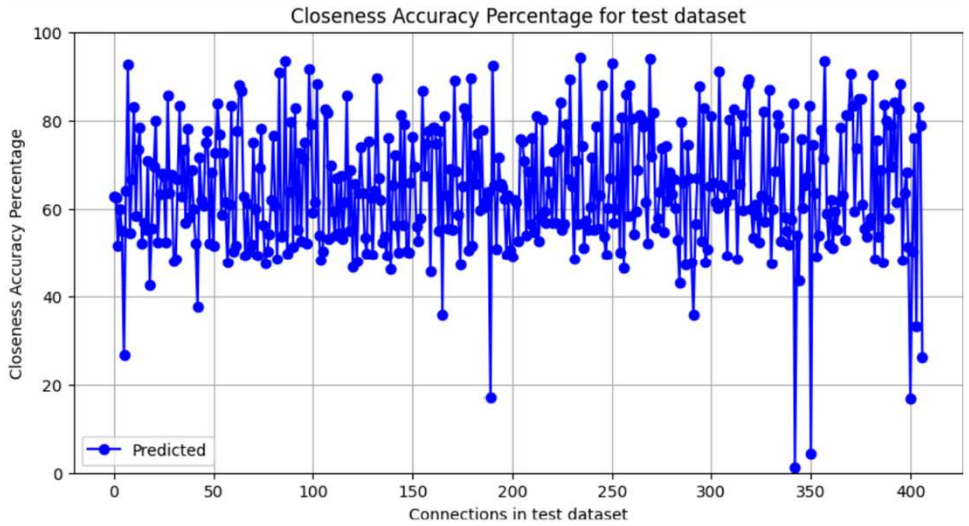
- The model was tested on a ***535K µm²*** design using ***28nm*** technology.
- The design contains FPU, decoder, load/store units, fetch modules, bus interface units, and an ALU, etc.
- A total of ***33K*** test cases were considered, encompassing both good and bad tests.







RESULTS



Code Coverage	BUS Interface Unit (BIU)				
	Full Regression	Rand1	Rand2	Rand3	Proposed
Expression	89.84%	66.10%	71.42%	69.55%	84.75%
Total	94.62%	80.23%	83.48%	79.95%	91.59%

	R.Test Constraint*	Full Reg	Rand Test	SR. Rand W	SR. Proposed
T.Time or Cyc	15,400k	2 Days	50 mins	50 mins	50 mins
No Tests	3k	30k	100	100	100
Coverage %	98%	94%	80%	84%	91%

* S. Sokorac, "Optimizing random test constraints using machine learning algorithms," 2017 Design and Verification Conference and Exhibition US (DVCon), 2017, pp. 583–588.

PUBLICATION

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Abishaan Ravikumar*, Xiaohan Yang†, Rajendra Prasad†, RajaNataraj Sivaraj†, Alexander Rast*, and Abusaleh Jabir*
*School of ECM, Oxford Brookes University, Oxford, UK. E-mail: {19232440, arast, ajabir}@brookes.ac.uk
†Infineon Technologies, Bristol, U.K. Ltd. E-mail:{Xiaohan.Yang, Rajendra.Prasad, RajaNataraj.Sivaraj}@infineon.com

FURTHER RESULTS

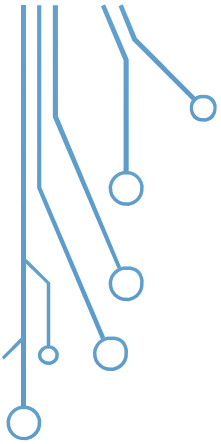
B3	Block Average	Block Covered	Branch Average	Branch Covered	Expression Average	Expression Covered	Toggle Average	Toggle Covered	name
SR 100 tests for B3	92.09%	84.67% (221/261)	90.24%	81.04% (171/211)	89.49%	79.48% (368/463)	41.35%	62.84% (93/148)	i_tc18_idle
Proposed	***98.62%***	***97.32%***	***98.29%***	***96.68%***	***96.02%***	***92.22%***	***96.71%***	***79.73%***	i_tc18_idle
Proposed with Distribution	98.22%	96.55% (252/261)	97.80%	95.73% (202/211)	95.91%	92.01% (426/463)	92.86%	78.72% (116.5/148)	i_tc18_idle

B4	Block Average	Block Covered	Branch Average	Branch Covered	Expression Average	Expression Covered	Toggle Average	Toggle Covered	name
SR 100 tests for B4	75.18%	71.79% (832/1159/79)	71.91%	67.70% (677/1000/69)	73.43%	69.50% (1187/1708/26)	66.56%	75.61% (775/1025)	i_tc18_pmbi
Proposed	89.75%	90.60%	87.85%	89.10%	88.05%	85.83%	93.98%	95.41%	i_tc18_pmbi
Proposed with Distribution	***96.11%***	***96.55% (1119/1159/79)***	***95.39%***	***96.00% (960/1000/69)***	***91.83%***	***90.46% (1545/1708/26)***	***93.74%***	***95.32% (977/1025)***	i_tc18_pmbi

Distribution	38	0.99	Shutdown Trap
	48	0.54	Smart Lockstep
	39	0.47	DLMU
SR Targeted	38	0.97	Shutdown Trap
	48	0.51	Smart Lockstep
	39	0.49	DLMU

CONCLUSIONS

- Our approach is showing noticeable improvements over the random cases, which is quite popular for simulation-based verification.
- Considerable accuracy improvement over a full regression test is also observed, where a full regression test required 27K tests (vs 100 tests) to achieve 89.52% expression coverage (vs 84.75%) over a 2-day run (vs about 50 mins).
- In conclusion, our AI-assisted weight prediction for regression testing shows promising results, and efforts are ongoing to automate other stages of regression testing using AI technology.



THANK YOU FOR YOUR ATTENTION

ANY QUESTIONS ?

DATA ANALYSIS

- We utilised data from custom designs that included design specifications and connection information between design blocks.
    1. Construction of feature table: Refine and organise relevant information to construct a feature table for the design blocks, each represented as nodes in GNN.
    2. Correlated the integrated circuit (IC) design to create a foundational connectivity table.
    3. Reconstruct the connectivity table to include all possible connections between design blocks, accommodating all combinations and permutations of connections.

This approach ensures comprehensive mapping of interconnectivity within the design.