A HERO ELECTRONIX VENTURE

TESSOLVE

Al in Design Verification

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Outline

- Tessolve AI Strategy
- 1: UVM AI Training Tool
- 2: Assertify Tool
- 3: Spec Extraction
- Collaboration Opportunity





Tessolve's Effective AI Strategy

- Models are replaceable
- Maintaining security
- Centre supports innovation at the edge

External tool/ vendor scrutiny



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AI/ML Experiments in IP Verification



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AI Ecosystem

Knowledge Bots:

- Features: Faster to develop & deploy
- Use case: With less confidential data, Project CoPilot
- Security: Low
- Cost: Low,
- Reasonable accuracy
- **Project:** UVM Chatbot, Automotive FUSA Assistant

Clouds

- Feature: Faster develop & deploy
- Use case: Client projects, highly confidential data.
- Security: High
- Cost: High

Local

- Features: Slower to develop & slower to deploy
- Use case: For highly confidential data
- Security: High
- Cost: High
- Challenge: Less Adaptability, less Scalability, Upfront Cost

AI Apps

•DV Spec Analysis Tool

- DV AI TB Tool
- •Assertify Tool
- •Code converters (e.g. SV to Cocotb code converters)
- Domain/ Project based
- AI models & applications
- PDK AI Training Tool
- •UVM Training Tools
- •Al Code Copilot

1: UVM AI Training Tool

Organized Content

• Follows planned flow

Quick Topics

• Most important topics' explanation

MCQs

•Test, Evaluation, weak concept suggestions

FAQs

• Clarifies on common important doubts

Q&A

•ANY question support

About

• Tool briefing for effective use

Dashboards

•Analytics, time spent, evaluation results

Benefits:

- Self guided and self paced flow
- Analytics & custom topic suggestions
- Ask anything about UVM
- Improved accessibility
- Reduced training time
- Scalable for other domains



1: UVM AI Training Tool





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Tessolve UVM AI Training Tool

🗭 Q&A Chat



Explain UVM Sequencer please!

UVM Sequencer

Introduction

In Universal Verification Methodology (UVM), the sequencer is a key component responsible for controlling the flor sequences that generate complex stimulus and the drivers that convert these stimuli into pin-level activities.

Role of the Sequencer

🖋 Developed by AI CoE team

1: UVM AI Training Tool





Tessolve UVM AI Training Tool

Generate MCQs

Select a topic

UVM Components

MCQs for UVM Components:

Question 1: What is the primary class from which the uvm_component class inherits?

Select an option:

- (A) uvm_report_object
- (B) uvm_sequence
- (C) uvm_driver
- (D) uvm_monitor

Question 2: Which of the following uvm_component classes encapsulates sub-components for sequence communication with the uvm_driver?

Select an option:

(A) uvm subscriber

💋 Developed by AI CoE team

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Problems around Assertions are:

| Growing Complexity in Verification

| Human Errors

| Time intensive asks | Lack of Consistency and Skill Gap

Use case:

- 1. Generate Assertions from spec/ engineer's simple description using AI models.
- 2. Generate description from the SVA code.





pload TOP Level PDF File:	0			
Drag and drop file here Limit 1GB per file • PDF				
Browse files		English to SystemVerilog Assertion		
		Enter Description	③ SystemVerilog Assertion Code	0
			Convert to SVA Code	
		SystemVerilog Assertion to English		
		SystemVerilog Assertion Code	O Code Description	0
			Convert to English	
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Tool 2: Assertify Tool - Signal match analysis

#	Approach	Top signal	Assertify tool input english description signal	Signal in generated SVA	
1	Case mismatch	axi_awvalid	AXI_AWVALID	axi_awvalid	
	Case mismateri	axi_awready	AXI_AWREADY	axi_awready	
2	Additional character	axi_awvalid	AXIVALID	axi_awvalid	
		axi_awready	AXIREADY	axi_awready	
3	Partial match	axi_awvalid	AXIVLD	axi_awvalid	
	r ai tiai match	axi_awready	AXIRD	axi_awready	
Λ	Dartial match	axi_awvalid	valid	axi_awvalid	
4	Faltial Match	axi_awready	ready	axi_awready	
5	Highly mismatch	axi_awvalid	VLD	axi_awvalid	
	i ligiliy iliisilatti	axi_awready	RDY	axi_awready	



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SystemVerilog Assertion to English

SystemVerilog Assertion Code	
sustamuarilag	
systemveniog	
property awvalid_protocol;	
<pre>@(posedge clk) disable iff (!rst_n)</pre>	
axi_awvalid -> ##[1:\$] axi_awready;	
endproperty	

assert property (awvalid_protocol);

Convert to English

?

Code Description

The SystemVerilog assertion `awvalid_protocol` checks that whenever the `axi_awvalid` signal is asserted (indicating that the write address is valid), the `axi_awready` signal must be asserted at some point in the future, ensuring that the write address handshake is completed. This must hold true on every positive edge of the `clk` signal, provided the `rst_n` signal is not asserted (i.e., the system is not in reset).

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Tool 3: Spec Extraction Tool

• RAG (Retrieval Augmented Generation) **Tool for DV Spec Extraction**

Model

- Inputs: Project Spec, Training Data,
- Prompt (Character)
- User Prompt
- LLM Intelligence
- Output



Spec PDF

Review

Flow

Tool 3: Spec Extraction Tool





Extraction Process



Tessolve Chatbot v6.0

please generate detailed AXI4 feature list with different bus channels, unaligned data transfers, burst based transactions with more details on burst type, burst size and length from the uploaded pdf

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Detailed AXI4 Feature List

1. AXI4 Bus Channels

The AXI4 protocol defines several independent transaction channels to facilitate high-performance and high-frequency system designs. These channels are:

- Read Address Channel: Carries control information describing the nature of the data to be transferred for read operations.
- Read Data Channel: Transfers data from the slave to the master during read operations.
- Write Address Channel: Carries control information describing the nature of the data to be transferred for write operations.
- Write Data Channel: Transfers data from the master to the slave during write operations.
- Write Response Channel: Signals the completion of the write transfer from the slave to the master.

These channels allow for the separation of address/control and data phases, which helps in achieving high-frequency operation without using complex bridges.

2. Unaligned Data Transfers

The AXI protocol supports unaligned data transfers using byte strobes. This feature is crucial for accessing mixed-endian data structures in a single memory space. The protocol uses a byte-invariant endianness scheme, which ensures that any multi-byte element in a data structure:

- Uses the same continuous bytes of memory, regardless of the endianness of the data.
- The order of bytes in memory is determined by the endianness, indicating whether the first byte in memory is the most significant byte (MSB) or the least significant byte (LSB) of the element.
- Any byte transfer to a given address passes the eight bits of data on the same data bus wires to the same address location, regardless of the endianness of any data element.

3. Burst-Based Transactions

The AXI protocol is burst-based and defines three burst types:

- Fixed Burst: The address remains constant for every transfer in the burst.
- Incrementing Burst (INCR): The address increments by the size of the transfer for each transfer in the burst.
- Wrapping Burst: The address increments like an incrementing burst but wraps around to a lower address when a wrap boundary is reached.

Burst Size

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RAG

Assessment

RAG Assessment

• Manual validation The generated content is manually validated by the engineers and tagged with *confidence score* (How satisfied they are with the response?)

• RAG Pipeline Assessment



RAG Assessment

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question	answer	contexts	ground_truth	faithfulness	answer_relevancy	context_recall	context_precision
What role do integrated circuits (ICs) play in	Integrated circuits (ICs) are used in virtuall	[Applications in Electronics\nThe ability to c	Integrated circuits (ICs) are fundamental buil	1.000000	0.946481	1.00	1.0
What are the potential future developments in 	The future of semiconductors will likely invol	[Future Directions\nThe future of semiconducto	The future of semiconductors is poised for exc	1.000000	0.992269	1.00	1.0
How does Moore's Law relate to the development	Moore's Law predicts that the number of transi	[The Role in Technological Advancement\nThe co	Moore's Law predicts that the number of transi	0.833333	0.936722	1.00	1.0



Collaboration with DV Flow

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Collaboration with AI Research





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THANK YOU



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Test



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Chip Engineering Design

Hardware Design



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