Verification Futures Conference 2023 US

Hybrid Architecture Validation

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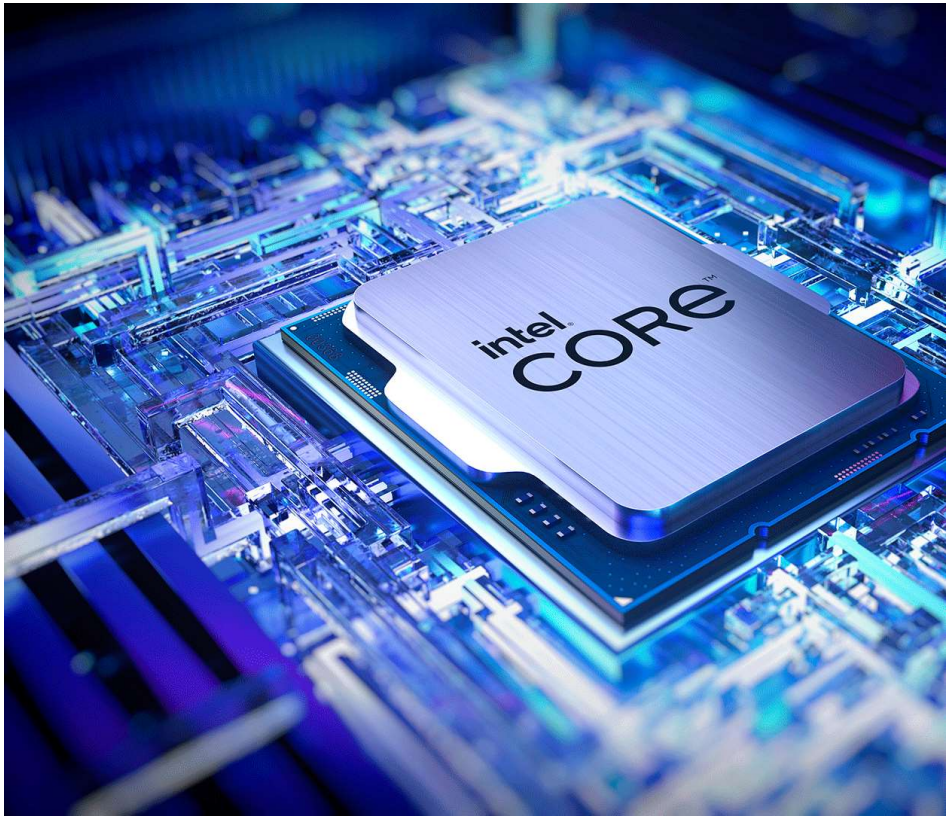
Agenda

- Introduction to Intel Hybrid architecture
- Pre-Silicon challenges and solutions
- Post Silicon functional validation methodologies
- OS Based Verification
- Functional Validation Sign Off



Intel Performance Hybrid Architecture[1][2]

Designed to deliver efficient high-compute performance in a large dynamic power and performance range

Performance-cores

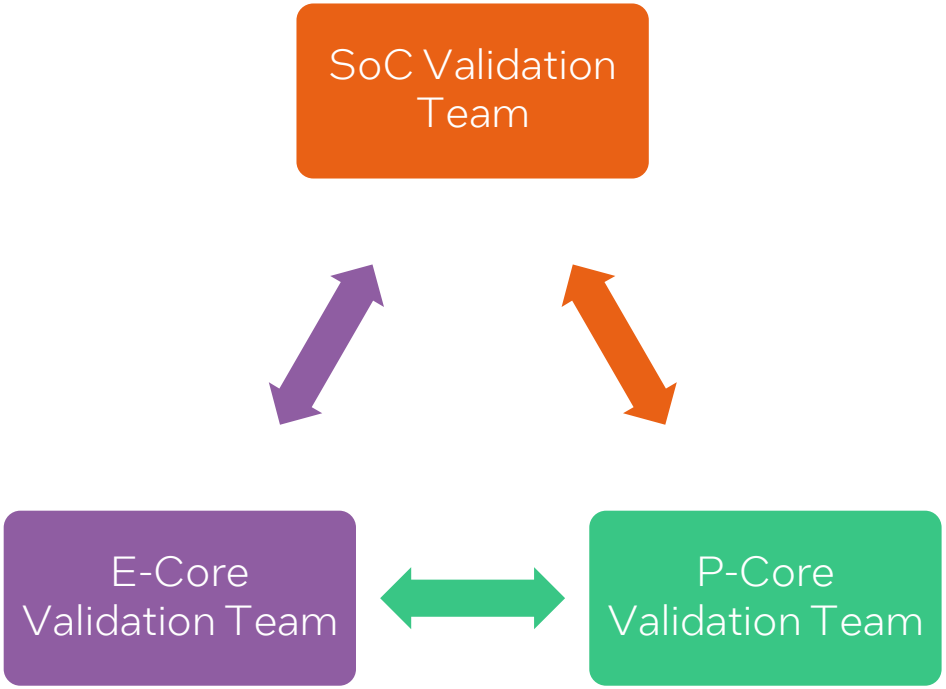
- Larger, high-performance cores designed for speed while maintaining efficiency.
- Tuned for high IPC (instructions per cycle) and high turbo frequencies.
- Supports hyper-threading

Efficient-cores

- Smaller, with multiple E-cores fitting into the physical space of one P-core.
- Designed to maximize CPU efficiency, measured as performance-per-watt.
- Ideal for scalable, multi-threaded performance. Does not support hyper-threading

Pre-Silicon Verification

- 3-prong approach
- Each CPU team performs dedicated IP validation (Simulation, Emulation & FPGA environments)
- SoC validation team performs
  - Integration
  - Hybrid Validation
- Periodic, Consistent check-ins between each Core and the SoC



IP Validation teams (E-core and P-core)

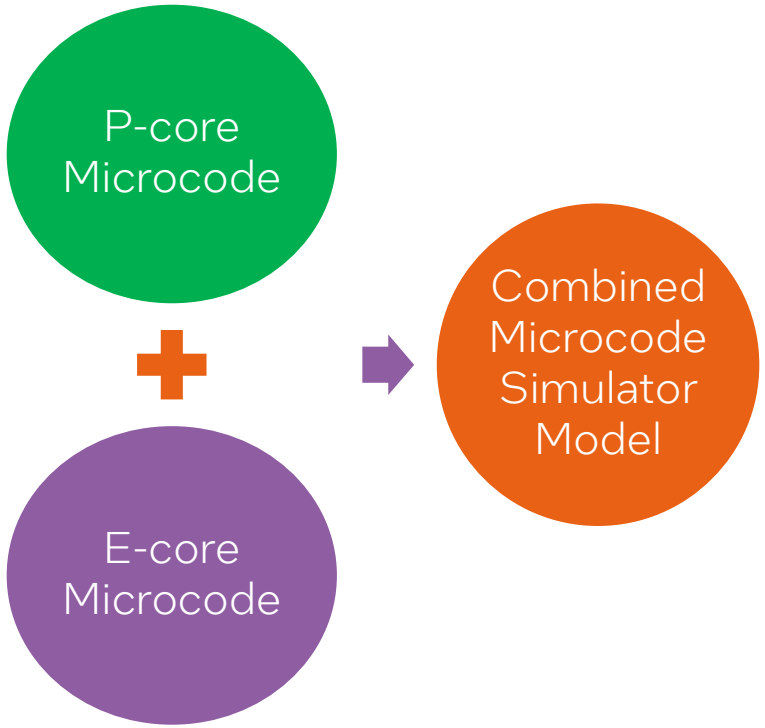
- Experts in their uArch
- Validate their IP in isolation
- Support SoC / Hybrid / Integration Debug

SoC Validation team

- Validate Hybrid Integration
- Run Hybrid Workloads
- Verify Key Performance indicators
- Coordinate debug with the appropriate IP team

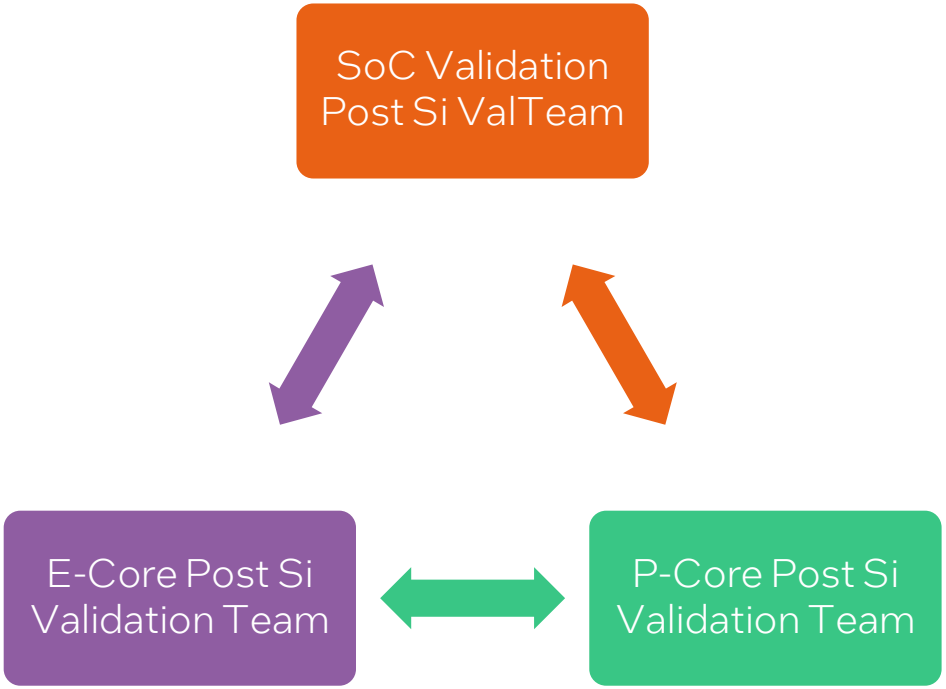
Extensive Pre-Silicon Microcode Validation

- Built a combined Microcode simulator model.
- Allows validation of interaction before Simulation/Emulation models are built
- Faster turnaround of short experiments for validation



Post Silicon Validation

- Similar approach to Pre Si val
- Each CPU team performs dedicated IP validation
- SoC validation team performs
  - Integration
  - Hybrid Validation
- Periodic, Consistent check-ins between each core family and the SoC



OS Based Verification

What if Synthetic Workloads are not stressful enough?

- External Software may have corner case behaviors that are not always modelled.
- External Software may do things that are not completely to ‘spec’
- Need to see how random task switching might behave

1. Analyzed Open-Source OS scheduler source code for task switching
2. Ran Task Switching OS Scheduler code on the combined microcode simulator model to understand the behavior
3. Built a randomized OS task switcher for Post Silicon validation

Functional Validation Sign off

Pre-Silicon

- Pass rates for synthetic test content.
- All failures accounted for, understood and dispositioned
- Coverage data analysis complete.
- Power and Perf data collected, analyzed and within expected ranges.

Post Silicon

- Acceptable pass rates for synthetic test content
- All failures accounted for, understood and dispositioned
- Power and Performance data meeting projections
- 100% pass rate for the OS task switching tests.
- Thread Director working as expected

References and Additional Resources

[1] E. Rotem et al., "Intel Alder Lake CPU Architectures," in IEEE Micro, vol. 42, no. 3, pp. 13-19, 1 May-June 2022, doi: 10.1109/MM.2022.3164338.

[2] How 13th Gen Intel® Core™ Processors Work: https://www.intel.com/content/www/us/en/gaming/resources/how-hybrid-design-works.html

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Gracemont (E-Core)	"Efficient-core - Architecture Day 2021" YouTube, 19-Aug-2021. [Online]. Available: https://youtu.be/agUwkj1qTCs [Accessed: 16-Jul-2023]
GoldenCove (P-Core)	"Meet Performance-Core - Architecture Day 2021," YouTube, 19-Aug-2021. [Online]. Available: https://youtu.be/FNrOfDuP3rg [Accessed: 16-Jul-2023]
Meteor Lake	W. Gomes, S. Morgan, B. Phelps, T. Wilson and E. Hallnor, "Meteor Lake and Arrow Lake Intel Next-Gen 3D Client Architecture Platform with Foveros," 2022 IEEE Hot Chips 34 Symposium (HCS), Cupertino, CA, USA, 2022, pp. 1-40, doi: 10.1109/HCS55958.2022.9895532

Q & A