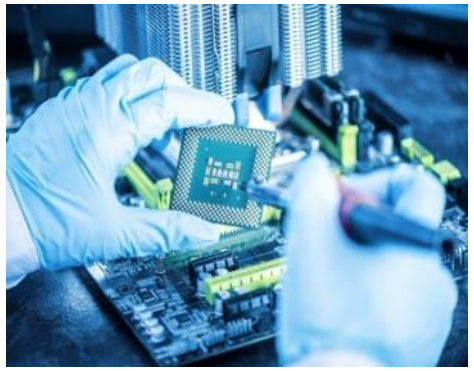
TESSOLVE

A HERO ELECTRONIX VENTURE

Verification Futures Austin 2023

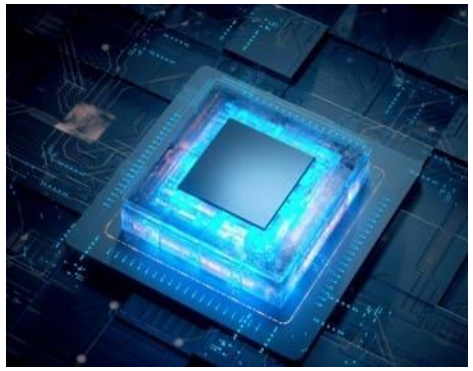
12 years of challenges = 100+ challenges from 30+ experts

Chip Design



Test Engineering

Hardware Design



Embedded Systems

Historic summary

Challenge	Mentions
Complexity	12
Debug	12
Resources	12
Integrating Methods, Languages and Tools	10
Completeness	10
Safety verification	9
Scalability	8
Mixed Signal	7
Power Verification	6
Productivity	5
Reuse	5
HW/SW	5
Security verification	5
Using AI/ML in verification	4

↔ Non-mover — Design complexity stabilising

↔ Non-mover — 70% projects use UVM
All other methods <10%

↑ On the rise — 44% of IC/ASIC projects are safety-critical

↑ On the rise — 58% of IC/ASIC projects add security features to their designs

← New entry

2022 Wilson Research Group IC/ASIC functional verification trends

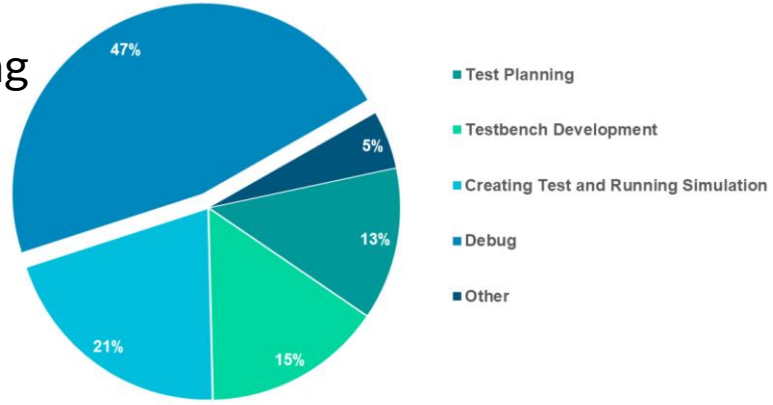


Fig. 9. Where IC/ASIC verification engineers spend their time.

AI/ML Experiments in IP Verification

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