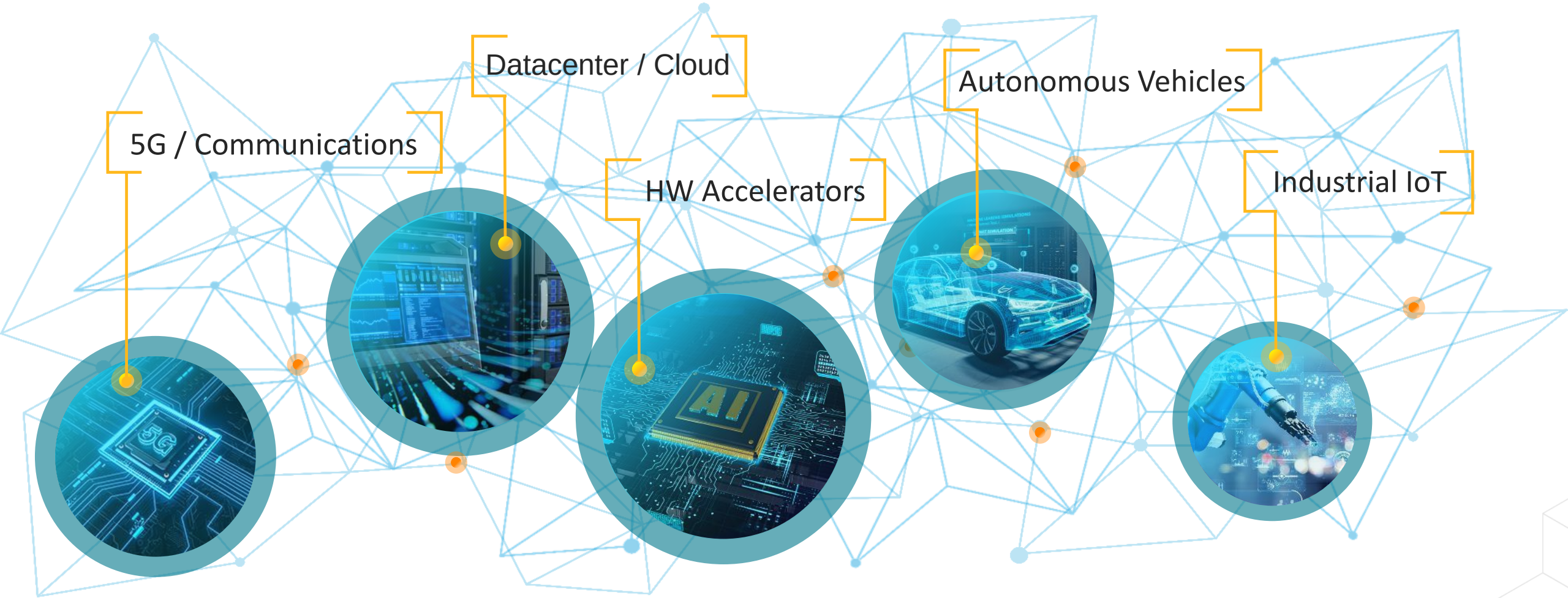
Engines, Logistics, and AI

Verification Futures Austin

Bahadir Erimli
Group Director, Verification Application Engineering

cadence®

5 Generational Trends…All Anchored Around Compute



The Scale of the Problem is Outpacing Engineering Resources

More Annual Design

4X

Over the Next Decade

(<=10nm)

Source: IBS Global Semiconductor Industry Service Report: Design Activities and Strategic Implications, July 2022
Source: Cadence analysis

Transistor Count Increasing

100X

Over the Next Decade

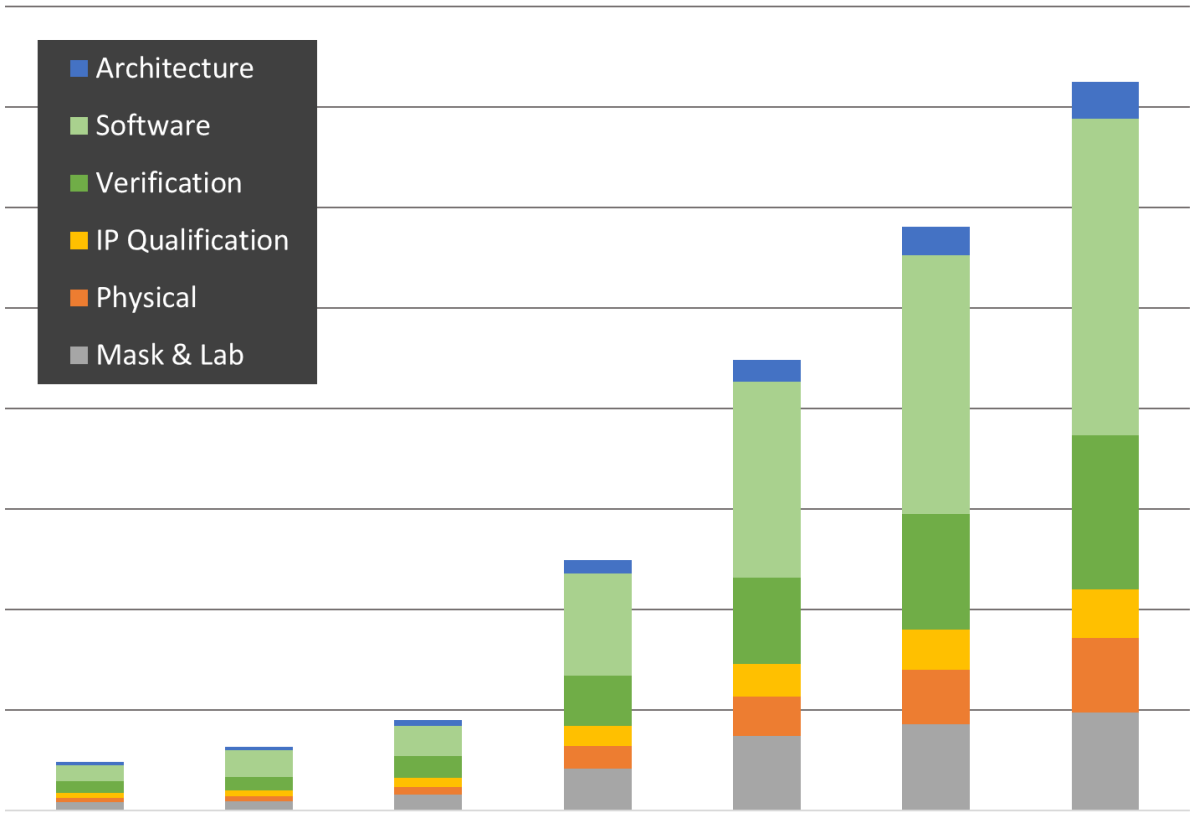
Source: Cadence analysis

Not Enough Engineers

Source: https://semiengineering.com/engineering-talent-shortage-now-top-risk-factor/

Plus new (additional) requirements! E.g. power aware verification, functional safety verification

Total Cost of Silicon – Industry Trend



IBS, Global Semiconductor Industry Service Report
July 2022

“Amateurs talk about strategy…
…professionals talk about logistics.”

(most commonly attributed to)
Omar Bradley
General, United States Army

Package Throughput = Engines x Logistics

Best Logistics

UPS – We Love Logistics

Best Engines

	Van	Truck	Plane
			
Prep time:	10mins	30mins	Few hours
Speed:	25mph	60mph	600mph
Reach:	Front door	Warehouse	Airport

Verification Throughput = Engines × Logistics

Best Logistics

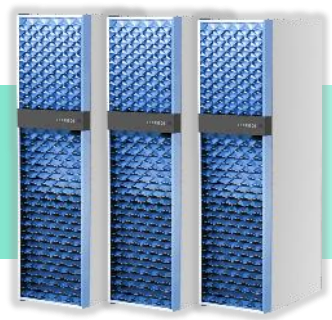
Verification Logistics

Best Engines

Xcelium™

X86 or Arm®-based server

Palladium®



Custom Processor

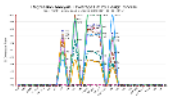
Protium™

FPGA

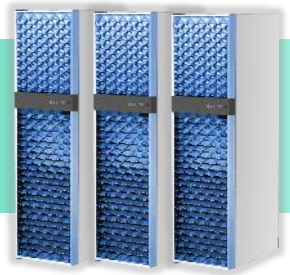
Compile Time:	Minutes	Few Hours	1-2 Days
Speed:	100Hz	1MHz	5MHz+
Reach:	IP Debug	SoC Debug	Software Debug

Verification Throughput = Engines × Logistics

Best Logistics

Run  Cover  Debug 

Best Engines

Jasper™	Xcelium™	Palladium®	Protium™	Helium™
				
X86/Arm	**X86/Arm**	**Custom Silicon**	**FPGA**	**X86/Arm**

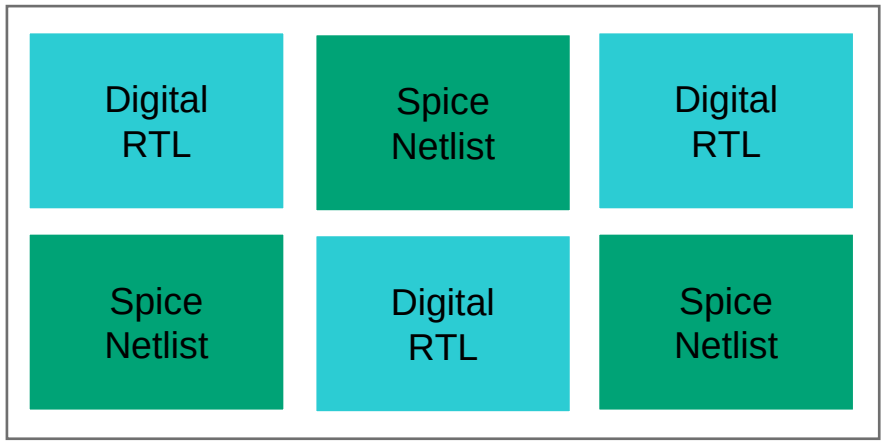
Mixed Signal

⋮

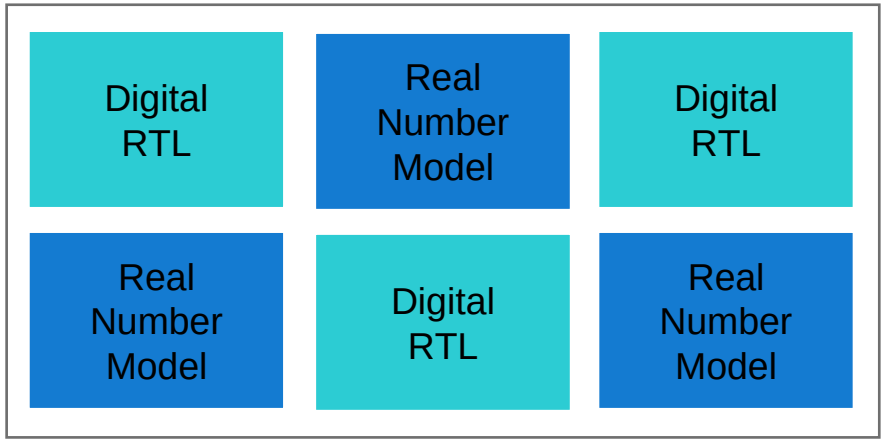
Functional Safety

Xcelium Mixed Signal Simulation

Analog Mixed Signal (AMS)

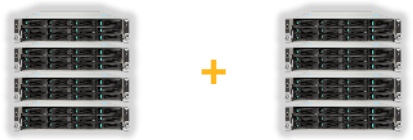


Digital Mixed Signal (DMS)



Unified Debug, Testbench, and Coverage

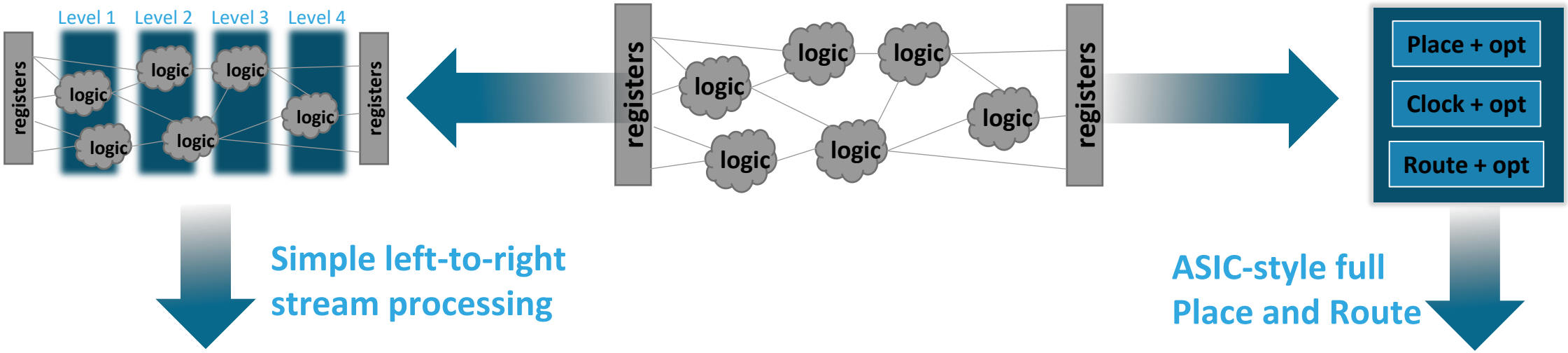
Xcelium™ Spectre®



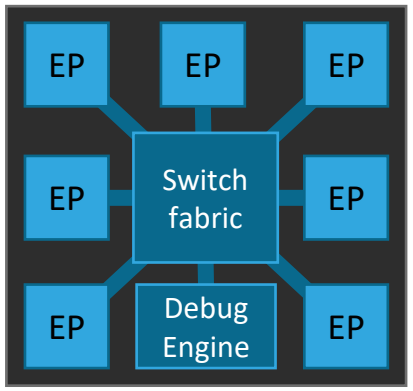
Co-Simulation

Xcelium RNM

Domain-Specific Hardware for Simulation Acceleration



Custom Processor



Debug your Chip

Fast predictable compile
Flexible debug

Debug your Software

Highest
Performance

FPGA

Engines x Logistics with Verisium Manager

Multi-site multi-project global verification management

Job scheduling

Test Plan

Verisium™ Manager

Formal and Static
Jasper™

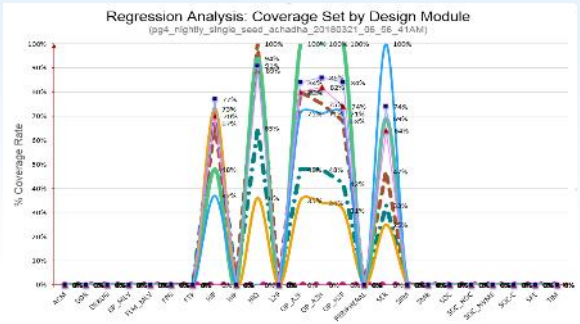
Simulation
Xcelium™

Emulation
Palladium®

Prototyping
Protium™

Regression Type	Block Name	Total Runs	#Passed	#Failed
(no filter)	(no filter)	(no filter)	(no filter)	(no filter)
REGRESSION	Mixed	33	20	13
nightly	DEBUG	6	3	3
nightly	SOC	15	12	3
nightly	DEBUG	9	4	5
nightly	C2C	3	1	2

Block Name	Passed %	Unique Failures	Expression Cov	Block Cov
(no filter)	(no filter)	(no filter)	(no filter)	(no filter)
Mixed	51.95	5	51.67%	72.14%
C2C	33.33	1	36.05%	55.03%
DEBUG	44.44	2	51.85%	72.04%
DEBUG	50.0	1	58.77%	80.76%
SOC	80.0	1	60%	80.76%



Engines x Logistics for Functional Safety

FMEDA

Midas™ Safety Platform

vManager™ Safety
Fault Campaign Management

Fault Reachability
Jasper™ Safety

Fault Simulation
Xcelium™ Safety

Fault Emulation
Palladium® Safety

future

Test Selection and Fault Pruning

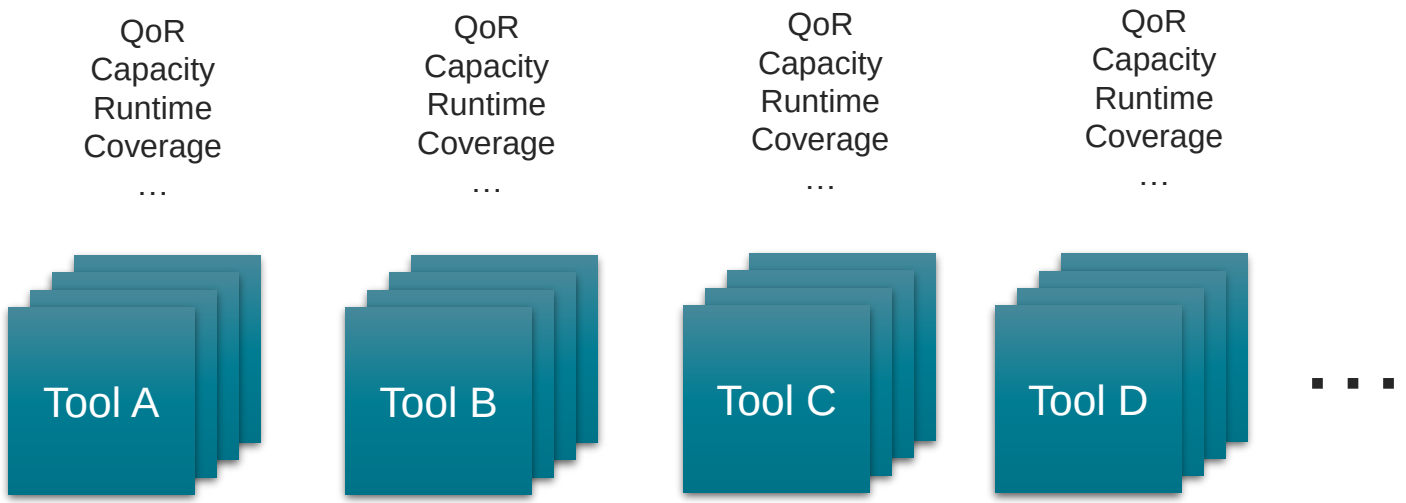
Fault Campaign Orchestration

Fault List Annotation

Safety Reporting

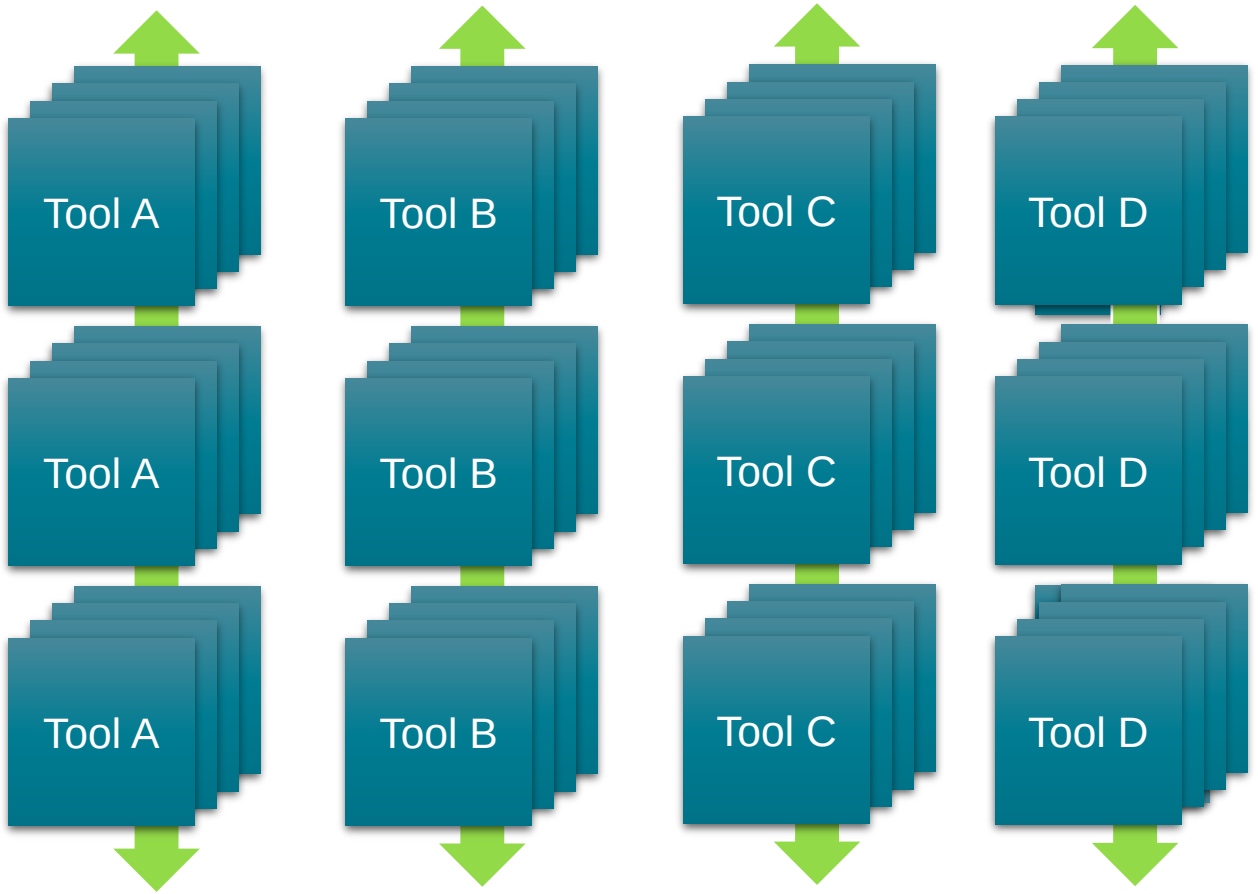
Certification

EDA 1.0



User Perspective

Meet PPA Goals
Meet Coverage Goals
…



Today

Tomorrow

Next Day

Next-Generation EDA

AI-Driven Design and Verification

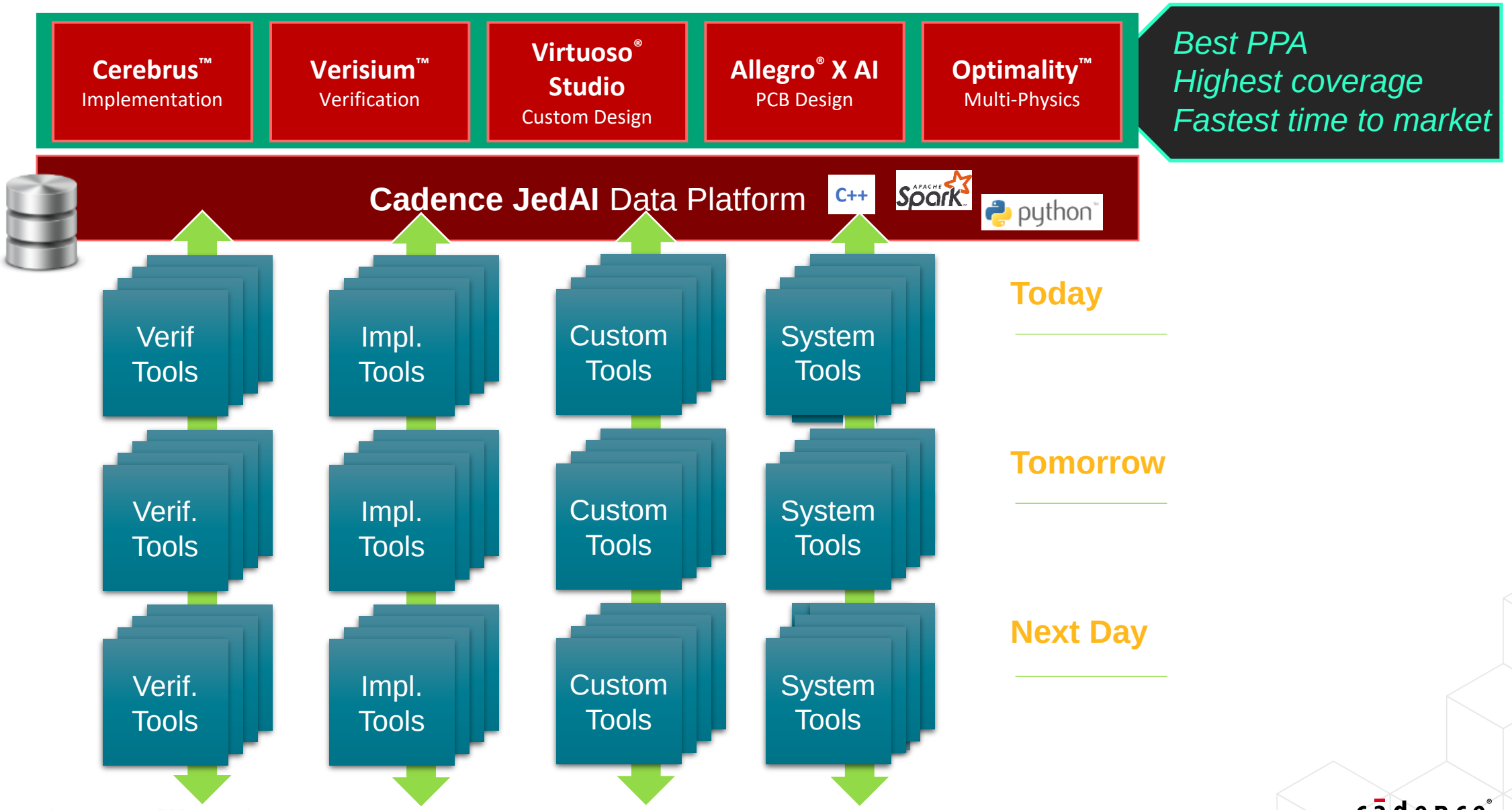
Multi-engine multi-run learning and optimization

Best PPA
Highest coverage
Fastest time to market

Big Data Platform

	Verif Tools	Impl. Tools	Custom Tools	System Tools
Today				
	Verif. Tools	Impl. Tools	Custom Tools	System Tools
Tomorrow				
	Verif. Tools	Impl. Tools	Custom Tools	System Tools
Next Day				

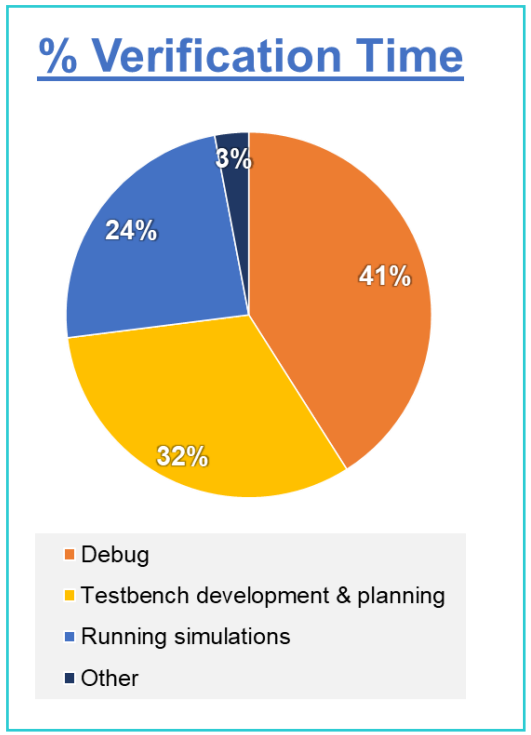
Cadence EDA 2.0 Solutions



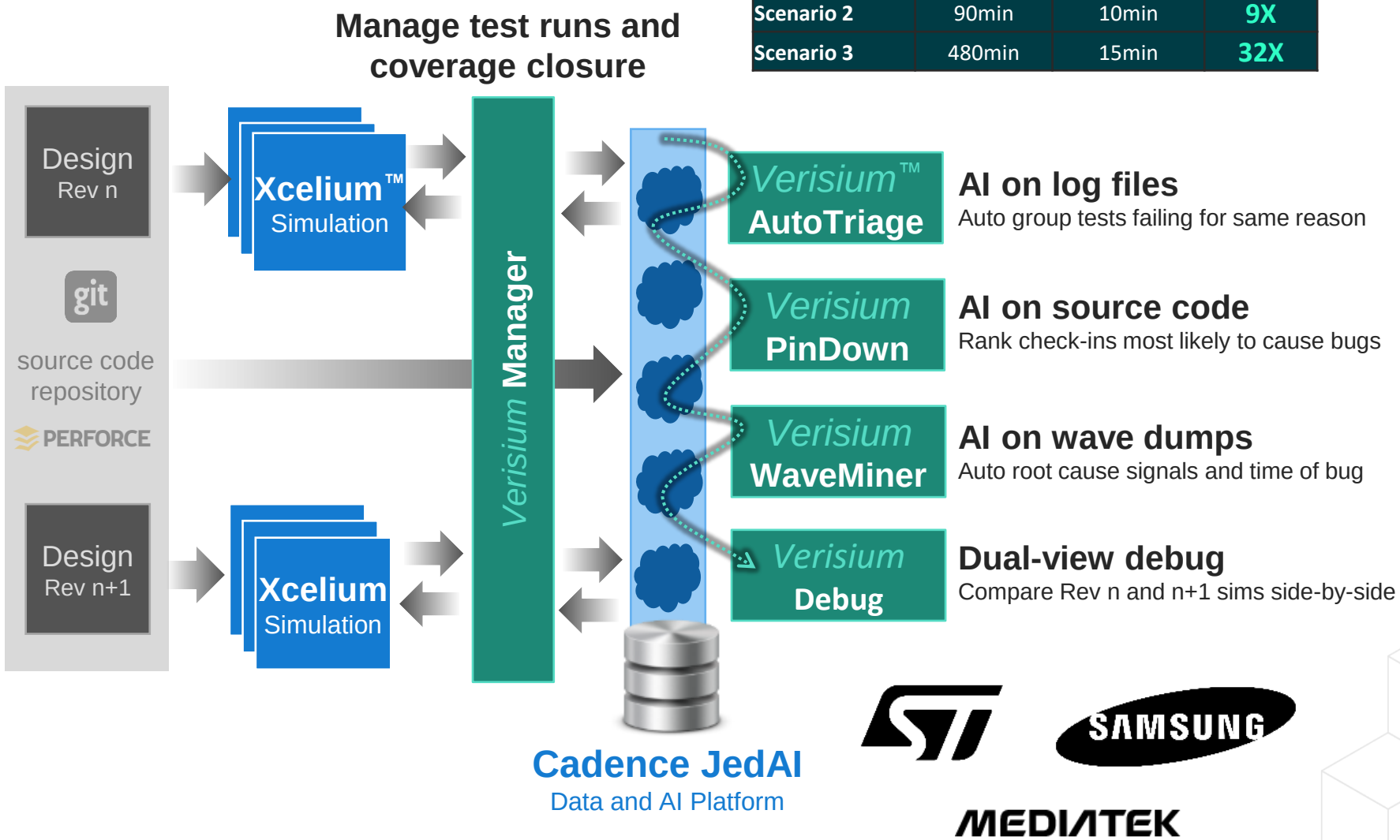
Verisium AI-Driven Verification

Customer Case Study

Time to Debug	Current Flow	Verisium Flow	Speed-up
Scenario 1	300min	10min	30X
Scenario 2	90min	10min	9X
Scenario 3	480min	15min	32X

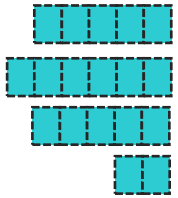


Wilson Research Group, October 2020



AI-Driven Simulation Performance

Randomized Test Suite **Run N**

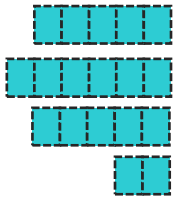


Xcelium™ ML

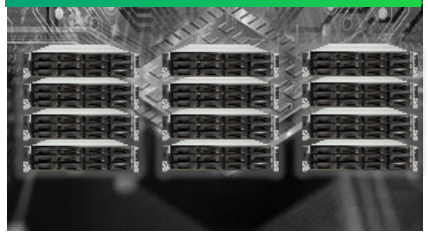
*Up to **5X** faster*
Same coverage

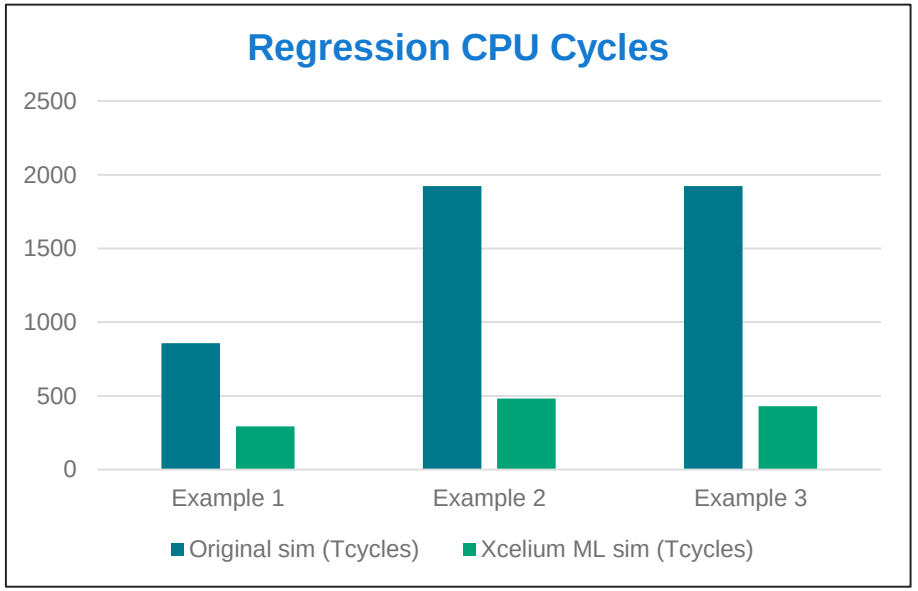
Machine Learning

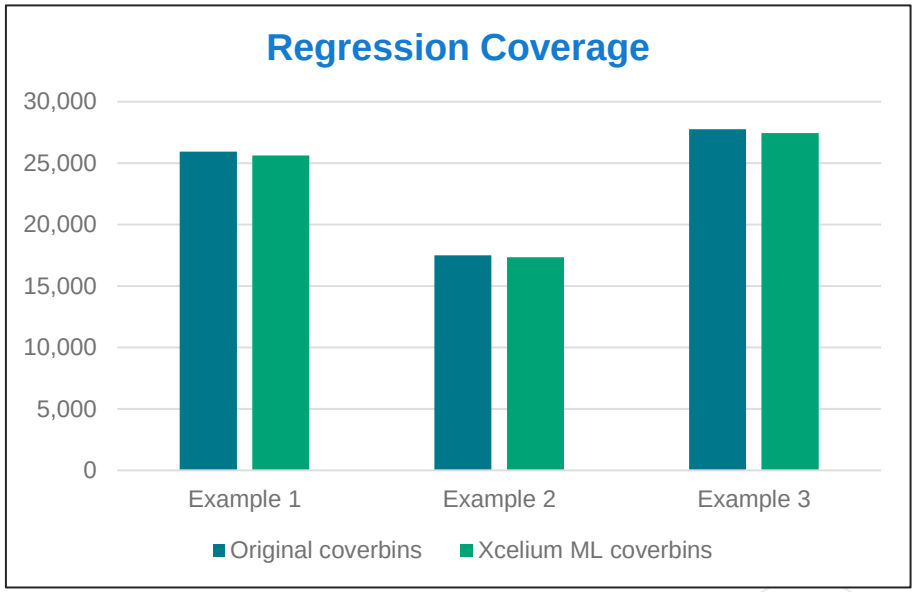
Randomized Test Suite **Run N+1**



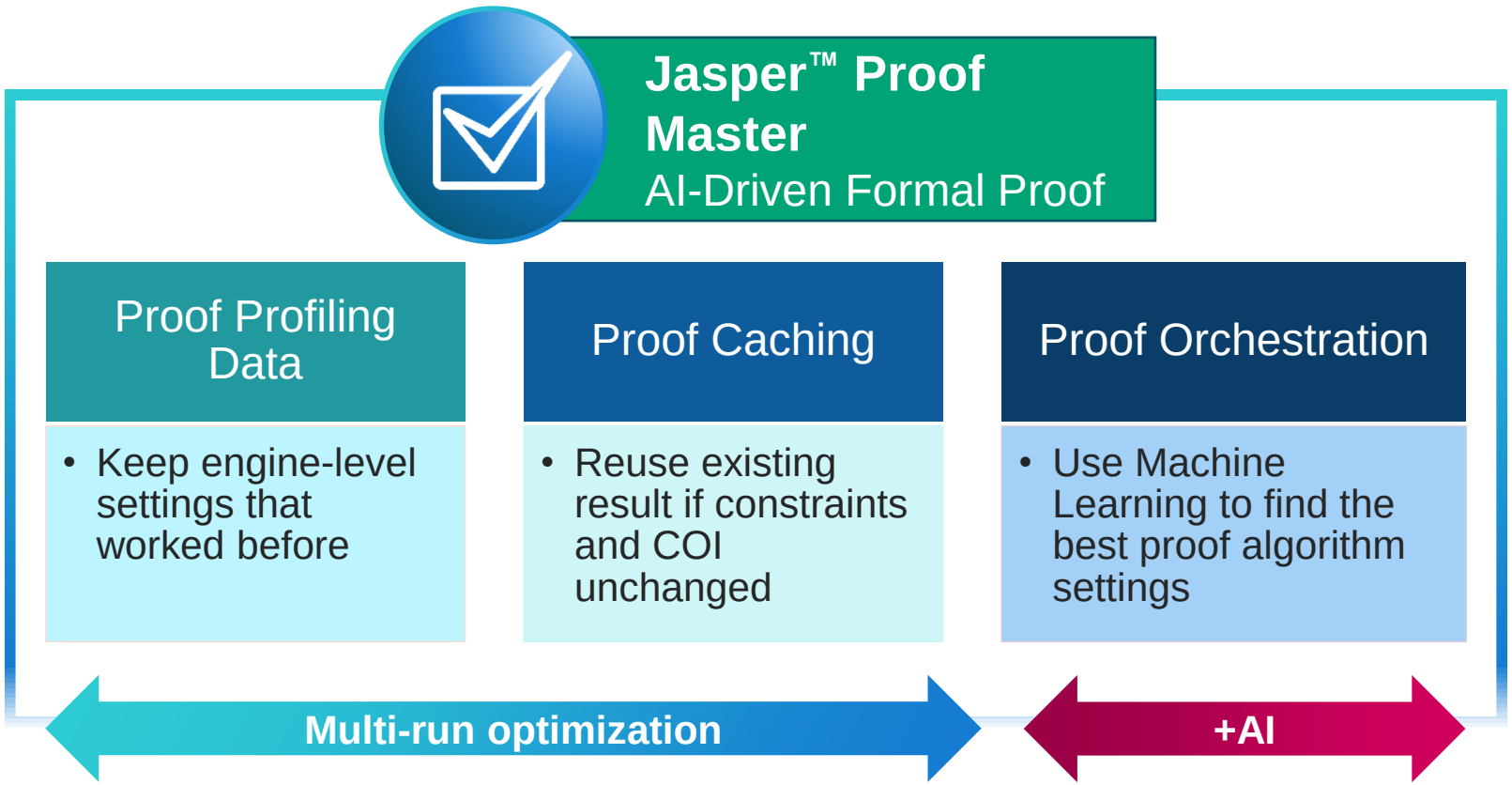
Xcelium ML







AI-Driven Formal Proof

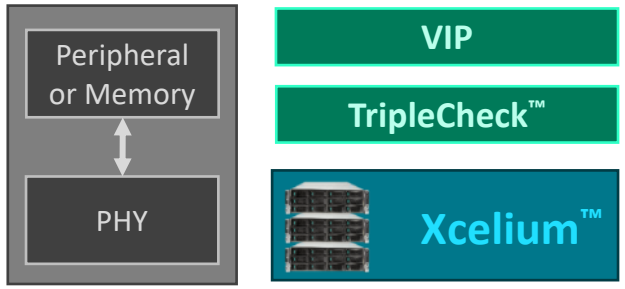


Proof Success Rate

Testcase	Baseline	Smart Proof	Gain
A	50%	59%	1.2X
B	69%	69%	1.0X
C	12%	25%	2.1X
D	44%	83%	1.9X
E	57%	94%	1.6X
F	68%	69%	1.0X
Total	53%	71%	**1.3X**

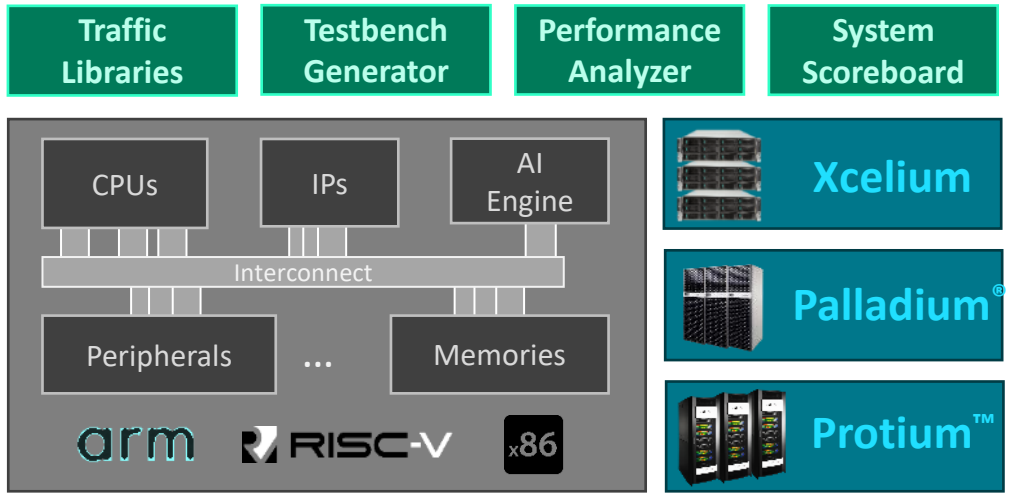
Extending the Reach of Verification IP

Interface and Memory VIP



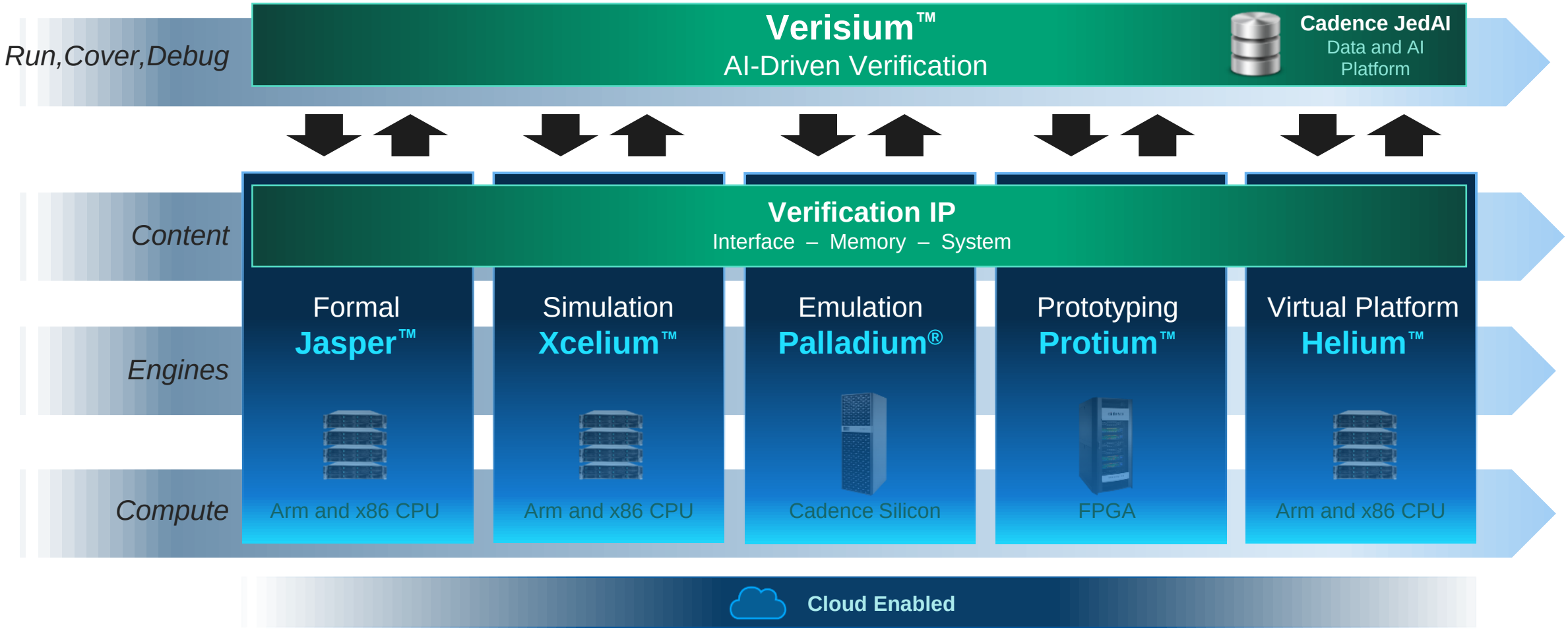
- Industry's broadest portfolio
- Verify compliance and cover the corner cases with TripleCheck
- Highest performance with C-based kernels

System VIP



- System-level tests up and running in a day
- Validate PCIe® for Arm SBSA
- Boot Linux and Windows over PCIe

Cadence Verification Solution



Thank You