Ericsson's Challenges of IP Development and Verification for Products with a Long Shelf Life

Alex Duhovich – PEU Silicon IP Verification Methodology Lead

About myself

- 20+ Years, mainly in Telecommunications Industry (Hughes, Ericsson)
- Bachelor's in EE from Drexel in 2000
- Master's in EE from University of Maryland College Park in 2015
- At Ericsson since 2017
- Started in IP verification -> Team Lead -> Verification Methodology Lead
- Email: alexei.duhovich@ericsson.com
- LinkedIn: https://www.linkedin.com/in/aduhovich/

Ericsson at a glance:
A world leader in ICT and 5G

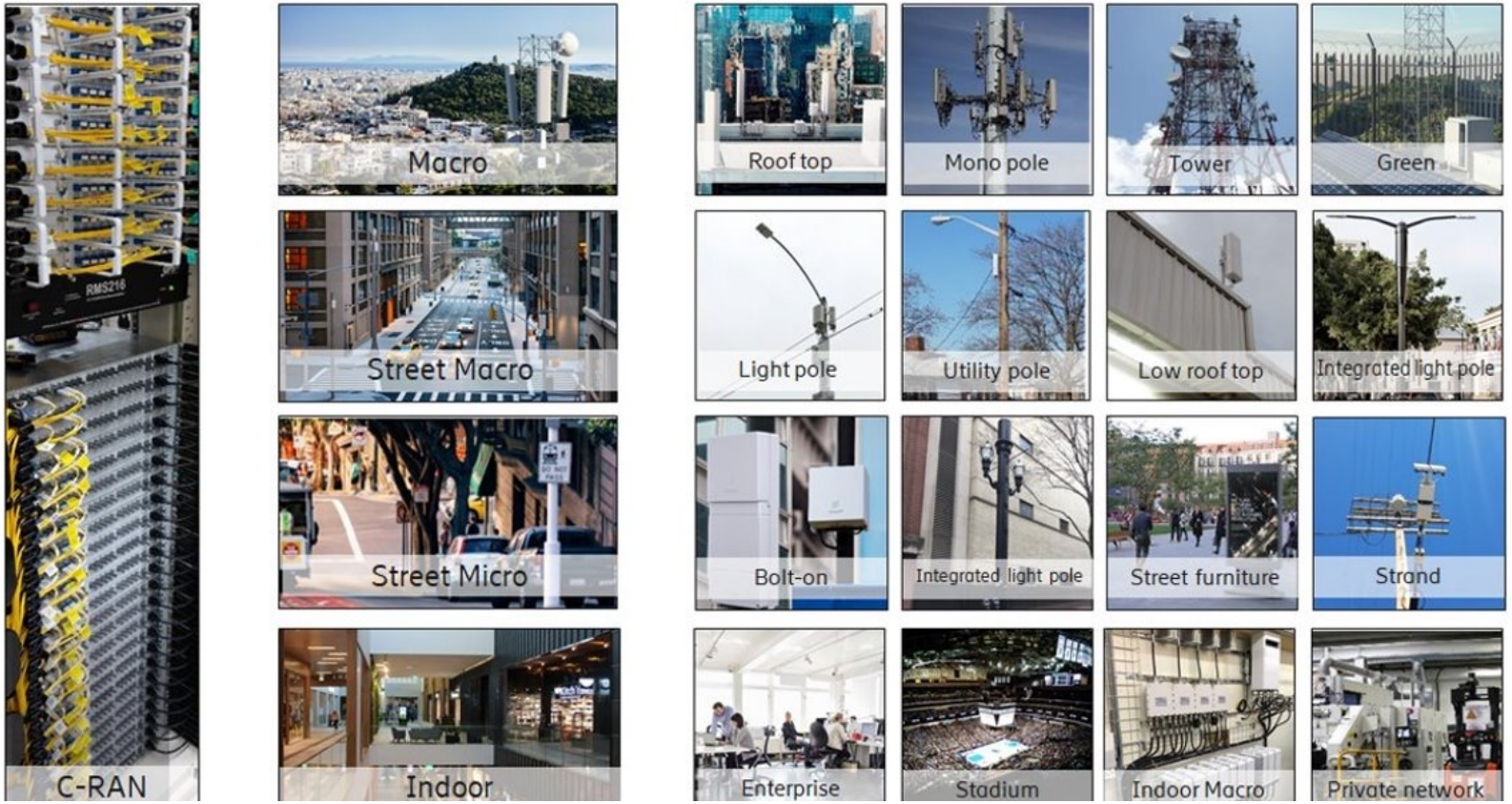
Purpose:
- To create connections that make the unimaginable possible

Vision:
- A world where limitless connectivity improves lives, redefines business, and pioneers a sustainable future

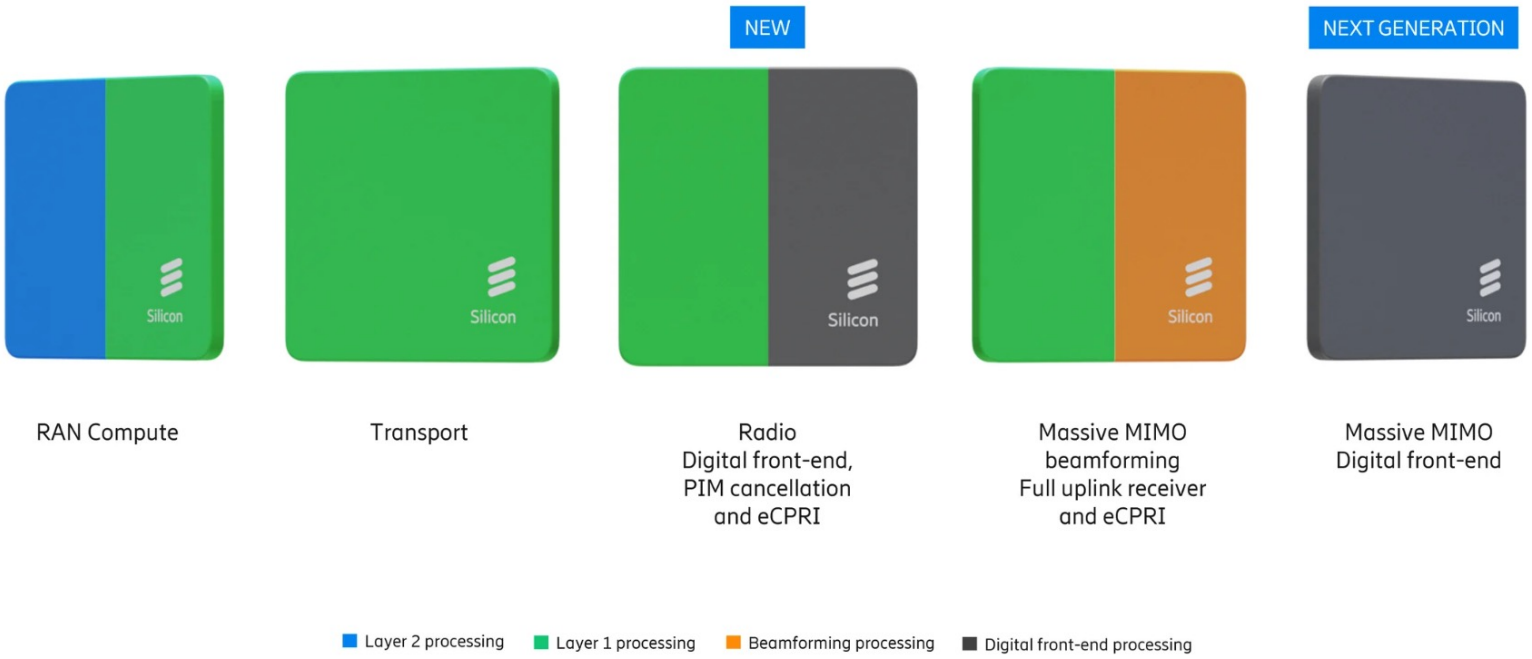
History:
- 140+ years of delivering ground-breaking solutions and innovative technology for good

Leader in Technology:
- Leading provider of Information and Communication Technology (ICT) to service providers
- 227.2 b. SEK (~ $ 27b) in Sales
- 54,000 patents

Solutions take many form factors



Ericsson Silicon Portfolio



Challenges

Product-centric development

Long product shelf lives lead to requirements creep

Requirement quality gaps lead to planning challenges and schedule slips

General increasing complexity challenge with verification: Methodology scaling, Power, Security

Product Centric Development

- IP requirements based on product
- Requirements come in at the start of a project
- Conflicting requirements possible between projects
- Team to close all milestones for each project
- Difficult to maintain code base and version control
- Difficult to deliver to multiple projects at once

Long Product Shelf Lives

- Product lives of ~10 years
- Customer expects longevity
- Products are overdesigned to support future standards
- Cannot iterate on fixes between generations. Must be right the first time.

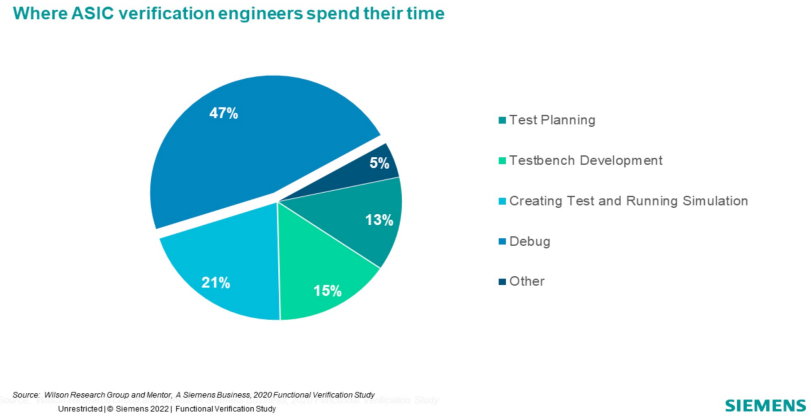
Planning Challenges

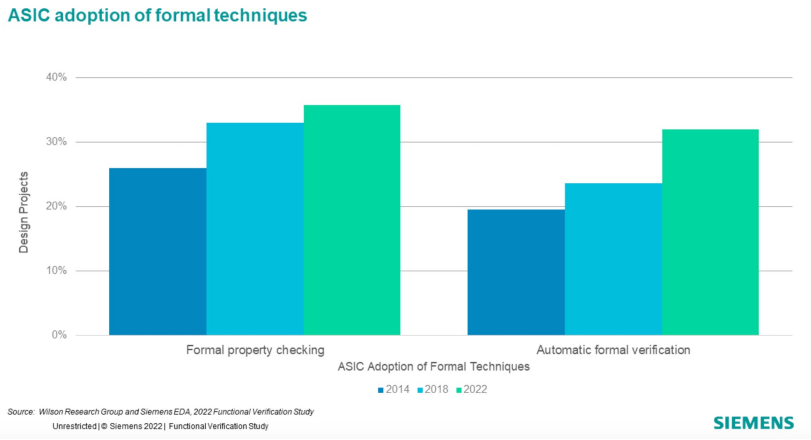
- Requirements quality varies at the start of the project
- Requirements creep happens
- Initial planning often inaccurate
- Replanning is disruptive
- Causes schedule slips, missed scenarios/use cases

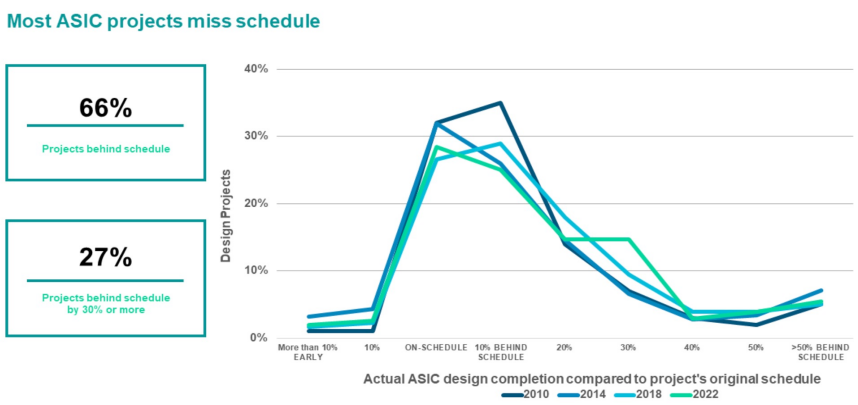
Increase of Complexity

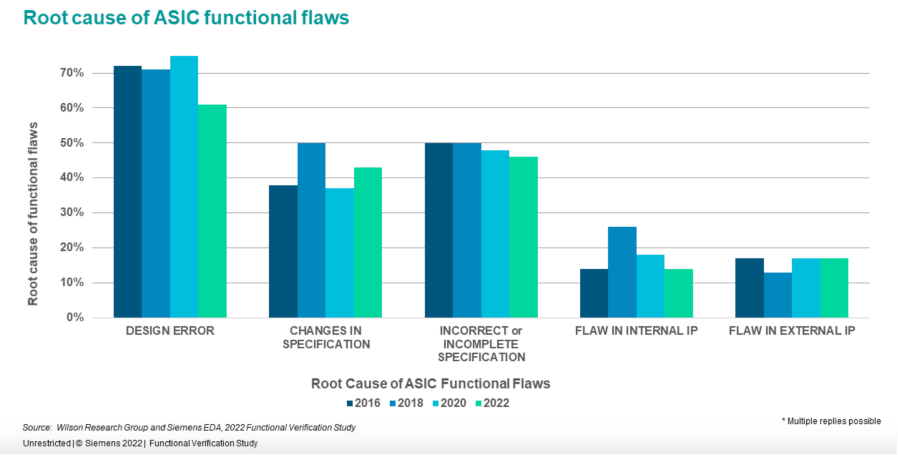
- Design complexity increases exponentially
- Workforce cannot keep up
- Constrained-random verification doesn’t scale
- Most time spent on debug and coverage closure: These are hard to predict.
- Power and Security are becoming extremely important

Industry Trends in ASIC Development









IP Centric Development

Architecture mindset shift: IP Roadmaps with forward looking requirements

Reuse and feature superset mentality for design and verification

Methodology and process update for feature-based, agile development

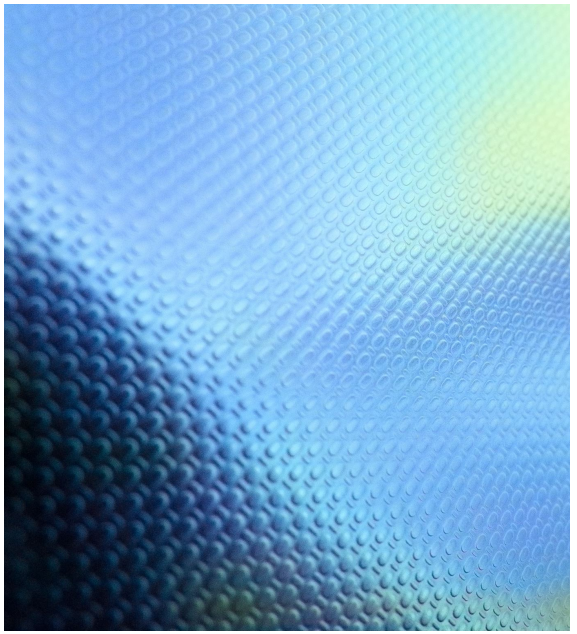
Infrastructure update to support this way of working

Planning for the Unknown

- Increased visibility of development data: Early warning system
- Robust documentation and tracking of requirements
- Using past data to predict the future and plan appropriately
- Building risk into schedules

Hedging Your Bets

- Infrastructure expansion and efficiency improvement for better engineering turn-around-time: LSF, Compute, Storage
- Simulation and Regression time improvement: Looking for opportunities to improve performance
- Updates to verification strategy and methodology to leverage latest techniques and enable shift left: Formal, HLS
- Leveraging EDA state of the art solutions to improve development, debug and coverage closure times



Q & A