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SLT in the Era of Heterogeneous Integration

Agenda

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Trends in the SOC Product development

Challenges from the Test Perspective

Actual Use Case Test … Leading to System Level Test

Inclusion of SLT to Test Flow for Heterogeneous Integration

Summary

Trends in the SOC Product development

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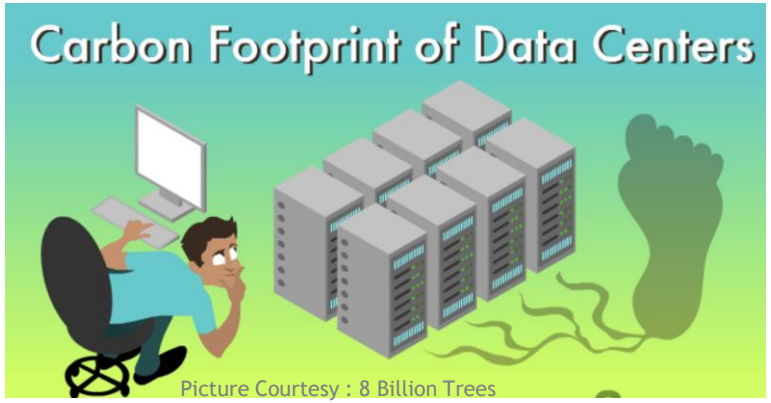
- Data centre offers massive computing resources, typically in the form of an elastic cloud platform
  - Carbon Footprint
    - Electricity Consumption
    - Water Consumption
    - Lifetime of the Equipment



Data centres are responsible for 2% of overall U.S. **greenhouse gas emissions**

- Needs of Diverse Domain Specific Architectures
  - Machine Learning, Deep Learning, Block Chain and NLP
    - Dedicated Memory
    - More / Scalable ALU
    - Host of Interfaces .. etc
- Chiplets
  - Reduce Product Development time
    - Integrating Pre-Developed Die (KGD) https://www.youtube.com/watch?v=yDaZe1Xb9Ls
    - Different Process Node in the Same Package
    - Substrate a key element in System Performance

Trends in the SOC Product development

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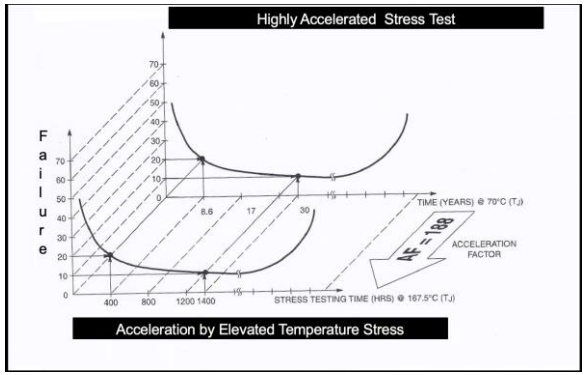
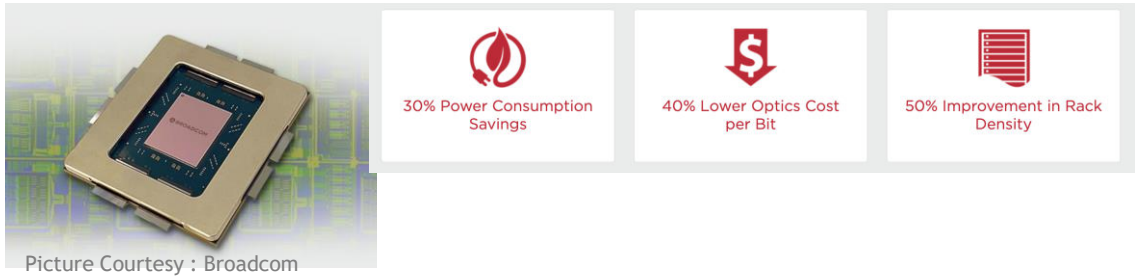
- Adaption of Lower Process node in Mission Critical application like Automotive
  - Reliability
  - TDP Vs Operating Temp



- Connected Vehicles
  - Latency (1ms for 5G)

- Hi Speed Inter connect standards
  - CXL
  - BOW. https://opencomputeproject.github.io/ODSA-BoW/bow_specification.html
  - UCIE https://www.uciexpress.org/specification

- Co-Packaged Optics



Picture Courtesy : Broadcom

Trends in the SOC Product development

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Key Essence	Key Essence that is of Importance for Test
• Carbon Footprint	• Every mV of power optimization saves M$
- Electricity Consumption	- Substrate Design optimized for PDN
- Water Consumption	- Thermal Management
- Lifetime of the Equipment	- Silicon Monitoring
• Reduce Product Development time	
- Chiplets	- Chiplets deigned considering “Off Die DFT”
- Integrating Pre-Developed Die (KGD)	- KGD could be from many different vendors
- Different Process Node in the Same Package	- Test / Validation of Substrate Performance
- Substrate influence in System Performance	- Traceability and Security

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Heterogeneous Integration - Helping to keep up with Moore's Law scaling

Time to put a robust Test solution in Volume – Test can't be a after thought

Individual Die not necessarily define the full functionality of the Packaged IC .. could be only partial.

Assembly defects after package of a particular KGD many not be 100% directly detectable – Additional test.

Individual Die DPPM come into picture .. The over all package level DPPM becomes additive of individual KGD DPPM

Additional Challenges in Lego Block World

Thermal influence from the neighboring Die.

Thermal Control Mechanism for Volume Test.

Classifying DUT a Good based Short Duration Test.

Challenges from the Test Perspective

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What is happening inside the Chip? – Monitor (Design , Volume Test and In-Field)

In-Chip-Monitor – Instantaneous Environmental Monitor.

- Process Monitor.
- Power Rail Voltage Monitor.
- Temperature Monitor.

Process Monitor

- Decision making before classify the Die a KGD
- Behavioral understanding of Wafer Level and Lot Level

Power Rail Voltage Monitor

- Compute Performance optimization by monitoring Voltage
- Alarm / Interrupt Signal activation to other subsystem and bring the device to safe state
- Could be considered as a part of POST

Temperature Monitor

- Compute Performance optimization by monitoring Voltage
- Alarm / Interrupt Signal activation to other subsystem and bring the device to safe state
- Could be considered as a part of POST and Mission Mode Test.

Traceability

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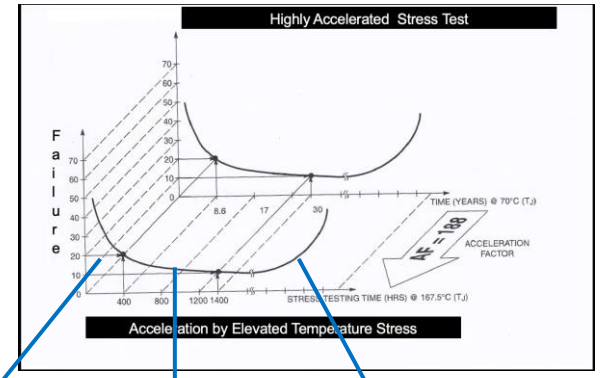
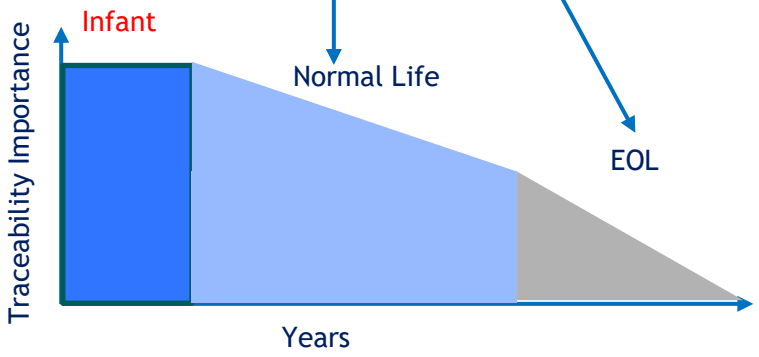
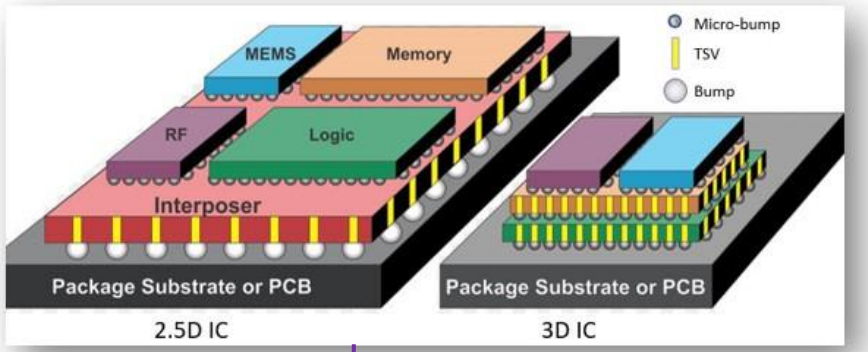
What is happens when the Heterogenous packaged IC Fails in the Field?







- Wafer ID
- Die ID
- Assembly Data
- Test Data

Standardizing traceability for Chiplet Based Heterogenous IC Packed at Individual Diel level and exchange of information form the Packaged IC on a established Interface protocol .. Thus, enabling Datal Analytics need to considered of Importance

OSAT provide Unit Level Traceability (ULT) by 2d Barcode on a Packed Device

Commercial Device may need about 5 years of traceability but for Automotive it would extend to 15 Years

Identifying root cause sooner would be important for Automotive Grade IC (especially for ADAS Levels 4 and 5) and probably for high end HPC ICs

SEMI Traceability Standards committee SEMI T23

KGD Monitoring

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In-Chip-Monitor – Structural Monitor

- Semiconductor do have aging as inherent property as it is influenced by NBTI (Negative Bias Temperature Instability), HCI(Hot Carrier Injection) and TDDB (Time dependent dielectric breakdown).
- Aging affecting Propagation Delay

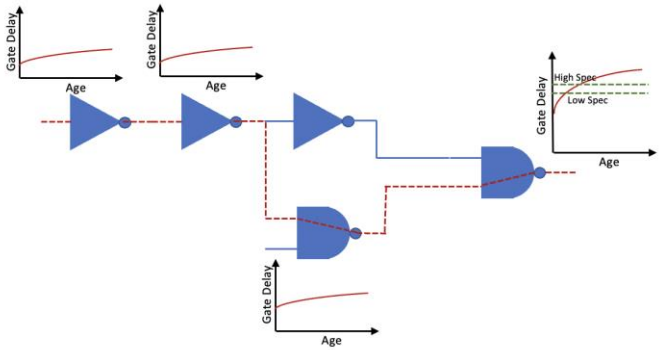
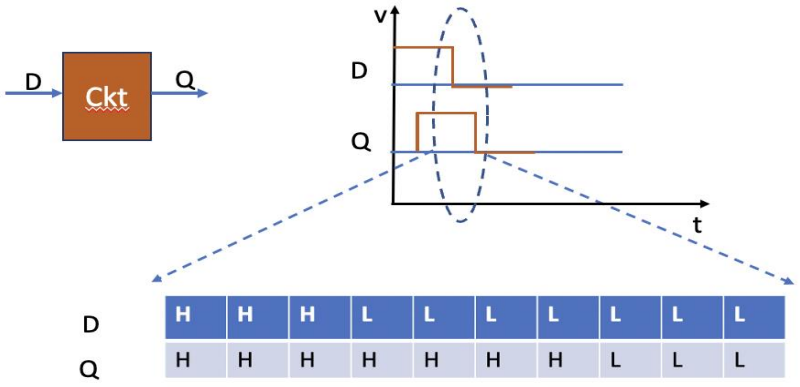


Figure 1: Foundry provides aging model of the transistors to do timing analysis of the circuit. As the transistor ages over period, it increase the gate delay. This could

- Path Margin Monitoring



D	H	H	H	L	L	L	L	L	L	L
Q	H	H	H	H	H	H	H	L	L	L

Figure 2 : Response of a digital path in a circuit constituting a Delay and its time domain response. The dotted line captures the state of the input D and out put Q, which are sampled faster.
In this illustration 10 logic states are collected from D and Q to form a Signature

EDA Vendors now provide Silicon Life Management Tool (SLM) for end-to-end Visibility.. Right from Design, Product Ramp, Volume Production and finally In-Field

Seems no SLM Standards established yet !!

Actual Use Case Test … Leading to System Level Test

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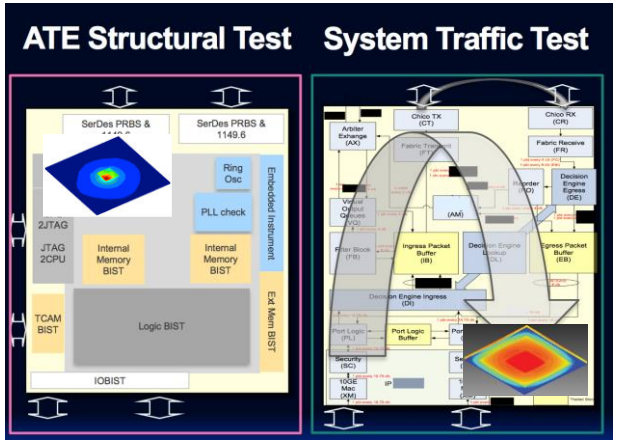
System-level test is the ability to test a chip, or multiple chips in a package, in the context of how it ultimately will be used.

*Source: Semiconductor Engineering 9 Oct 2017



In ATE based test the focus is more on getting the various blocks that are present within the IC tested for a pass and fail and classify the device a pass, when all the blocks in the device pass

Complex IC used for HPC, Automotive etc.. the device needs to be tested along with the other supportive ICs such as PMIC, External Memory, Display, and other power electronic and running on a customer-specific firmware. It is important to mention that the external support ICs mentioned may not be from the same manufacturer.

Testing for customer-specific Use Case is becoming a key need for the devices that are used for mission-critical applications such as Automotive and Data Centers (Silent Data Corruption)along with the need for DPPM quality levels drives SLT requirement

System Level Test - Facts

Compared to ATE test time that are usually in Sec .. SLT test time could run to several minutes

Number of parallel device tested in ATE is limited by ATE available resource and hence usually 4 to 8 device tested in parallel for high pin count device

SLT is performed in massive parallelism in 100's of Device tested in Parallel and hence a specialized SLT Handler Equipment needed .. Additional Capex

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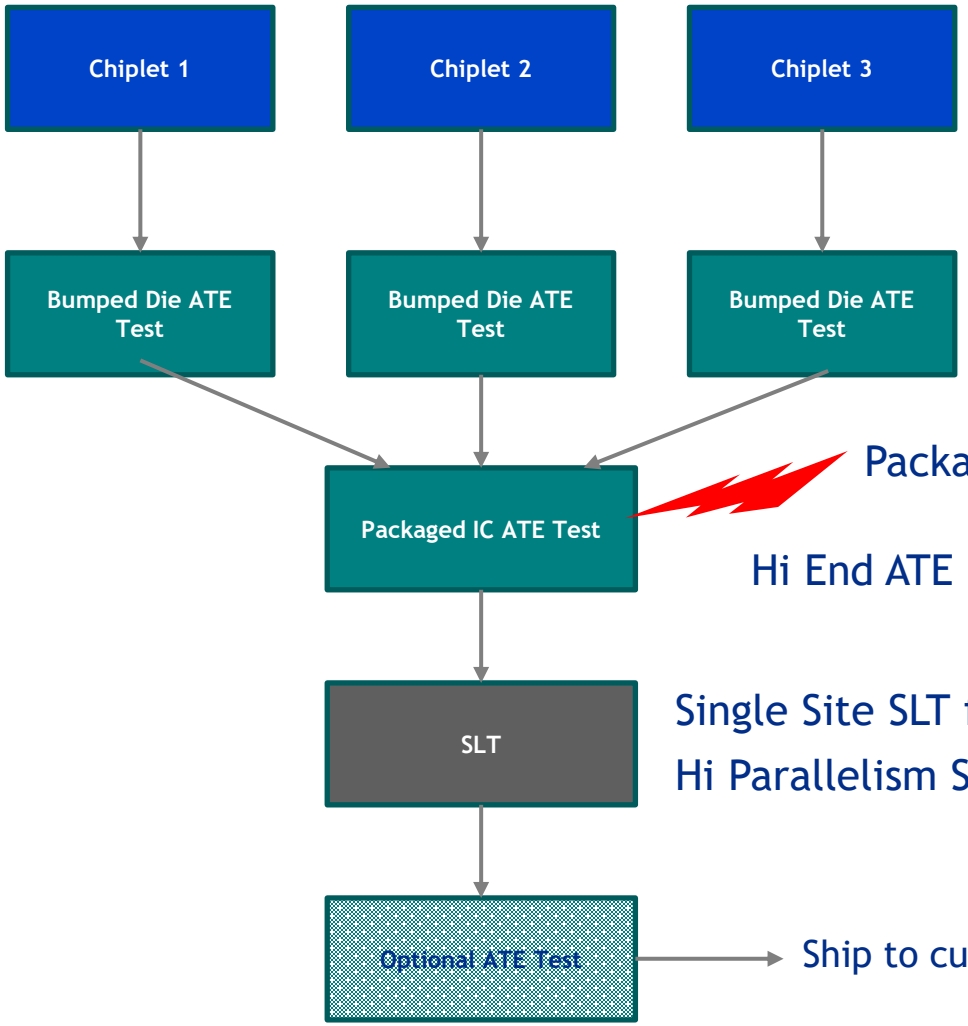
Test Flow for Chiplet Based IC



Low Cost ATE - Parallelism more than 8

Package Substrate performance

Hi End ATE – Parallelism 4 to 8

Single Site SLT for NPI - Use existing Handler

Hi Parallelism SLT for Volume – SLT Handler

Summary

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Deep experience on Chip level Volume test and Systems Level Validation across various type of market segment (Consumer, Medical, Automotive, Avionics) and Various type of Device (Digital, PMIC, Mixed-Signal , RF and SOC)

Rich experience on the embedded product development cycle and end OEM expectations on product side and expertise to create SLT **Uses Cases** for semiconductor companies

Domain specific expertise in creating end application based **Use Case** testing for automotive / Industrial / Multimedia / Compute applications

Expertise in developing Use Case Test using OS like Android /Linux /RTOS

SLT Handler partnership to create a robust volume Test Solution

Thank you for your time

Team Tessolve