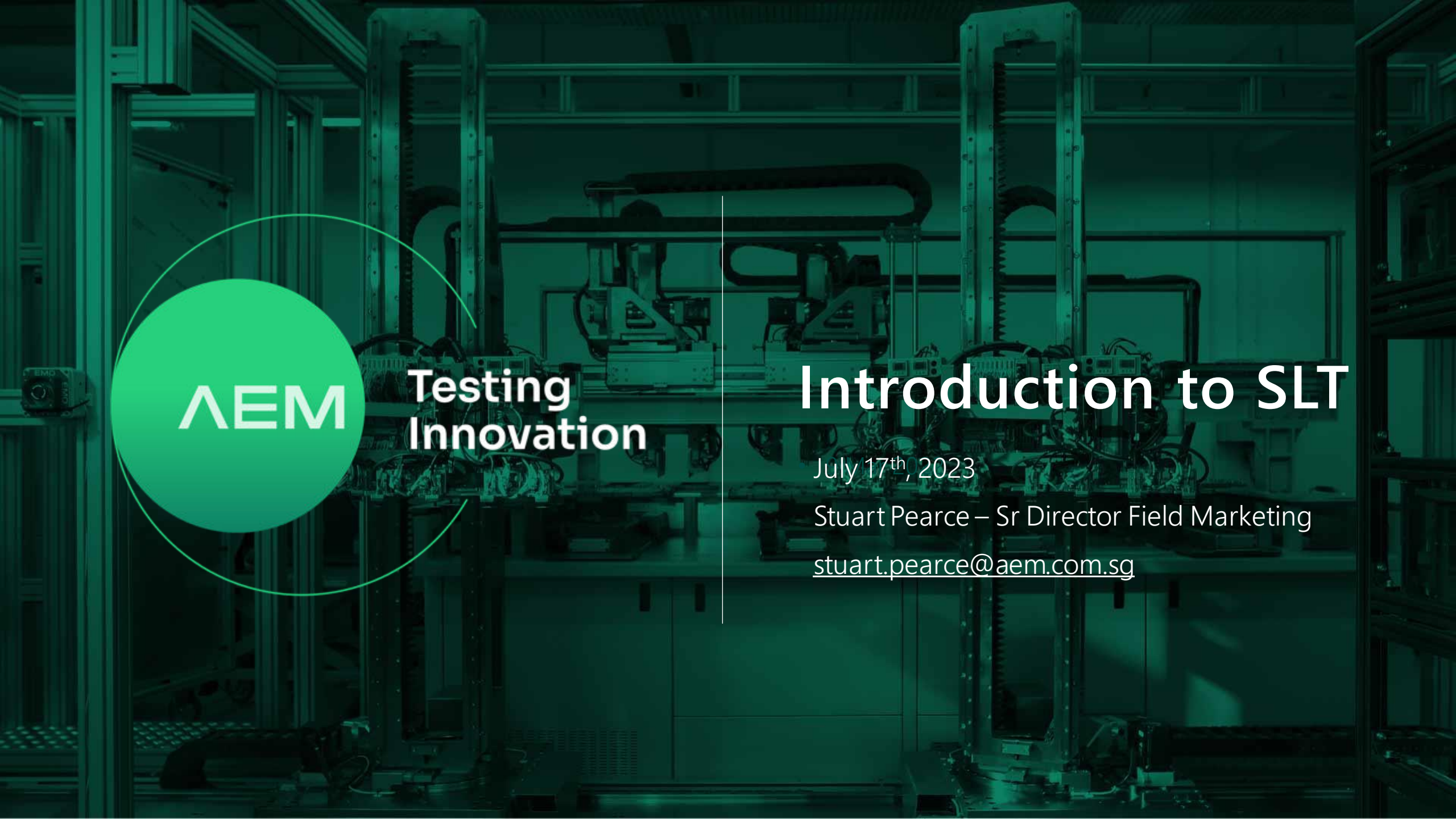

AEM

Testing Innovation

Introduction to SLT

July 17th, 2023

Stuart Pearce – Sr Director Field Marketing

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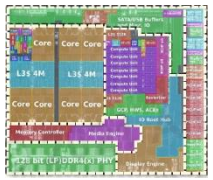
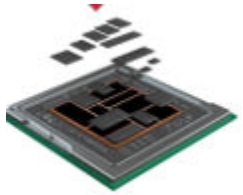
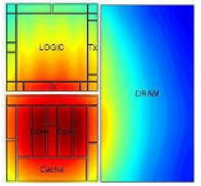
Industry Trends



Die complexity
- Increased transistor counts
- Larger number of test escapes
- TTM, development $$$, KGD



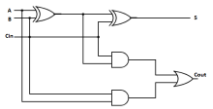
Packaging
- Heterogenous
- Application specific
- Evolving technologies, 2.5D, 3D, POP, WLCSP
- Interfacing



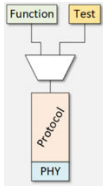
Emerging Thermal challenges
- Local power density, multiple zones
- Die warpage and chip to chip planarity
- Interfacing during test
- Increasing power requirements

Supply chain evolution
- IP from multiple vendors
- Shifting boundaries between IDM, OSAT and foundries.
- Customer / application expansion across multiple industries
- Test and yield visibility across supply chain
- Security

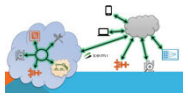
Test Development And Flow Changes



Design Tools
- EDA tools are evolving
- Links between EDA tools and Test Siemens/Mentor Tessent Silicon Insight and ATE connect, Cadence Portable stimulus etc
- Ability to handle multiple DFT cores



Industry standards
- IEEE 1149.x SCAN, 1149.10 high speed serial SCAN
- IEEE 1687/ IEEE 1500, IEEE 1838 standard interfaces
- SSN
- System level SCAN tests



Data collection and Analytics
- Support STDF, RITDB industry standards
- Ability to use industry solutions
- Data Analytics

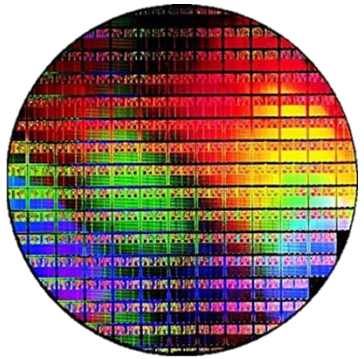
Test Flow
- SLT is now required for mission mode testing
- Use SLT data to help determine Shift left, shift right trade offs
- Move test insertions to optimize TTM and cost of test
- Development of system eval. boards and development kits
- Ability to load and run application stack in system tester

AEM Test Coverage

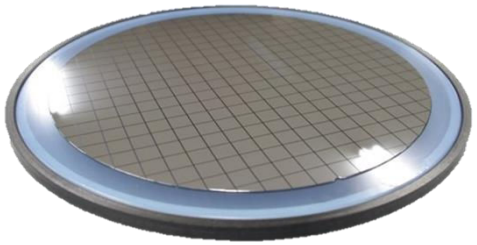
AEM Test Flow Centric Strategy

Handling, Interfacing, test and thermal management across insertions

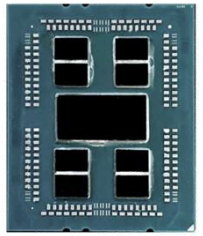
Wafer Probe



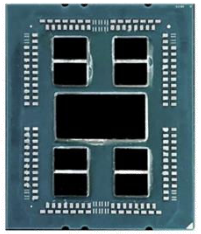
Die Level Probe



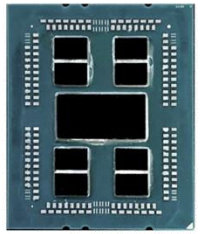
Burn In



Final Test



SLT



SLT was adopted by HPC in Mid 2010's as an additive test process to ensure quality
SLT has now been adopted for Automotive, consumer and mobility components

Next step is integration of SLT+ and test 2.0.

Paradigm Shift in Test, System Level Test Application driven

Traditional Semiconductor Test Flow

Wafer Sort

100%

Final Test

M%

(100-M)%

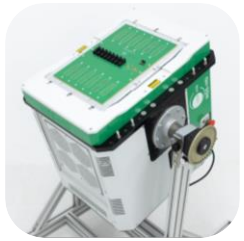
Limited SLT

Product Ship

New Semiconductor Test Flow:- SLT+ and Data Analytics

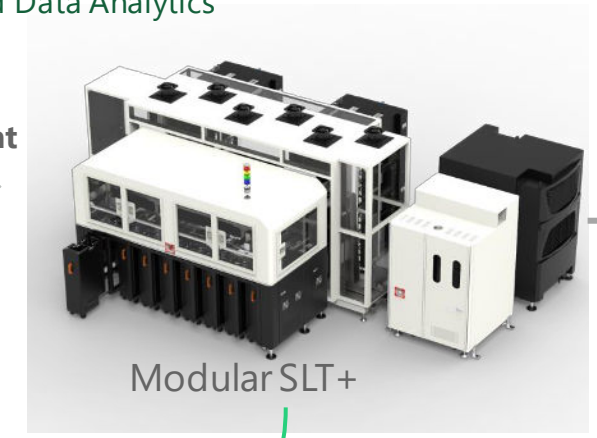
Wafer Sort

Shift Left



Basic Final Test

Shift Right

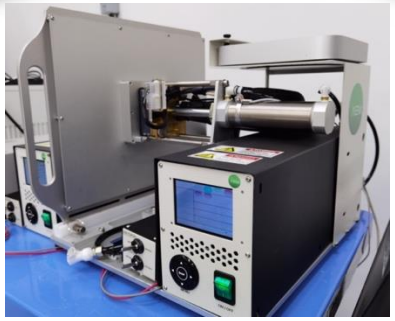


Modular SLT+

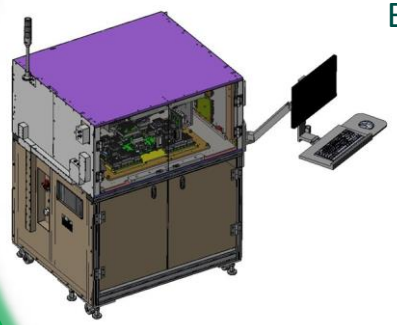
Product Ship

Upstream Data Analytics
Test Flow optimization

Scalable SLT Solutions with Active Thermal



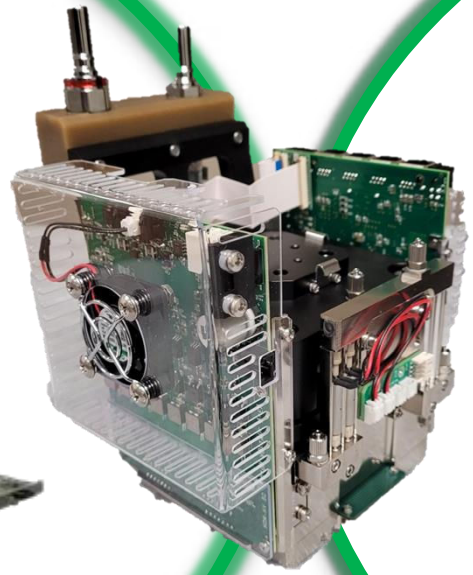
Benchtop Thermal Stations (x1 site)



Customer Test Cells (x1 - x4 sites)

HD Thermal Arrays. Re-use in production (Up to x32 sites)

ATC Thermal



Slot Base High Parallelism SLT/BI

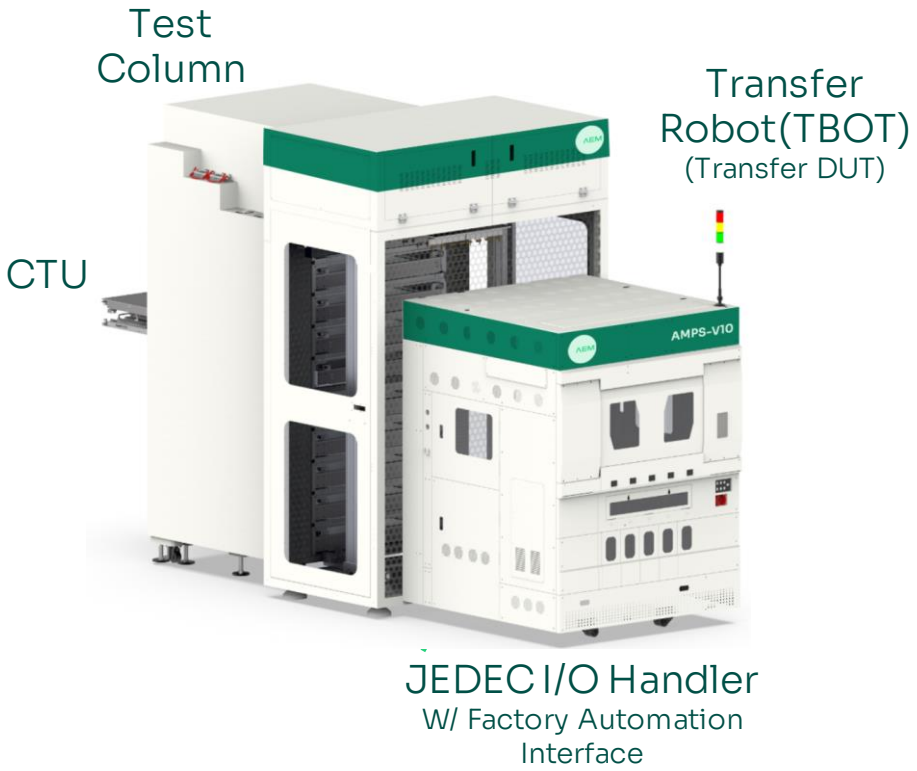
Large Format *12 SLT/BI

Lab Solutions

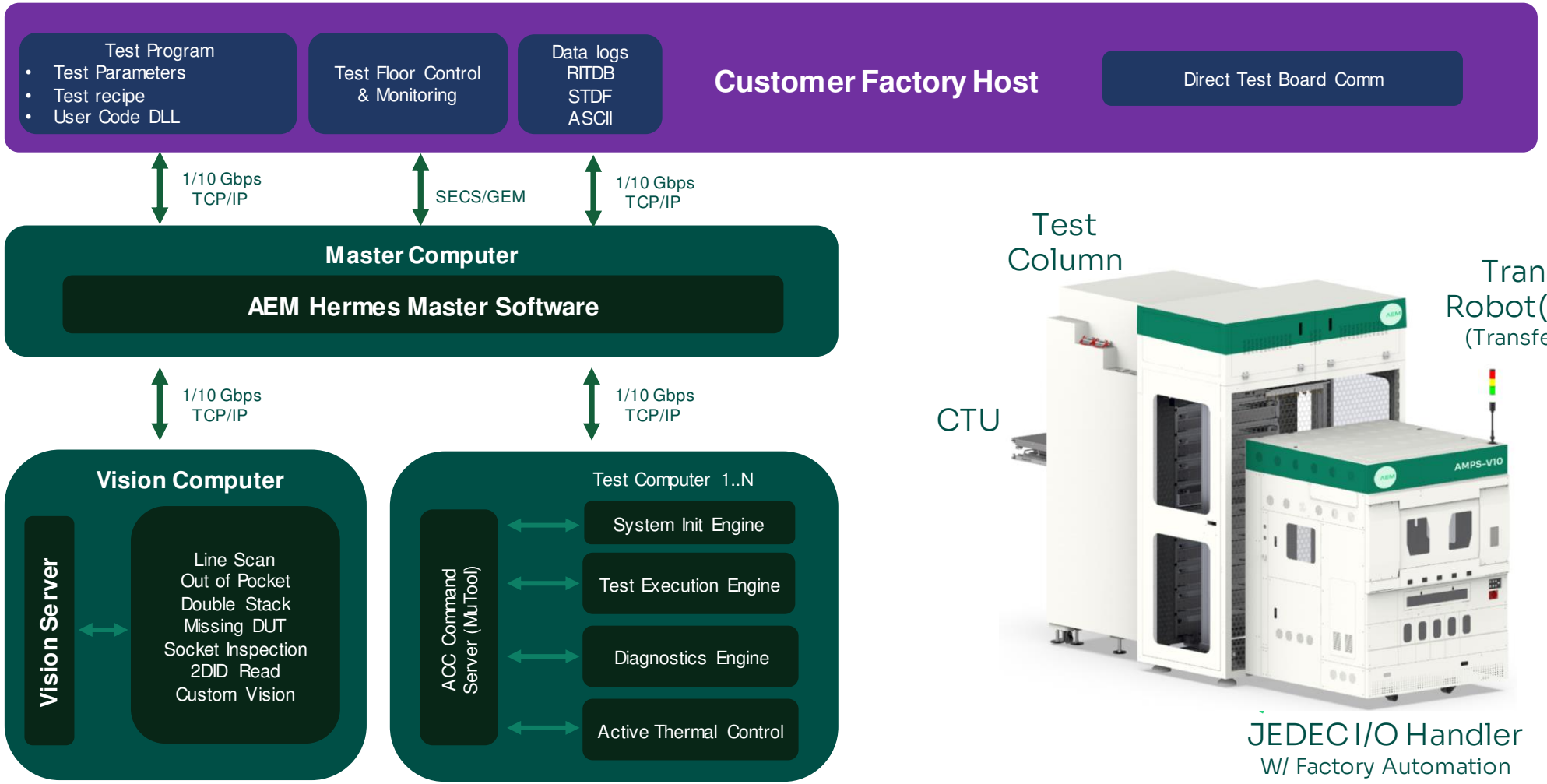
High Volume Manufacturing Solutions

SLT HVM System's

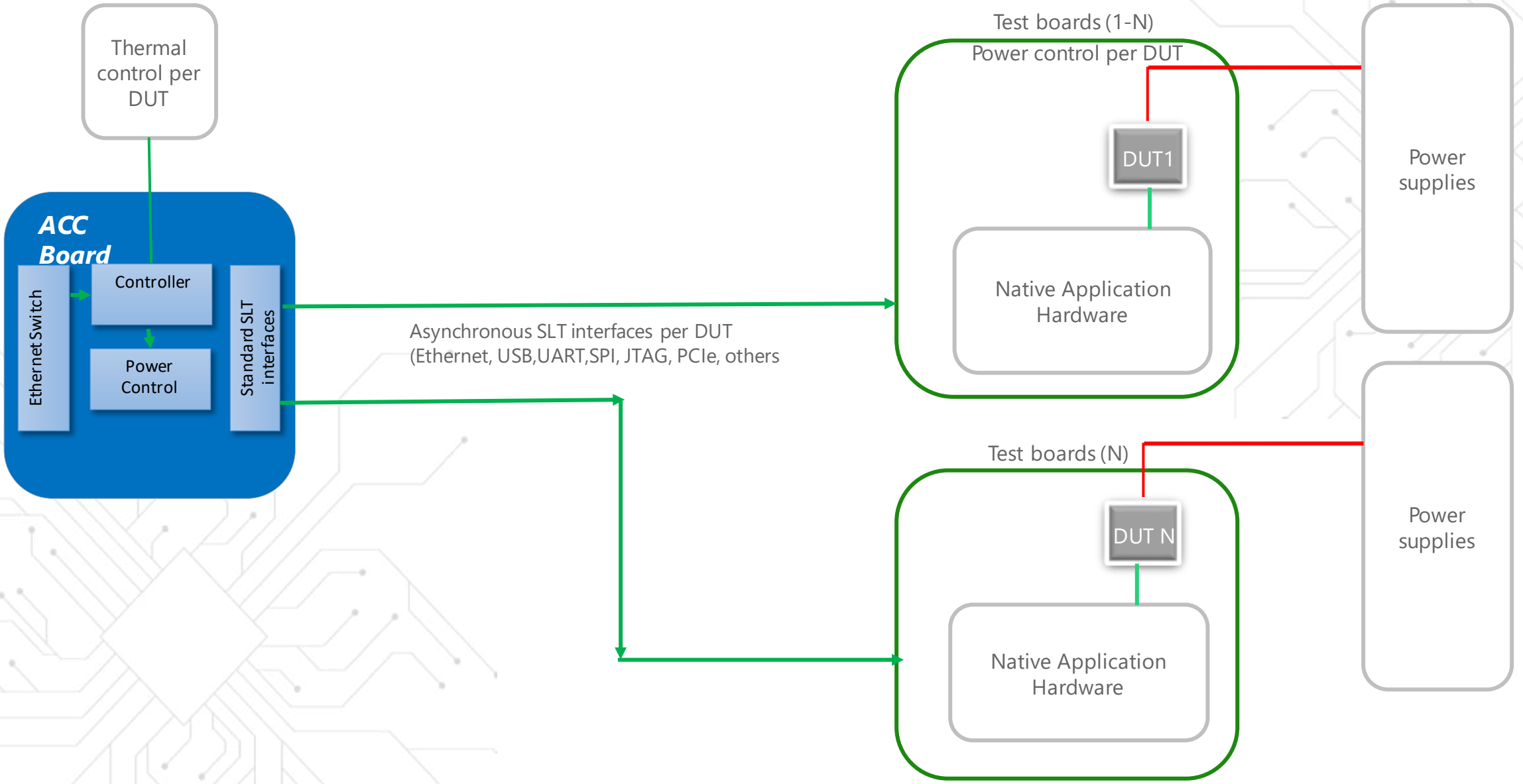
- Jedec tray I/O handler and binning
- Transfer Robot PLC control and monitoring
- Test column PLC control and monitoring
- Vision control and monitoring
- Test control and monitoring
- Test development and debugging
- Thermal control and monitoring



AMPS SLT – Systems Architecture

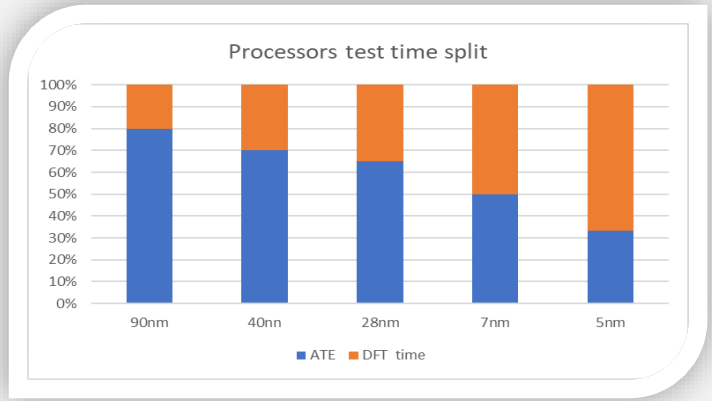


AEM SLT Architecture

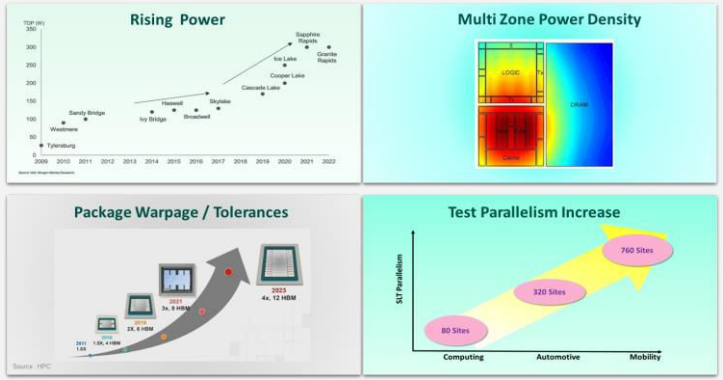


AEM's Test 2.0 Mission → Disrupts the legacy cost of test paradigm

Processor Technology Trends

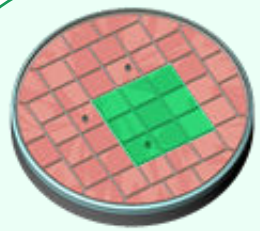


DFT content *(as a % of test time)* is increasing as technology nodes shrink



Multi-Chiplet based High Power Processors

AEM's Test 2.0 Flow Focus



AEM Coverage

Data Analytics & Management

"Expanded" Wafer Test — DFT

"Focused" Final Test — DFT

Burn In+ / HTOL — DFT

High Parallel SLT+ — DFT

Optimizing Test Content Across All Test Insertions

Thank You

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