TESSOLVE
A Hero Electronix Venture

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FIRST BIN

A Newsletter for the
Semiconductor Engineering Community

Contents

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Dear Customer,

Hope you and your extended family are doing safe and healthy. Thankfully the worst of the pandemic is behind us, and we are back to meeting in person!

As most of you would know, our semiconductor industry is one of the industries to have been positively impacted in this phase. Tessolve has also grown substantially in this phase. We continue making all the investments necessary to be your preferred platform company for silicon productization and have taken all measures in this regard.

We have welcomed Huzefa Cutlerywala as SVP of worldwide sales and Madhav Rao as SVP of IC Design. Both are veterans of ASIC business and align with our aim to become a full-fledged ASIC solution provider. In the last few years, we have won multiple ASIC projects from top-10 semiconductor companies, and our ASIC project pipeline is growing. Our IC design engineer headcount has reached 800+, and we are on track to have 1000+ trained IC design engineers in the next few months. We have also acquired to strengthen our physical design team (100+) and are in the final phases of acquiring a European headquartered company to improve our presence in Europe.

Our new state-of-the-art Test labs in San Jose and Austin have started operations with advanced testers and handlers. Customers book these testers for rental and production tests and give turnkey projects. With the inauguration of these two labs in the US, we have a tester presence in the US (both east & west coast), Malaysia, Singapore & India with more than 20 different tester combinations. Also, our centers in the Philippines, Vietnam, and Romania are going strong. We are focused on providing the best of engineers and testers to turn your ideas into action and be the best Test engineering company in the world.

We have grown significantly in Embedded business as well. From a team of 150+ engineers, we have grown to 400+ engineers. Now, we are a force to reckon with in Automotive, post-silicon validation, and avionics. Our collaborative development in post-silicon and automotive space with the few most significant companies in the world is going full stream and getting the attention of other big players.

Our PCB engineers are getting accolades from different customers for their superior and complex board-building skills. Siemens has recognized us in their 28th Xcelerated Technology Innovation awards in the telecommunications category. Most of the industry expert judges had not seen this kind of complex board design. The PCB was a 54-layer stack-up with a 0.35mm pin pitch, meticulous crafting of high-density routing, and a thoughtful approach to power integrity and distribution.

We are constantly renovating ourselves to provide the best engineering solutions to you. We are one of the best companies in the industry on customer NPS scores and would need your support to keep the same trend. This is a testament to our strong partnership with our customers and our employee's dedication to putting the Customer first in everything we do.

Best Regards,
Srinivas Chinamilli
Co-Founder & CEO
Tessolve Semiconductor

Tessolve Showcase

1. ATE-BASED HIGH-VOLUME PRODUCTION TEST FOR GAS SENSORS

Ronnel Estrella – Lead Engineer, Test Engineering
Alvin Concepcion – Test Lead, Test Engineering
Kingsly Christopher – Sr. Director, Test Engineering

Abstract

Sensors are devices that detect and respond to changes in an environment. A typical intelligent sensor in IoT, IIOT, and mobile, wearable applications have Analog Front End (AFE), Microcontroller Unit (MCU), and Communication interface. The sensor inputs are from various sources, such as light, temperature, and gases. The data sensed is collected after booting the device firmware. These data are then uploaded to the cloud for further processing, such as sending an alert to the end user. This paper discusses a low-cost Automated Test Equipment (ATE) based scalable high-volume test solution for a gas sensor that detects and measures Carbon Monoxide (CO). The interaction with the sensor is through I2C frames and SWD. Test conditions for the gas sensors were set up through UDP packets. These were developed using the tester's software. The final solution is then integrated into existing architecture.

Introduction

The work at Tessolve Singapore Lab involves ATE to stimulate the test environment conditions of the gas chamber where multiple sensors under test were placed in a test card (Figure1). The chamber can hold multiple test cards. Each test card can be used to test 560 units. The ATE sends UDP (User Datagram Protocol) packets over the network to request a server to set various chamber environment conditions such as temperature, gas concentration, type of gas, etc. The sensor's firmware is programmed through the ATE. Upon booting, the sensors do the necessary data collection while subjected to different test environment conditions. The data from the sensors are collected and decrypted by the ATE before dumping the data into customized log files. The log files have detailed information on the test results and the conditions to which the sensors were subjected. The test conditions will be recorded through UDP messages that run in parallel while the test data is being collected from the sensor through an I2C interface.

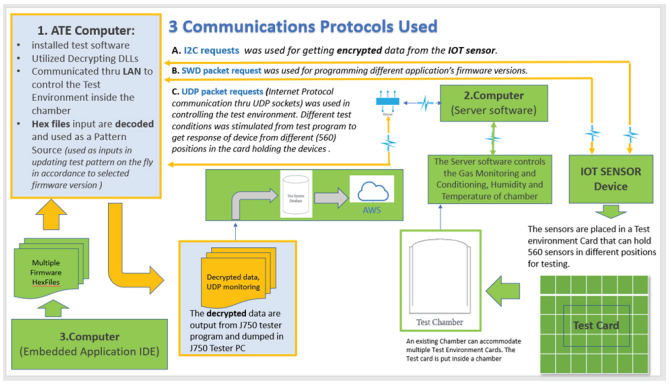
Approach

The typical programming setup of an IoT device using IDE (Integrated Development Environment) is shown in Figure2. The scalability and parallelism of ATE to test the volume of devices is leveraged to test 560 units. With the tester PC's network interface, a UDP software client was created, and Internet Protocol was used to communicate with the server, establishing the stimulus environment inside the chamber.

SYSTEM ARCHITECTURE

The high-level block diagram in Figure 1 was presented with distinction in color to highlight Tessolve Singapore Lab's work in the integration. The green colored blocks represent the existing architecture.

Figure1. Functional Block with Computer Setups



Note: The works created by Tessolve Singapore Lab are highlighted in color orange.

The three computers are shown in Figure1 to show the different subsystems.

Computer1: Tester PC

The tester program in this PC communicates to the server PC through UDP. The SWD data packets are created by decoding the Hex Files copied to this computer. The logs and decrypted files are stored on this computer.

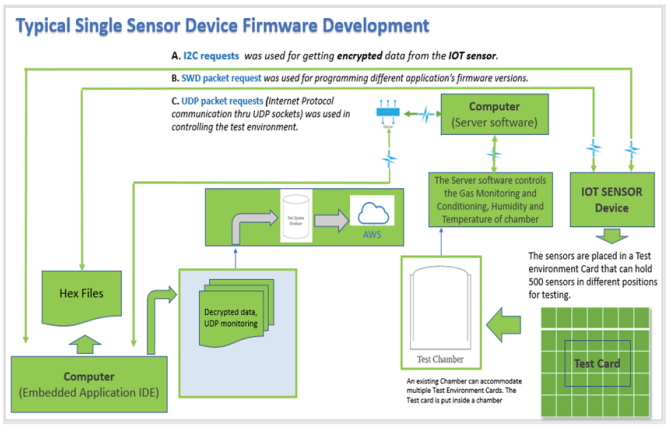
Computer2: Computer with Server Software

This computer contains the server program. This is connected to the same LAN as the tester's PC.

Computer3: Computer with IDE

The firmware Hex files are generated in this PC.

Figure2. Typical Firmware programming without ATE



Conclusion

This ATE-based high-volume scalable test solution can be used to test IoT gas sensors in the order of 560 units under actual application environment conditions. A typical fully configured ATE can support testing up to 8960 units.

Tessolve Engineering Challenge Contest

1. EFFECTIVE PCB DESIGN APPROACH FOR FINE PITCH ICS TARGETED TOWARDS HIGH VOLUME MANUFACTURING.

Sunil BK – Test Lead, Test Engineering

Abstract

Ever since the invention of CMOS, manufacturing Semiconductor components with smaller form factors and on a given system real estate with reliable, repetitive, and proven techniques is of great significance. That said, while High Volume Testing via ATE's the industry has matured with more stable measurement techniques, the test community should also focus on the challenges of a MultiSite Test Interface PCB and its Power/Current Handling capacity that could potentially affect the Test Performance and Reliability cum LifeSpan of this hardware.
This article focuses on one such area as an awareness mainly towards understanding the PCB hardware design limitations and a simplistic resolution on how the Test & PCB Design engineers could apply their relevant applications.

Detailed Description:

In this case study, we are referring to a 32-Site HVM Test solution for a conventional 6-terminal LoadSwitch (Die size = 0.778mm X 0.778mm, pitch = 0.4 mm).
LoadSwitch Ron generic Test Condition:
· Force Current I1= 200mA, Measure V1
· Force Current I2 = 1mA, Measure V2
· RON = -ΔV/ΔI = Abs[(V1-V2)/(I1-I2)]

While designing a Multisite PCB of 32-Sites with such a small form factor, the Trace Routing b/w individual nets of the DUT must follow 3x clearance to the adjacent tracks, limiting the Trace Width.

Root cause analysis:

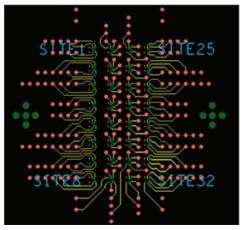


Fig1: 32 Site PCB Layout Footprint

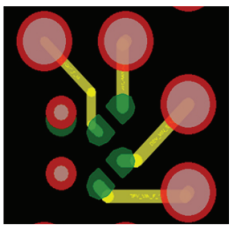


Fig2: CloseUp took of Single Site

However, reducing Trace Width would limit the current carrying capacity. The relevant Test cum PCB Design engineers should be cautious of the desired Force Current (further Guardbanded with Ipeak/Irms).

A glimpse of Trace Wear Out due to improper Cu Thickness as illustrated below:

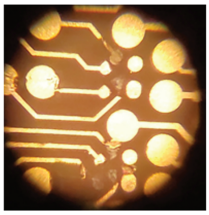


Fig3: Image of burnt traces

Given a such scenario, an optimized approach is followed to increase the effective Area of the Trace but without change in the Trace Width, thereby choosing the appropriate Copper Thickness during PCB Fabrication from Standard 1oz/to, say, 1.2oz /2oz.

The table below shows the Trace Width thickness (INT/EXT) vs. the Cu Thickness.

Sr.No.	I-DC (A)	I-AC (DC *1.414) (A)	Cu Thickness (Oz)	Trace Width-INT Layers (mils)	Trace Width-EXT Layers (mils)
1	0.2	0.2828	1	3.34	1.28
2	0.2	0.2828	1.2	2.78	1.07
3	0.2	0.2828	1.5	2.23	0.85

Conclusion:

High reliability of the HVM targeted PCBs that often foresee dense cum stringent routing constraints owing to their small form factor can be achieved with Adhoc planning b/w Test & PCB Design engineers alongside PCB Manufacturing house to further guardband for targeted operating specifications.

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Thank You !

India | USA | UK | Germany | Romania | Thailand | Malaysia
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