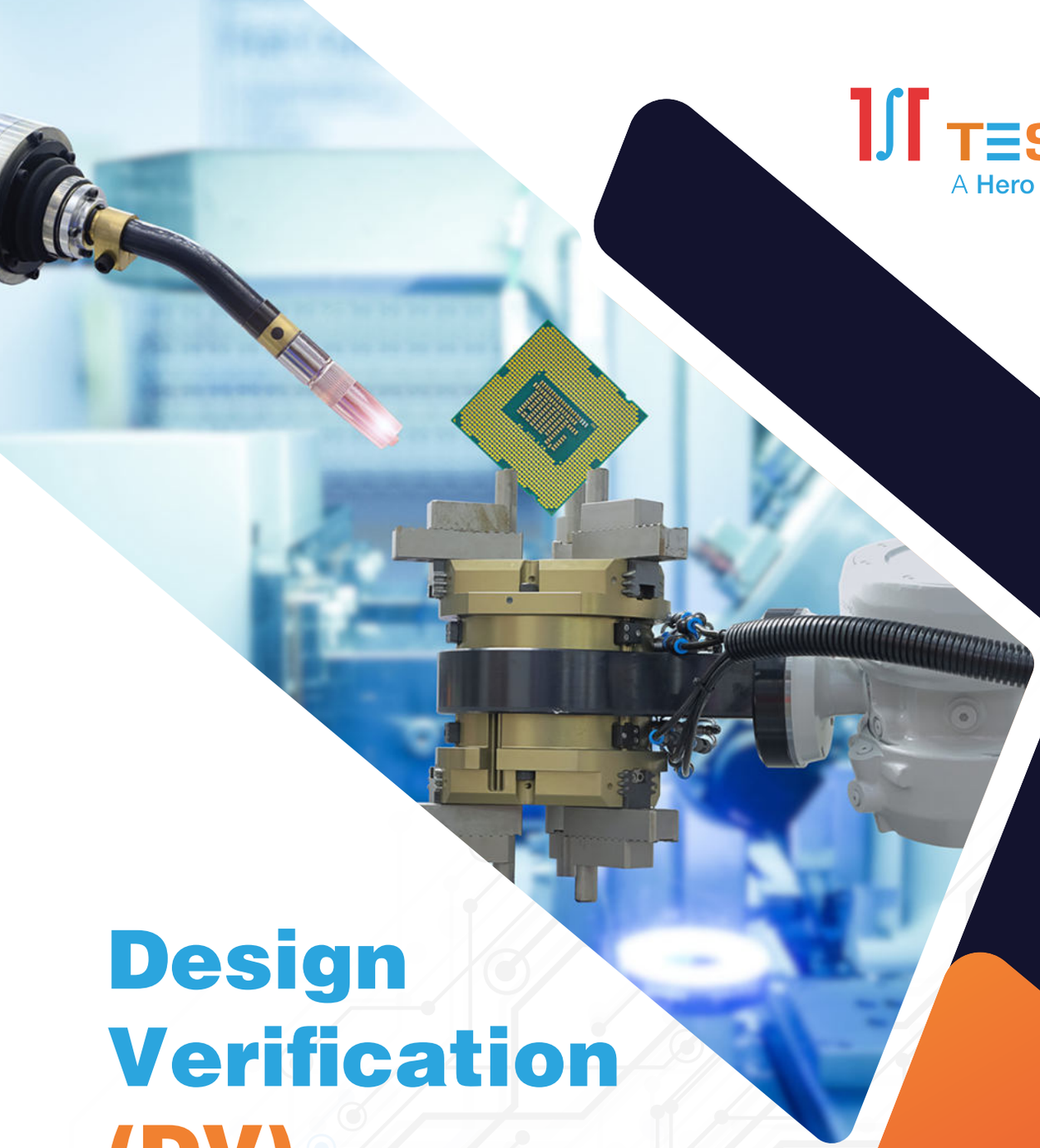
TESSOLVE
A Hero Electronix Venture



Design Verification (DV)

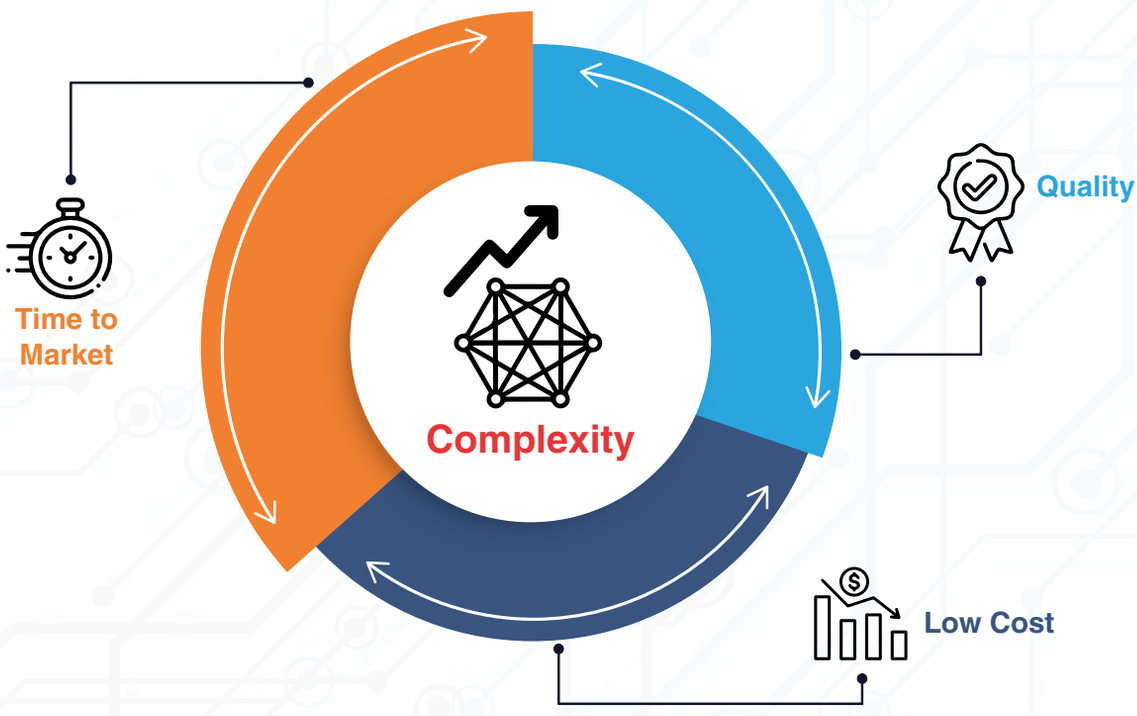
How to improve quality whilst reducing costs and Time to Market?

Hardware Verification is the process of checking the design functionality for the given specifications. It is one of the largest tasks in silicon development and has the biggest impact on the key business drivers of quality, schedule, and cost. The Tessolve verification offering covers all aspects of the Verification flow from feature extraction to coverage closure and is equipped with custom-designed verification productivity tools for reducing verification turnaround times. Tessolve brings verification expertise across multiple industry verticals spanning Consumer Electronics, Wireless, Data Centre, Automotive and Memory/Storage segments.

Tessolve Value Proposition

Value Proposition in Verification

- Improved effective, efficient verification
- Improve quality
- Reduce costs
- Improve time-to-market



Team Size

We have a Design Verification Team Size of around 350 Engineers with skills in the following

- IP level Verification
- AMS Verification
- Full chip Verification
- Verification across verticals– Automotive, Data Centre and HPC, Graphics, and mobile platforms, to name a few.

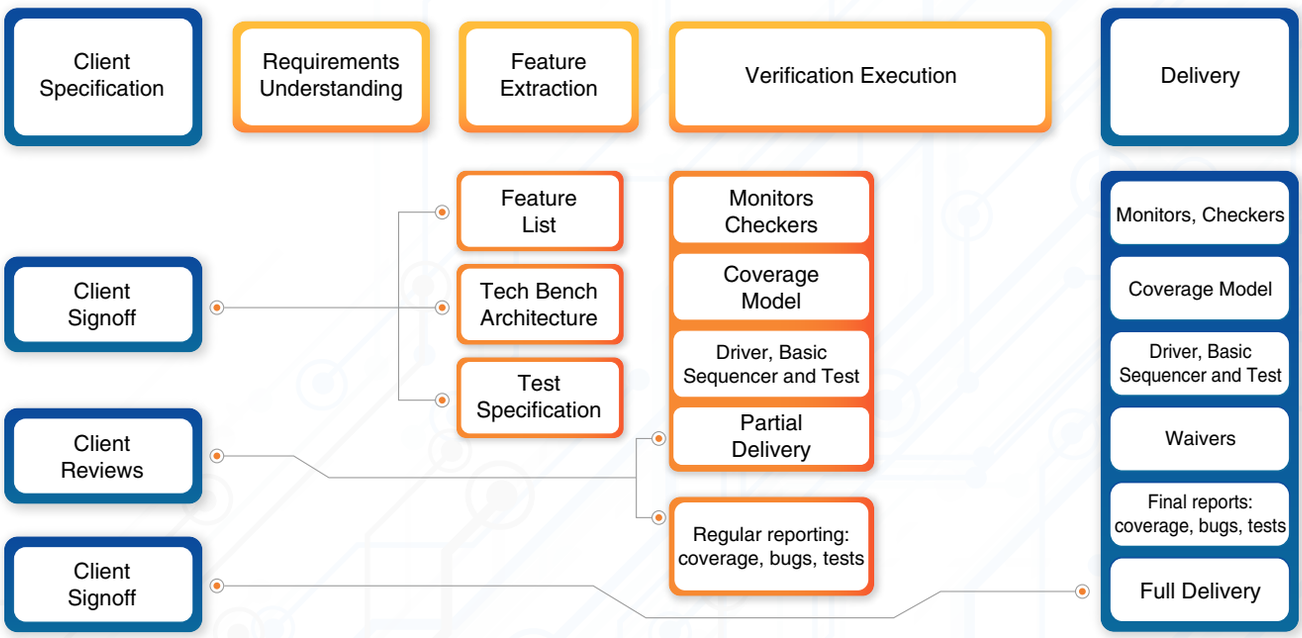
Tessolve Verification Expertise and IP

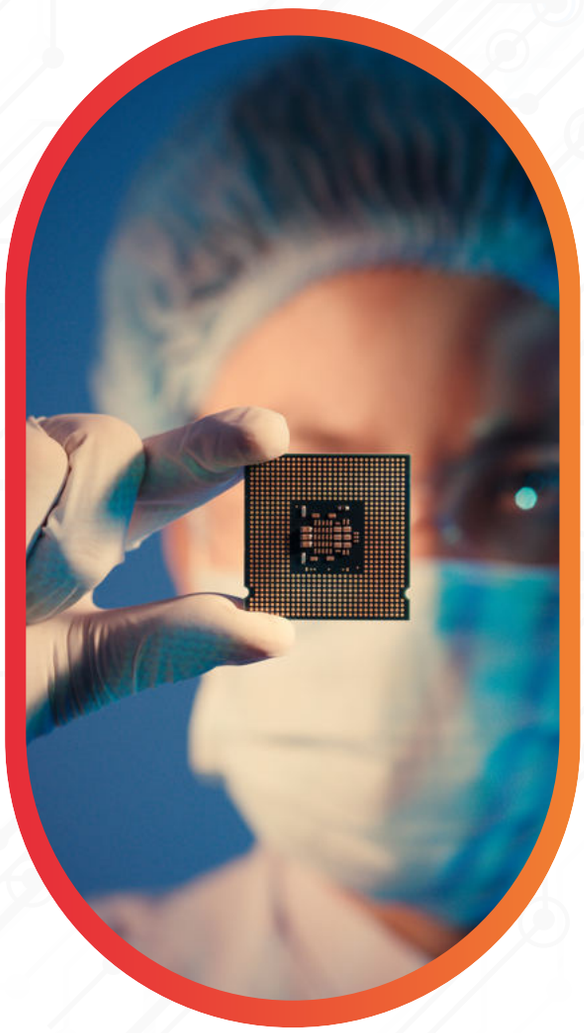
- Verification IP and verification efficiency tools for Verification productivity
- Verification frameworks for SoC verification and AMS verification
- Specialist verification services for formal verification deployment, portable stimulus (PSS) and a verification methodology audit
- Consultancy programs and continuous improvements through benchmarking
- Training on verification strategy and the latest verification methodologies.

Offshore Development Centre

- Build expertise within the team
  - o Retain team
- Value add services
- Run multiple projects in parallel
- Expand teams quickly
  - o Cope with growth
  - o Can also shrink the team

Verification Design Flow





Verification Improvement

Portable Stimulus Standard

Improve Verification Reuse:

- Hierarchy (block, subsystem, SoC, system)
- Platform (simulation, emulation, FPGA, Silicon)
- Project (reuse from one project to the next)

Tessolve collaborate with tool suppliers

- Cadence, Breker

Formal Verification

- Development of a Formal Verification Strategy
- Full Formal Verification of complex IP Blocks
- Automate checks at SoC level
  - Connectivity, X propagation, power checks, etc.

Verification Audit

- Audit current verification practises across the organisation
- Identify and agree potential improvements
- Establish low overhead, best-practise verification processes

Recent Projects Delivered

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802.3 IP level Verification

Tessolve's client offers a broad range of chip offerings for data center, networking market

Tessolve was selected as a preferred vendor for verification of multiple generations of the client's 802.3 controller IP

Layers Verified: PCS for 10Gbps, 25Gbps, 40Gbps, 50Gbps, 112.5Gbps
CL74 FEC for 10Gbps, 40Gbps
CL91 RSFEC for 25Gbps (528,514), 50Gbps (544,514), 112.5Gbps (544,514), 112.5Gbps (4080,3855)

Key Features Verified: PCS: 64b/66b Encode Decode State Machines, Scrambler, Block Distribution and AM insertion for 40G, PCS Lock State machine FEC and RFSEC: FEC Lock state machine, AM lock state machine, Error indication and correction combinations

Achievements: Debugged multiple complex SerDes issues, Verification closure with 100% functional coverage and code coverage is done by writing directed test case to cover the holes in coverage

PCIe Subsystem Verification

Tessolve Client offers a portfolio of semiconductor and system solutions

Tessolve was selected as a preferred vendor for verification of multiple generations of the PCIe subsystem

Layers Verified: Transaction Layer, Data Link Layer, Physical Layer

Key Features Verified:
x1, x2, x4, x8, x16 PCI Express Core, Link rates of 2.5, 5.0, and 8.0 GT/s per lane, 8-bit, 16-bit, and 32-bit PIPE interface, PHY Interface for PCI Express (PIPE) 3.0, Revision.4.4 compliant, Design for Endpoint, Root port and dual mode/shared silicon, Integrated Clock Domain Crossing (CDC) to support user-selected frequency for the Bridge

Achievements: Developed UVM based Verification Environment, Responsible for bring-up of GEN1, GEN2, GEN3 and GEN4 environments , Integrated PCIe EP and RC IP with third party RC and EP VIP respectively with common SERDES, Developed Test Plan with around 500 test cases to verify all the above features for all the Speed Modes

SERDES Verification

Client offers a comprehensive portfolio of semiconductor and system solutions for the communications, defence & security, aerospace and industrial markets

Tessolve was selected as a preferred vendor for verification of SERDES for client's test chips across 7nm and 16nm nodes

Verification Modes:
16 Lanes with 4 MLD IP instantiations connected to 2 SerDes instances; 8 Lanes with 2 MLD IP instantiations connected to 1 SerDes instance; 48 Lanes with 12 MLD IP instantiations connected to 6 Osprey SerDes instance

Verification Challenges
Running various SerDes functionality related test scenarios such as PRBS tests for various data rates

Achievements
Debugged multiple complex SerDes issues

Developing and executing verification plans for multiple lanes operating at multiple speeds

Achieved verification closure with 100% functional coverage and code coverage

For More Details Please Visit:
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