TESSOLVE
A Hero Electronix Venture

Design for Test/ Debug (DFT/DFD)

Our team of Design for Testability experts can help increase IC test coverage, yields and quality.

Design for Testing (DFT) and Debugging (DFD) are critical stages in the micro-architectural phase of a design. Working in tandem with a client's design team, our experts understand the structure of the chip which enables them to create the complete DFT and DFD architecture.

Involving in early stage of architecting

- Improve design testability & Coverage
- Scoping reduction test costs

- Improve time to market
- Despite considering complexity
- Address domain specific methodologies

DFT & DFD – The Highlights

Team

Our team includes highly skilled and experienced professionals ranging from project managers, testers, programmers, designers, and developers.

Design Solutions

- Multiple Clock and Voltage Domains
- Mixed signal low speed and high-speed designs
- Power sensitive designs
- Embedded processor-based designs
- Complex Analog testing includes SERDES, DDR and A/D, D/A converters

Technical Advantage

- Adept at handling standard EDA tools for MBIST, LBIST, SCAN, COMPRESSIONS, ATPG, JTAG & iJTAG. from Mentor Graphics, Synopsys, and Cadence
- DFX Verification frameworks for
  - SOC Verification
  - And AMS Verification

Specialist in DFT Architecture

- Hierarchical & Compression SCAN
- iJTAG/JTAG based MBIST networks
- DfX frameworks to address macros (OTP, EFUSE, PLL, LDO)
- High speed IO (PCIE, USB, MIPI, DDR, SERDES)

Offshore Development Centre

- Build expertise in team
  - Retain team
- Value add services
- Run multiple projects in parallel
- Expand teams quickly
  - Cope with growth
  - Can also shrink the team

Tessolve asureDFT Services Overview

Continuously shrinking process nodes have introduced new and complex on-chip variation effects creating new yield challenges. Combined with ever-increasing design complexity with multiple memories, mixed signal blocks and IPs from multiple vendors crammed into a single SoC, Design for Testability (DFT) implementation and signoff has become a major challenge. The Tessolve asureDFT services suite helps you overcome these challenges by establishing a DFT strategy that delivers improved DFT execution quality and reduced time-to- market.

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asureDFT Portfolio Expertise

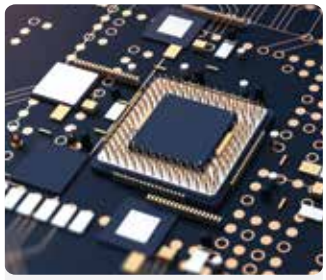
Services	• Scan (Compression/ non compression based on structure of the device and test time requirements) • ATPG (stuck at, at speed or new faults based on the technology and strategy) • Memory BIST with industry standard EDA tools • Logic BIST
Training	• DFT Strategy/Structural Testing • Exclusive trainings on JTAG, BSCAN, SCAN, MBIST • Customized contents for customer requirements
Off the shelf Components	• JTAG TAP based test controllers and verification frame works (JTAG, IEEE 1149, TAP and its customized Instructions) • Test suites for Verifying BSCAN • Generating Tester compatible vectors for Post Si validation (ATE) • Format conversions with ATE logs for diagnosis
Development of DFT Methodology	• Support to develop your own DFT Strategy/Structural Testing • Experts in developing pyhton, perl based user interactive GUI based DfT flow applications and utilities.
Benefits	• Reduced overhead no need to hire costly DFT resources • End to end support from design to silicon • Off the shelf components reduce DFT turnaround times • Training support • Flexible business models ODC, Re source augmentation, Managed services, Turnkey services

Recent Projects Delivered

Automotive grade micro controllers

- **Technology:** 130nm/180nm
- **Tools:** DC, DFTMAX, Custom memory solution
- **Metrics, Design Details:** Responsible for DFT team implementing run time Logic Bist, Memory Bist, Boundary Scan, analog and functional test modes.

  Architecture, Implementation, validation and production ramp, FA support



Processors. Multiple devices

- 10 - 15 billion transistors running, 32 cores at 5GHz, 64MB L3 Cache, > 1TB/s I/O BW
- **Technology:** Multiple nodes 90nm up to 10nm FinFET process
- **Tools:** Mentor ATPG, MBIST
- **Metrics, Design Details:** Defined the new test methodologies to reduce test time and estimate test power to optimize the test flow to manage test economics. DFX, debug and bring up.

Wireless Infrastructure Devices

- Multiple devices Multicore ARM CPU and DSP device ~80 Sq mm , ~300K flops --> 600K FF
- **Technology:** 90nm / 65nm
- **Tools:** DC, DFTMAX, Tetramax ATPG, Custom memory bist
- **Metrics, Design Details:** Complete DFT Architecture, SCAN, MBIST, JTAG, Analog Test, concurrent testing, pre and post layout pattern generation and validation. ATE pattern generation,debug and bring up. Production, FA support.

XG modem chipsets (client project)

- **Technology:** 7nm/14nm
- **Tools:** SPYGLASS, Synopsys, DC, Mentor ATPG
- **Metrics, Design Details :** RTL DFT analysis, DRC checks and fixes, Defining JTAG constraints for scan modes and DFT constraints for scan implementation with pre and post DRC analysis, scan chain balancing and scan compression EDT hook up. Scan coverage analysis and improvement, fault accounting and fault grading.

Tessolve is the market leader in providing engineering solutions for silicon and systems development. We offer a unique combination of both pre-silicon and post-silicon expertise to provide an efficient turnkey solution for silicon bring up, spec to a product. With 2100+ employees worldwide, Tessolve enables customers a faster time-to-market through deep domain expertise in Analog, Digital, Mixed Signal, and RF, broad ATE platform experience, diverse embedded software services and built-in infrastructure including a test floor, characterization, reliability lab, system lab, and PCB FAB. Tessolve delivers ASIC design services including advanced process nodes with a strong eco-system relationship with EDA, IP, and foundries. Tessolve's post-silicon solution takes silicon from the foundry to high volume manufacturing. Our front-end design strengths integrated with the knowledge from the backend flow, allows Tessolve to catch design flaws ahead in the cycle, thus reducing expensive re-design costs, and risks.

Contact For more details **https://www.tessolve.com/vlsi-design** | www.tessolve.com