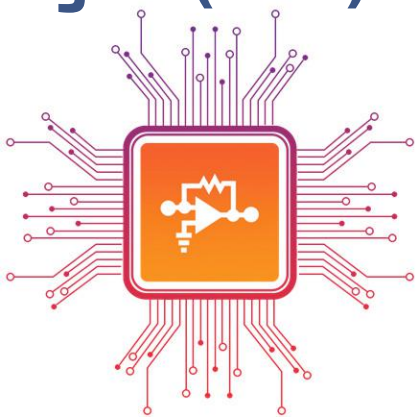
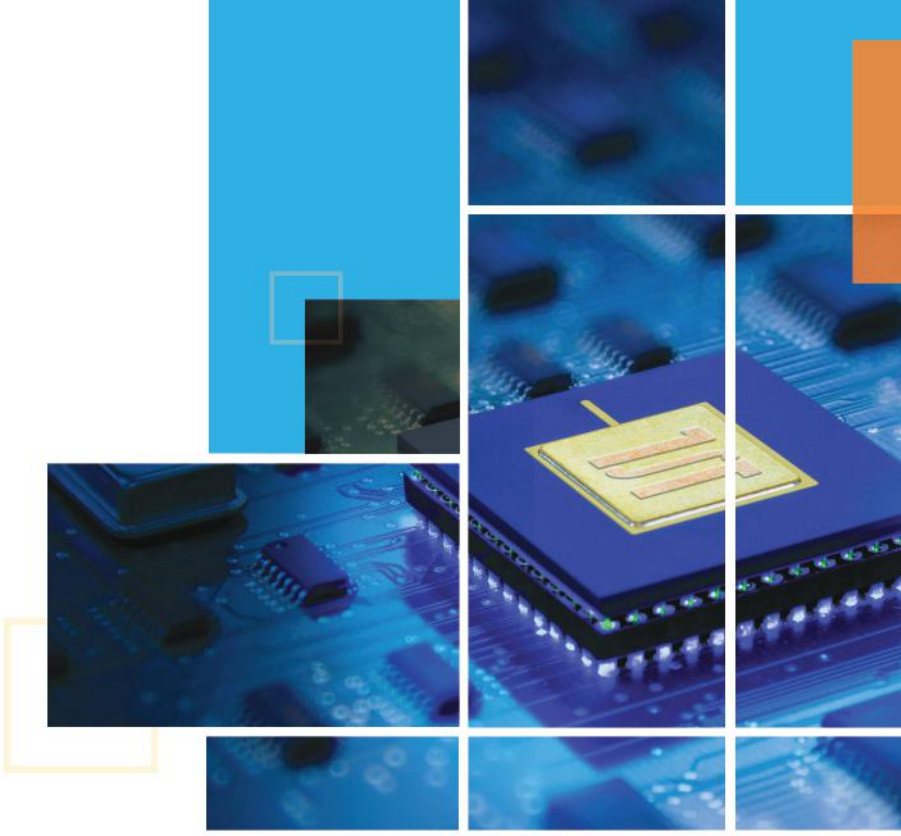
TESSOLVE
A Hero Electronix Venture

Analog & Mixed Signal (AMS) Design





Executing Turnkey Projects – Ownership from Spec to GDS to Silicon

Analog and Mixed signal design team at Tessolve specializes in High quality design for different applications with process nodes varying from 350nm to most advanced 5nm designs. The team has experience in the design of DC-DC converter, LDOs, Phase Lock Loop (PLL), amplifiers, Bandgap reference, High Voltage design and primary fly-back converters. The IPs were developed for different industry verticals like Automotive, Communication, Consumer, Medical, IoT etc. The competent team has rich experience of successfully delivering more than 50+ silicon proven Analog chips during last few years with full ownership of the delivery from Spec to GDSII sign off, supported with silicon validation to global semiconductor companies.

Analog and Mixed Signal Design Product Domain Expertise

Power Management

- PMIC (Power Management IC)
- DC-DC Converters (Buck, Boost, Buck-Boost)
- Charge Pump, LDOs
- Primary Fly-back Converters
- High Voltage Design

Data Converters

- Sigma Delta Converters
- Sub-Sampling ADC
- Pipeline ADC
- Cyclic ADC
- SAR ADC
- Current Steering DAC

Serial Interfaces

- SERDES Standards
- LVDS PHY TX/RX
- CAN/LIN Transceiver
- Power Line Communications

PLLs & CLOCKS

- Integer & Fractional PLLs
- Clock Generator for SoCs
- Ring Oscillator up to 5 GHz
- Clock Buffers

Value Proposition

Team Skills

- Analog Circuit Design
- Layout Design
- Macro Modelling

Design Solutions

- Feasibility Study
- Macro modelling
- Circuit Design
- Layout: RF Layout, IO Design & Layout, Standard Cell Design & Layout
- Centre of Excellence to build primitives

Technical Advantage

- **Technology:** CMOS/ BiCMOS
- **Process Nodes:** 7nm - 0.5um
- **Foundries:** TSMC/ Intel/ GF/ TowerJazz/ Dongbu/ XFAB
- **EDA Tools:** Cadence/ Synopsys/Mentor/ Apache

Foundation IPs / Library Development

Developing full IP & Block level

- Standard Cells
- I/O s
- Memory
- Technology Migration

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Recent Projects Delivered

4A Buck Converter

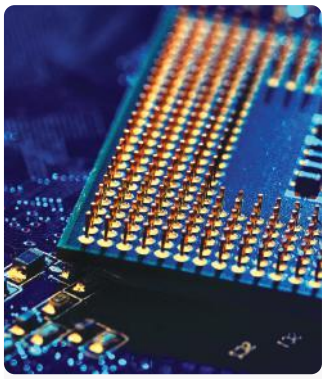
- Technology node: 65nm, TowerJazz
- It is a standalone DCDC Buck converter used for PCIe/Server side applications, Load current of up to 4A
- No external inductor needed
- User configurable transient response
- Wide Input voltage 4.5V to 16V
- Wide output voltage range 0.6V to 5V
- Efficiency > 85%

10-Bit SAR ADC

- 10-bit 160/80/40 MSPS IQ ADC
- Single Channel Async SAR ADC
- Low-power for IoT applications
- Design is applicable from 65nm-22nm CMOS process
- Internal Bandgap and Biasing system
- Segmented DAC with VCM switching technique

1.8V low noise LDO

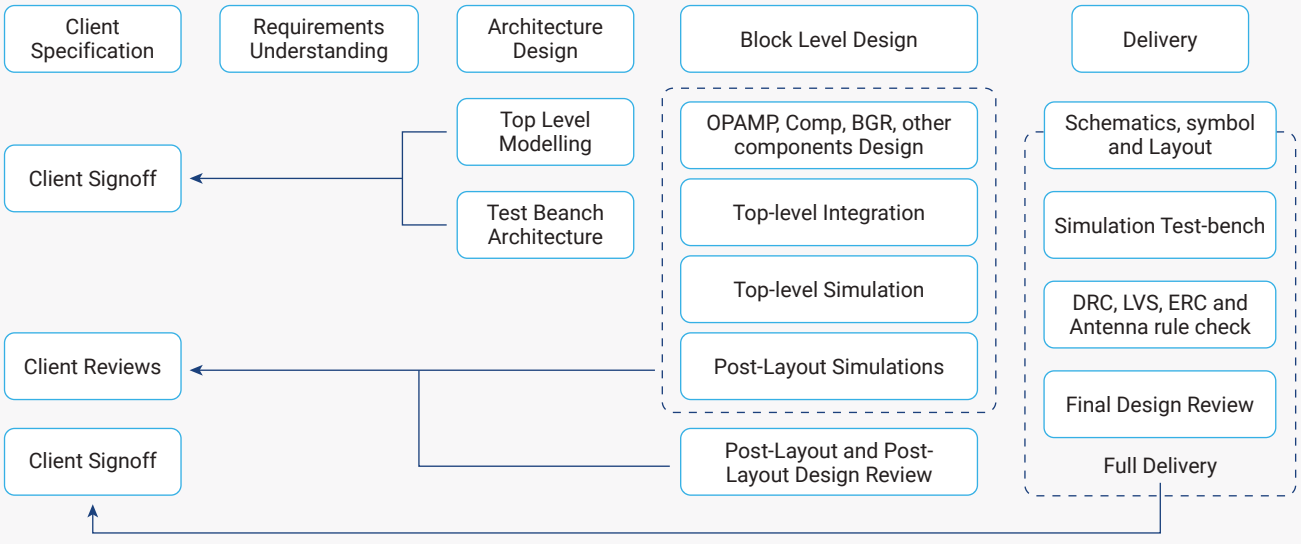
- Technology node: 40nm, GF
- It is a standalone LDO regulator for Automotive applications
- Load current 1A
- Low noise output
- High PSRR > 40dB
- nput voltage from 2.7V to 3.3V
- Output voltage: 1.8V



Serdes and High Voltage Design

- 10 channels of 28Gbps Serdes for server application in TSMC 28nm process
- 16G Multi-Protocol SERDES PHYs in GF 28nm
- Implemented on chip high speed serializer, deserializer and output driver
- 2.3 GHz, 1.2 GHz, 266 MHz PLL
- Primary side fly-back converter

Analog Design Flow



Tessolve is the market leader in providing engineering solutions for silicon and systems development. We offer a unique combination of both pre-silicon and post-silicon expertise to provide an efficient turnkey solution for silicon bring up, spec to a product. With 2100+ employees worldwide, Tessolve enables customers a faster time-to-market through deep domain expertise in Analog, Digital, Mixed Signal, and RF, broad ATE platform experience, diverse embedded software services and built-in infrastructure including a test floor, characterization, reliability lab, system lab, and PCB FAB. Tessolve delivers ASIC design services including advanced process nodes with a strong eco-system relationship with EDA, IP, and foundries. Tessolve's post-silicon solution takes silicon from the foundry to high volume manufacturing. Our front-end design strengths integrated with the knowledge from the backend flow, allows Tessolve to catch design flaws ahead in the cycle, thus reducing expensive re-design costs, and risks.

Contact For more details **https://www.tessolve.com/vlsi-design/**