CAN Bus

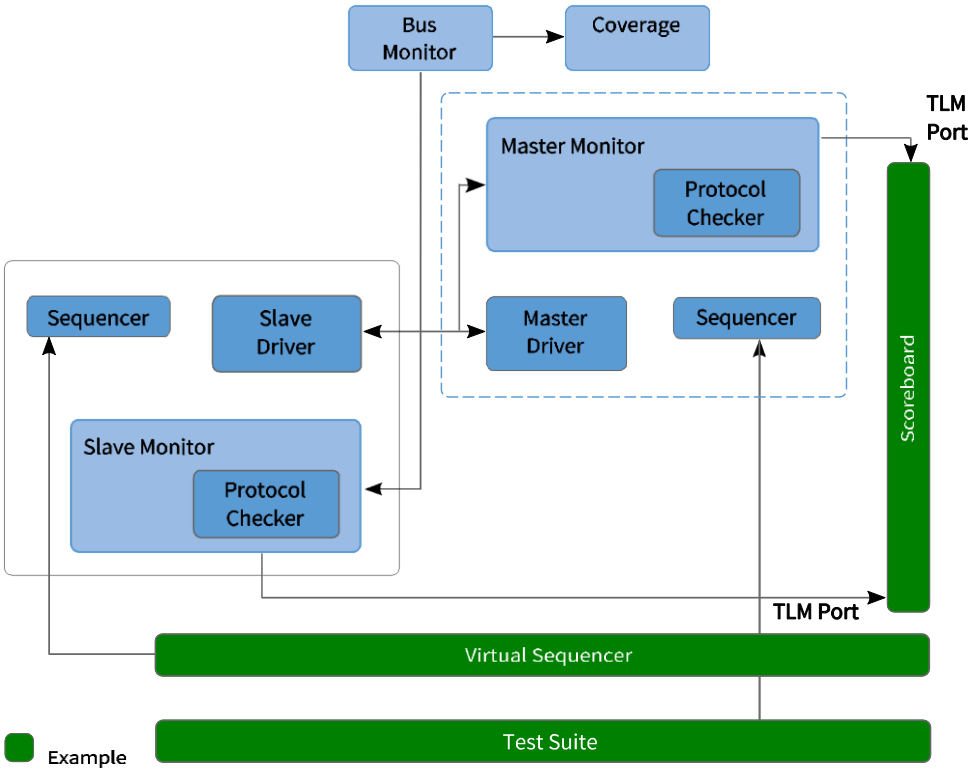
asureVIP

CAN Bus 2.0 Master and Slave UVM VIP

Tessolve offers a UVM-based CAN 2.0 Master and Slave VIP as part of its asureVIP series of offerings. This is a highly flexible and configurable verification IP, which can be easily integrated into any SOC verification environment. The Can Bus VIP has been interoperability tested with both Slave and Master VIP configurations.

The VIP comes with a Bus Monitor for performing all protocol checks. The monitor also performs key protocol checks and reports errors for non-compliance with CAN 2.0 Part A and B Specification.

Block Diagram



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TESSOLVE
A Hero Electronix Venture

Overview

VIP:	CAN Slave or Master
Compliance:	CAN V2.0 Part A and B CAN FD V1.0
Language:	System Verilog
Methodology:	UVM 1.1
Simulators:	Cadence Incisive, Mentor Questa and Aldec Riviera PRO

Deliverables

- CAN 2.0 UVM VIP
- Sample Testbench integrated with proven XILINX CAN 2.0 IP
- Sample Scoreboard
- Sample Virtual Sequencer
- VIP user guide

Key Benefits

- Highly flexible, independent and configurable CAN 2.0 VIP
- Tested against silicon proven VIP
- Less TAT in integrating into SOC Verification environments

Technical Specifications

- CAN 2.0 (A/B) and CAN FD 1.0
- Bit rates up to 1 Mb/s
- Two reset mechanisms
  - Software reset
  - System reset
- Transmit message First In First Out (FIFO) with a user-configurable depth of up to 64 messages
- Transmit prioritization through one High-Priority Transmit buffer
- Automatic re-transmission on errors or arbitration loss
- Acceptance filtering (through a user-configurable number) of up to 4 acceptance filters
- Supports Normal and Configuration modes
- Supports Sleep Mode with automatic wakeup
- Supports Loop Back Mode for diagnostic applications
- Supports Maskable Error and Status Interrupts, Readable Error Counters, Bit Timing Logic and Bit Stream Processor

Other VIPs Available

- ARM: AXI, APB, AMBA ACE and CHI
- Hi-Speed Interface: Ethernet (10/100/1000MB & 10GB), PCIe RC and EP, USB 3.0 Host and Device, CSIX and SPI
- Memory and Storage: SDCARD 4.0, DDR 4/3, LPDDR 4/3 and ONFI
- MIPI: DPHY, DSI, LPDDR, MPHY, SMBUS, RFFE and Unipro
- Universal Serial I/O: CAN, GPIO, I2C, UART, SPDIF, I2S, SMBUS, SPI and TDM

Independent Verification Service

Tessolve can deliver an independent verification service that not only reduces development costs and time-to-to-market, but also improves product quality.

Proven Implementations

Use asureVIP with the confidence of knowing that they have been successfully deployed by leading SoC companies around the world.

About Tessolve

Tessolve Semiconductors Private Limited provides services and products to organizations developing complex products in the microelectronics and embedded software and systems industries.

Tessolve operates globally with offices in the UK, France, Germany, India, Singapore, Japan, the USA plus a network of international partners.

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