I2C Master / Slave

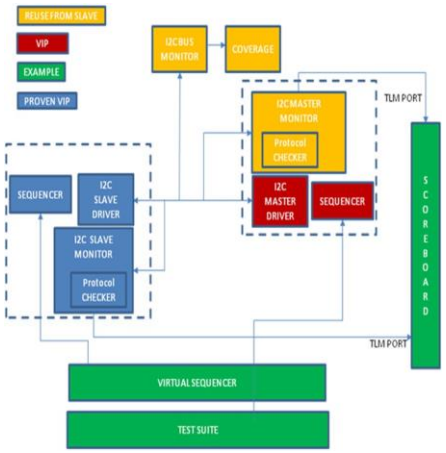
asureVIP

I2C Master and Slave OVM/UVM VIP

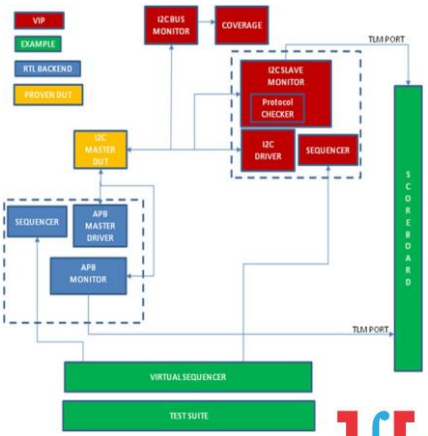
Tessolve offers I2C OVM/UVM Master and Slave VIP as part of its asureVIP™ series of offerings. This is a highly flexible and configurable verification IP, which can be easily integrated into any SOC verification environment. The I2C VIP supports standard, fast and high speed modes of operation. It also supports 7-bit and 10 -bit addressing modes. The Master VIP has been interoperability tested with a Slave VIP configuration. This slave VIP was used in successfully verifying a DUT, later silicon proven.

The VIP comes with a Bus Monitor for performing all protocol checks. The monitor also performs key protocol checks and reports errors for non compliance with Philips I2C Specification.

Master
Block Diagram



Slave
Block Diagram



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TESSOLVE
A Hero Electronix Venture

Overview

VIP:	I2C Master or Slave
Compliance:	UM10204 Rev. 4 13 February 2012
Language:	System Verilog
Methodology:	OVM 2.1.1 / UVM 1.1
Simulators:	Cadence Incisive, Mentor Questa and Aldec Riviera PRO

Deliverables

- I2C Master or Slave OVM/UVM VIP
- Sample Testbench integrated with proven I2C Master or Slave IP
- Sample Scoreboard
- Sample Virtual Sequencer
- VIP user guide

Key Benefits

- Highly flexible, independent and configurable VIP
- Tested against silicon proven VIP
- Less TAT in integrating into SOC Verification environments

Technical Specifications

- Each master or slave device connected to the bus is software addressable by a unique address and simple master/slave relationships exist at all times
- True multi-master including collision detection and arbitration to prevent data corruption if two or more masters simultaneously initiate data transfer
- Serial, 8-bit oriented, bi-directional data transfers can be made at up to 100 Kbit/s in the Standard-mode, up to 400 Kbit/s in the Fast-mode, or up to 3.4 Mbit/s in the High-speed mode
- General Call Addressing Support
- Addressing Modes Supported: 7-bit, 10-bit & general call address
- Ability to differentiate between Legal and Illegal Start/Stop conditions
- Wait State Insertion capabilities
- Clock Synchronization of more than two masters connected to the I2C Bus.
- Repeated Start Generation Scenarios
- Repeated Start Detection capabilities
- Bus monitor has capability to detect Illegal Start/Stop/Repeated Start Conditions.
- Switching between different modes (H-Speed, F-Speed and S-Speed)

Other VIPs Available

- ARM: AXI, APB, AMBA ACE and CHI
- Hi-Speed Interface: Ethernet (10/100/1000MB & 10GB), PCIe RC and EP, USB 3.0 Host and Device, CSIX and SPI
- Memory and Storage: SDCARD 4.0, DDR 4/3, LPDDR 4/3 and ONFI
- MIPI: DPHY, DSI, LPDDR, MPHY, SMBUS, RFFE and Unipro
- Universal Serial I/O: CAN, GPIO, I2C, UART, SPDIF, I2S, SMBUS, SPI and TDM

Independent Verification Service

Tessolve can deliver an independent verification service that not only reduces development costs and time-to-to-market, but also improves product quality.

Proven Implementations

Use asureVIP with the confidence of knowing that they have been successfully deployed by leading SoC companies around the world.

About TVS

Tessolve Semiconductors Private Limited provides services and products to organizations developing complex products in the microelectronics and embedded software and systems industries.

Tessolve operates globally with offices in the UK, France, Germany, India, Singapore the USA plus a network of international partners.

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