USB 3.0 Device & Host

asureVIP

USB 3.0 OVM/UVM Device and Host VIP

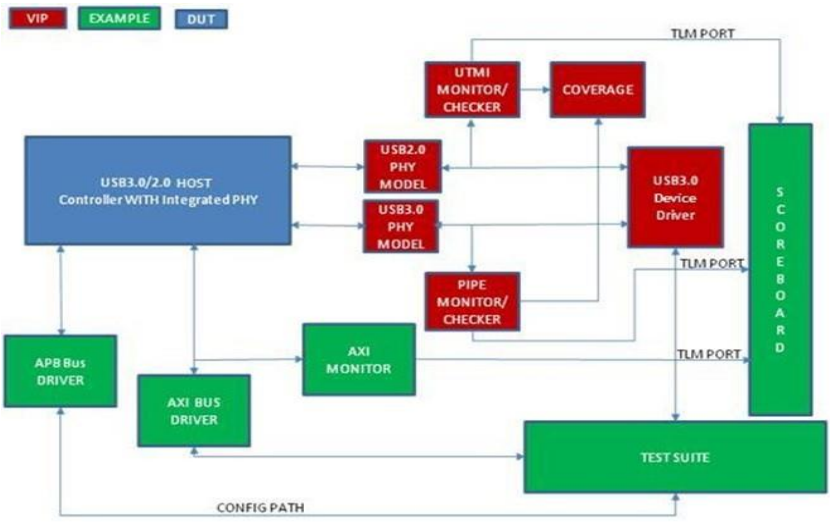
Tessolve Semiconductors offers USB 3.0 OVM/UVM Device and Host VIP as part of its asureVIP series of offerings. This is a highly flexible and configurable verification IP, which can be easily integrated into any SOC verification environment or Block level verification environment.

The USB 3.0 VIP supports both USB 3.0 and USB 2.0 functionalities and has been entirely programmed in System Verilog and provides support for OVM and UVM based testbenches.

The VIP comes with a protocol BUS Monitor which checks for non-compliance with USB 3.0/2.0 protocol violations, reported by monitors connected to PIPE and UTMI.

USB 3.0 VIP supports Bulk, Control, Isochronous and Interrupt transfers and supports SuperSpeed (SS), High Speed (HS), Full Speed (FS) and Low Speed (LS) which enables engineers to verify speed negotiation between SS, and 2.0 FS, HS, LS.

Block Diagram



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TESSOLVE
A Hero Electronix Venture

Overview

VIP: USB 3.0 DEVICE and/or HOST

Compliance: USB 3.0 Specification

Language: System Verilog

Methodology: OVM 2.1.1 / UVM 1.1

Simulators: Cadence Incisive, Mentor Questa, Aldec Riviera-PRO

Deliverables

- USB 3.0/2.0 Device and/or Host VIP
- UTMI Monitor
- PIPE Monitor
- Test Suite
- VIP User Guide

Key Benefits

- Highly Flexible, Independent and Configurable USB 3.0 VIP
- Proven against silicon proven VIP
- Less TAT in integrating into SOC verification environments

Technical Specifications

PHYSICAL LAYER

- USB 2.0 and USB 3.0 PHY Layer support

LINK LAYER

- Full LTSSM Support (PIPE Interface)
- Ordered Sets Support
- Cable Unplug & Re-plug Scenarios
- Auto Speed change detection (HS/FS/SS)
- Power management Suspend & Resume
- Support Low Power State (U1,U2,U3)

PROTOCOL LAYER

- The protocol-based test category verifies the packet fields for different types of USB packet transfers
- Transfer level tests include control read and write for two and three stage transfers, bulk IN and OUT transfers, ISO IN and OUT transfers and the Interrupt IN and OUT
- Data Bursting
- SS Bulk Stream
- LMP, LPM and ITP Generation
- Flow Control support (ACK/RETRY/NUMP/ NRDY…)

Other VIPs Available

- **ARM**: AXI, APB, AMBA ACE and CHI
- **Hi-Speed Interface**: Ethernet (10/100/1000MB & 10GB), PCIe RC and EP, USB 3.0 Host and Device, CSIX and SPI
- **Memory and Storage**: SDCARD 4.0, DDR 4/3, LPDDR 4/3 and ONFI
- **MIPI**: DPHY, DSI, LPDDR, MPHY, SMBUS, RFFE and Unipro
- **Universal Serial I/O**: CAN, GPIO, I2C, UART, SPDIF, I2S, SMBUS, SPI and TDM

Independent Verification Service

Tessolve can deliver an independent verification service that not only reduces development costs and time-to-to-market, but also improves product quality.

Proven Implementations

Use asureVIP with the confidence of knowing that they have been successfully deployed by leading SoC companies around the world.

About Tessolve

Tessolve Semiconductors Private Limited provides services and products to organizations developing complex products in the microelectronics and embedded software and systems industries.

Tessolve operates globally with offices in the UK, France, Germany, India, Singapore the USA plus a network of international partners.

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