MIPI RFFE

asureVIP

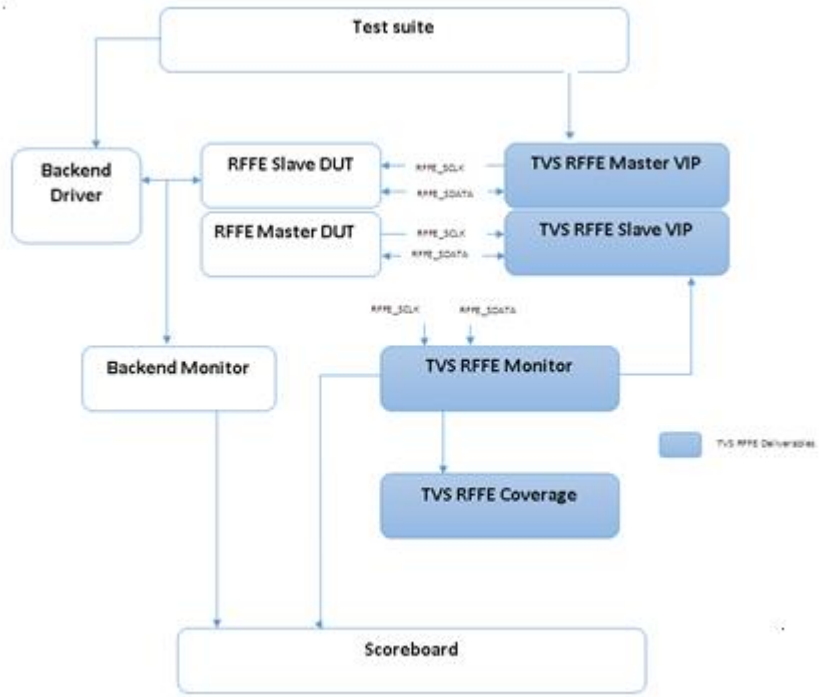
MIPI RFFE UVM VIP

Tessolve Semiconductors offers a Mobile Industry Processor Interface Radio Frequency Front End (RFFE) OVM/UVM VIP as part of its asureVIP series of offerings. This is a highly flexible and configurable verification IP, which can be easily integrated in any OVM/UVM SoC environment or Block Level Verification Environments.

The Tessolve OVM/UVM based MIPI RFFE VIP supports both Master and Slave functionalities and has been entirely programmed in System Verilog and provides support for OVM/UVM based testbenches.

The VIP comes with a protocol Bus Monitor which checks for non-compliance with RFFE specification. Monitor will collect the information from the bus and will frame the high-level abstraction classes such as command and address/data frames. During the "master passive and slave active" mode configuration, the monitor will collect the information from the bus and inform the slave on what command is initiated from the master and how many bytes are to be transferred from slave to Master.

Block Diagram



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A Hero Electronix Venture

Overview

VIP: MIPI RFFE

Compliance: MIPI RFEE 1.1 specification, support extendable for RFEE 2.0 specification

Language: System Verilog

Methodology: UVM 1.1

Simulators: Cadence Incisive, Mentor Questa, Aldec Riviera-PRO

Deliverables

- MIPI RFEE Master/Slave UVM VIP
- RFEE Monitor
- Test Suite
- VIP user guide

Key Benefits

- Highly Flexible, Independent and Configurable MIPI RFEE UVM VIP
- Proven against Silicon Proven VIP
- Less TAT in integrating into SOC Verification environments
- Excellent product support

Technical Specifications

- MIPI RFFE Master and Slave Functionality
- Configuration support Master, Slave or both
- Supports Multiple Slaves
- Supports FULL_SPEED and HALF_SPEED
- Supports following frames:
  - Command Frame
  - Address/Data Frame
  - No Response Frame
- Supported Read / Write Commands:
  - Register 0 write
  - Register Write and Read
  - Extended Register writes for single slave
  - Extended Register Read
  - Extended Register write long
  - Extended Register Read long
- Multiple slave address value configuration
- Supports Master and Slave Error Injection schemes such as:
  - Undefined command Frame
  - Command frame with parity error
  - Incompatible command length
  - Address frame with parity error
  - Data frame with parity error
  - Read using the broadcast ID

Other VIPs Available

- **ARM**: AXI, APB, AMBA ACE and CHI
- **Hi-Speed Interface**: Ethernet (10/100/1000MB & 10GB), PCIe RC and EP, USB 3.0 Host and Device, CSIX and SPI
- **Memory and Storage**: SDCARD 4.0, DDR 4/3, LPDDR 4/3 and ONFI
- **MIPI**: DPHY, DSI, LPDDR, MPHY, SMBUS, RFFE and Unipro
- **Universal Serial I/O**: CAN, GPIO, I2C, UART, SPDIF, I2S, SMBUS, SPI and TDM

Independent Verification Service

Tessolve can deliver an independent verification service that not only reduces development costs and time-to-to-market, but also improves product quality.

Proven Implementations

Use asureVIP with the confidence of knowing that they have been successfully deployed by leading SoC companies around the world.

About Tessolve

Tessolve Semiconductors Private Limited provides services and products to organizations developing complex products in the microelectronics and embedded software and systems industries.

Tessolve operates globally with offices in the UK, France, Germany, India, Singapore the USA plus a network of international partners

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