MIPI DPHY

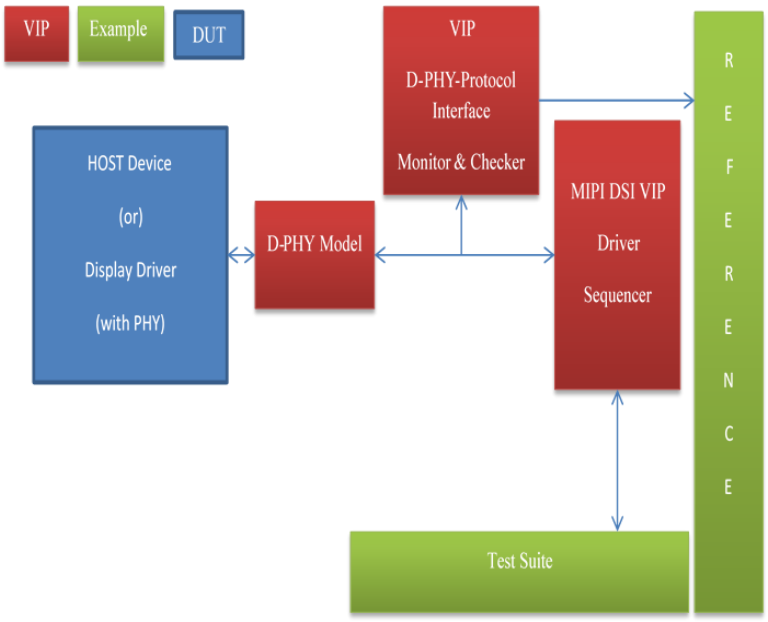
asureVIP

MIPI DPHY UVM VIP

Tessolve Semiconductors' asureVIP™ for MIPI DPHY enables constrained random metric driven verification of IP level or SOC level verification of this protocol specification. MIPI DPHY VIP offers flexibility, excellent product support, while UVM support allows reusability, fully configurable, coverage driven verification.

This UVM VIP has extensive constrained-random stimuli generation capabilities, configurable monitors and checks to ensure protocol compliance for Host as wells as Peripherals. Pre-defined coverage bins enable easier extension and coverage collection.

Block Diagram



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A Hero Electronix Venture

Overview

VIP: MIPI DPHY
Compliance: MIPI Alliance Specification for D-PHY, version 1.00.00, MIPI, Alliance, Inc., 14 May 2009
Language: System Verilog
Methodology: UVM 1.1
Simulators: Cadence Incisive, Mentor Questa

Deliverables

- MIPI DPHY UVM VIP
- Sample Testbench
- Sample Scoreboard
- Sample Virtual Sequencer
- VIP User Guide

Key Benefits

- Highly Flexible, Independent and Configurable MIPI DPHYUVM VIP
- Less TAT in integrating into SOC Verification environments
- Excellent product support

Technical Specifications

- One or more differential High-speed
- functions including differential transmitter HS-TX and differential receiver HS-RX
- One or More differential Low-Power
- functions including differential transmitter LP-TX, differential receiver LP-RX, Low-
- Power Contention-Detectors (LP-CD)
- Correlation between High-speed and Low- power functions
- Two Types of Data Lanes (Bi-directional and Unidirectional)
- Single or Multiple Data Lanes
- Supported types of Reverse communication (per Lane)
- Functionality supported by Escape mode (for each direction per Lane)
- Data transmission can be with 8-bit raw data (default) or using 8b9b encoded
- symbol
- Data shall be serialized in the transmitting PHR and de -- serialized in the receiving PHY
- Support for different Lane states and Line levels
- Support for different operating modes
- Bi-directional data lane turnaround
- Bi-directional control
- Support for detecting protocol errors and contention

Other VIPs Available

- **ARM**: AXI, APB, AMBA ACE and CHI
- **Hi-Speed Interface**: Ethernet (10/100/1000MB & 10GB), PCIe RC and EP, USB 3.0 Host and Device, CSIX and SPI
- **Memory and Storage**: SDCARD 4.0, DDR 4/3, LPDDR 4/3 and ONFI
- **MIPI**: DPHY, DSI, LPDDR, MPHY, SMBUS, RFFE and Unipro
- **Universal Serial I/O**: CAN, GPIO, I2C, UART, SPDIF, I2S, SMBUS, SPI and TDM

Independent Verification Service

Tessolve can deliver an independent verification service that not only reduces development costs and time-to-to-market, but also improves product quality.

Proven Implementations

Use asureVIP with the confidence of knowing that they have been successfully deployed by leading SoC companies around the world.

About Tessolve

Tessolve Semiconductors Private Limited provides services and products to organizations developing complex products in the microelectronics and embedded software and systems industries.

Tessolve operates globally with offices in the UK, France, Germany, India, Singapore the USA plus a network of international partners.

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