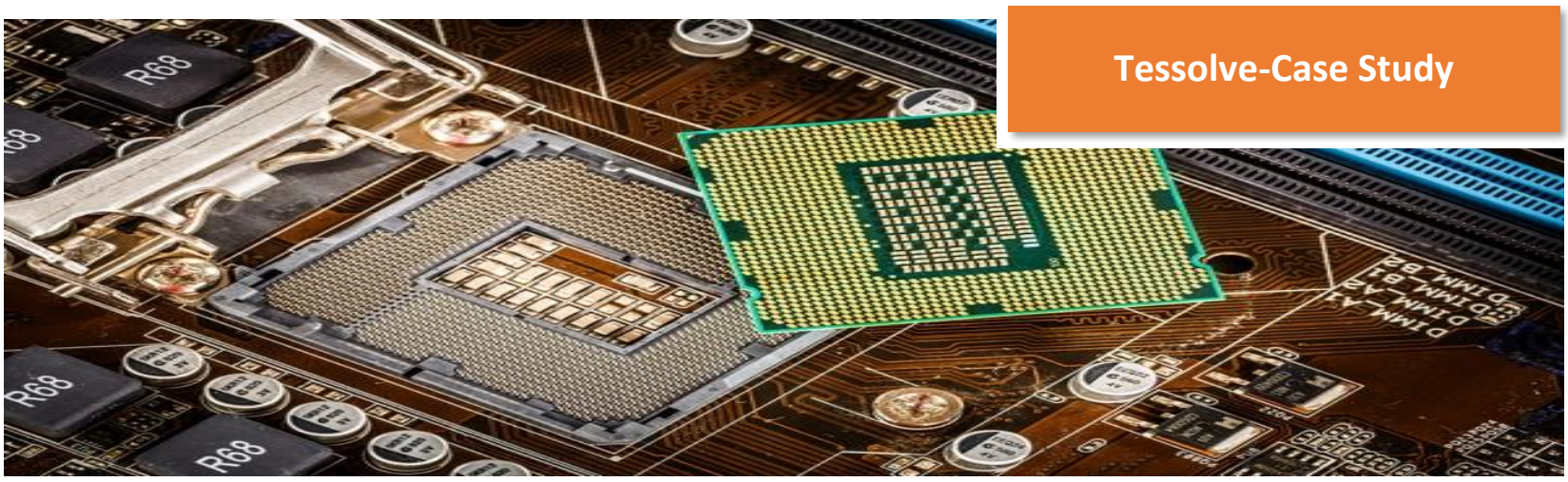
Tessolve provides DFT Solution for Network SoC



Tessolve-Case Study

Background

The customers serve across the spectrum of electronics applications with innovative semiconductor solutions by leveraging its vast array of technologies, design expertise and manufacturing strength.

When the customer urgently needed a team of engineers for DFT implementation and execution of its network SoC, they turned to the Tessolve DFT Services for help. Tessolve was chosen as the preferred vendor on the basis of its track record in executing managed services programs.

The Tessolve Solution

Tessolve initially analyzed the design and estimated the effort for DFT implementation of the SOC. As part of this program, Tessolve also had to execute DFT DRC for Scan and implement compression. The stuck-at coverage target for the SoC was an aggressive 99.8%.

Tessolve implemented a unified and modular test bench framework to cater to USB-PHY, PCIE-PHY and DDR PHY testing. The test environment was developed to test analog modules like PLLs, temperature sensors etc. The same environment could be reused to create vectors for tester also.

Tessolve used a blended model for project execution wherein the team structure provided flexibility for both offshore mentoring and onsite support. By providing DFT specialists for the duration of the project, Tessolve reduced customer overheads involved in hiring expensive fulltime DFT resources. The Tessolve DFT strategy reduced event-based vector to cycle based vector conversion effort to nil. Tessolve's competitive pricing for the framework also enabled customer to reduce overall development costs.

Benefits to Customer

- Reduced Customer Overheads.
- Event based vector to Cycle based vector conversion effort was reduced to null.
- Reduction in overall development costs