

Tessolve provides end-to-end DFT solution for Consumer SoC



Background

This project involved DFT implementation and execution of a complex Consumer SoC. Tessolve's expertise in development of DFT methodologies for complex designs and track record of providing a wide range of DFT Services from scan insertion to JTAG meant that the customer could rely on Tessolve to independently manage the DFT activities for their SoC.

Tessolve was tasked with scan implementation, verification and pattern delivery for the design which had a flop count of around 1.5 million. Memory BIST (MBIST) also had to be performed for 400+ memory instances. The stuck at and at-speed coverage analysis targets were set at 99% and 85% respectively.

The Tessolve Solution

Tessolve implemented a balanced compression ratio scan hybrid coded to generate optimum pattern count. MBIST generation and verification was performed on standalone test benches where different modes like diagnosis, hard repair, soft repair and BIST were verified before plug-in into the SoC.

The Tessolve approach enabled the customer to meet the stuck-at and at-speed coverage targets. Tessolve was also able to provide assistance to develop test mode constraints for Static Timing Analysis (STA). Tessolve automated the scan insertion and pattern generation process to provide quick turnaround for net list updates due to ECO.

Benefits to Customer

- All DFT expertise under single roof to assist STA constraints (TEST modes) till tester assistance.
- Re-usable automation scripts for scan insertion used pattern generation.
- Reduction in overall development costs.