TESSOLVE
A Hero Electronix Venture

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FIRST BIN

A Newsletter for the Semiconductor Engineering Community

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Dear Customer,

I hope you had a good year-end break and your New Year is off to a flying start!

We recently celebrated our 15th anniversary and I would like to take this opportunity to congratulate our employees for making Tessolve a company known for engineering excellence. I would also like to thank our customers and partners for your support and trust in us.

We have grown to over 2000 employees worldwide. We are in for the long run and continue to expand in all our core offerings i.e., VLSI design, Embedded Systems design, Test/Product Engineering and PCB Hardware Design and Manufacturing.

It has been a busy year for us.

In the VLSI design space we have successfully designed SOCs in 7nm and 10nm technologies. We have grown to over 700+ member team. Our acquisition of Analog Semi over 12 months ago has been fruitful. Analog Semi team has integrated well and successfully delivered turnkey projects in power management and data converter designs. We are also close to integrating another large, well reputed team in Design Verification space, which will further strengthen our Verification competency.

It has been an eventful year for our Embedded Engineering Team. We have successfully designed and deployed in high volume, a Snapdragon based Automotive GPS system for French market. We have also designed and deployed IOT based Gateway solutions, automotive pedestrian detection systems and LED lighting solutions. We have also developed several custom system designs namely Auto radar solution, Radar Signal Processing card, 6LoWPAN modules, NBIoT modules etc.

In Test and Product engineering space, we have provided several turnkey solutions for SOC, RF and Analog chipsets including those in 5G and Silicon Photonics space. Apart from Test Development solutions, we have extended our offerings to Package design, Mechanical design and complete Reliability qualification. We have successfully executed several Product Reliability and Qualification activities out of our new lab in Bangalore. We have also extended our engineering solutions to providing low volume production using our Singapore and Malaysia test labs.

On the PCB front, we have extended our offerings to not only take full turnkey ownership of Design, Fabrication and Assembly but also provide comprehensive testing prior to delivery of the fabricated boards. We are also setting up Load board diagnostics and repair services at our Singapore and Malaysia facilities to shorten the cycle time for our customers when the need arises, at the production facilities.

We are continuing to invest in growth and look forward to partnering with you to provide value add engineering solutions. I wish you all success in your endeavors in the New Year!

Let me also congratulate all the following special accomplishments in presenting papers and competition by our team members:

Jagadish Kumar Chandrasekaran, Srinivasan C, Kandhan Rajakumar, Gowri Shankar Ilankumaran, Siva Pavan Anala, Purna Chandra Sekhara Rao Neeli on their papers "Post Fabrication Fix for RF DIB Design Problems" and "RF Sensitivity test (7.5GHz) in non RF configuration using on board components", on their Tutorial " Challenges and Best Practices on ATE Load Board Design", and on their Poster presentation "Adaptive RF DIB Design for Bench & ATE" at ITC India & USA.

Aravindh Manokaran on winning the First Prize at the IPC Design competition at Elcina event, BIEC, Bangalore on 12 July 2019.

Best Regards,
Srinivas Chinamilli
Co-Founder & President

Tessolve Showcase

1. PACKAGE DIMENSIONAL TOLERANCE AND ITS ILL EFFECTS ON HVM

Author: Dominic Savio - Test Lead

Abstract-A land grid array is a packaging technology with a circular pad on the bottom side of the Package. when attempt was made to design a Socket for this package, it was evident from the initial socket drawing that the socket pogos would not make any contact with the package pads in worst case conditions. This would cause yield losses during HVM and cannot be considered as a robust Test HW design. Merely tightening the socket and/or pogo dimensions is not the solution as it would lead to device sticking into the package guide during HVM. The issue was that the device dimensional tolerance and the Pad Positional tolerance of the package was not within the acceptable boundaries and must be tuned to be considered as good design for manufacturability. This article describes on how this issue was approached and addressed at a very early stage of the Test HW design and providing adequate feedbacks to Package Design Team and to the Socket Vendor to have a most reliable HVM Test Solution.

I. Introduction

LGA packaging is a technology with a circular grid of contacts on the bottom side of a package. The electrical contact to the Device Pads is made by pogos located on LGA socket during HVM testing, and by using solder paste or socket during actual applications.

The initial Package was manufactured with the following Dimensions.

- Package Dimension: 7X7.5 ± 0.1mm
- Pad Diameter: 0.270±0.025mm
- Metal Diameter: 0.330±0.025mm
- Min Pich:0.615mm
- Pad Positional shift 0.1mm

An attempt was made to design a customized socket for this package which yielded the following Socket parameters

- Package Guide of 7.15 X 7.65 mm (including a manufacturing tolerance of +0.05mm)
- Kelvin Pin Diameter of 0.315mm
- Non-kelvin Pin Diameter of 0.290mm

These numbers looked disturbing at the first sight. It was found that the combination of largest Socket Package Guide of 7.65mm X 7.15mm against the smallest Package Dimension of 7.4mmX6.9mm in combination with smallest Pad diameter of 0.245mm, and a positional shift 0.1mm, the Pad simply would not make any contact with the Socket Pogos. But a complete analysis, with proven methodologies were required to convince different teams for a design change. The failure mode analysis was required to describes how this item could fail to perform its defined function and pose a risk during HVM.

II. Abbreviations and Acronyms

HVM- High Volume Manufacturing, LGA- Land Grid Array. BGA-Ball Grid Array, RSS-Root Sum Square, CAD-Computer Aided Design

III. Analysis

The contact simulation was done to illustrate the failure mode with the help of proven CAD tools by keying in the Significant Dimensions of the socket and package. `

The Socket was designed to accommodate this Package, by considering the dimensional tolerances of the socket and the Pad dimensions, it was evident that a combination of largest Socket Package Guide of 7.65mm X 7.15mm against the smallest Package Dimension of 7.4mmX6.9mm would create a play of 0.125mm as shown in Fig.1. This Play along with smallest Pad diameter of 0.245mm, and a positional shift 0.1mm would create an offset between the pogo and pad. Figure 2. shows this offset. Further CAD simulations on the Pad versus Pogo level proved that there is no contact between the socket pogo and the Package Pad under worst case conditions.

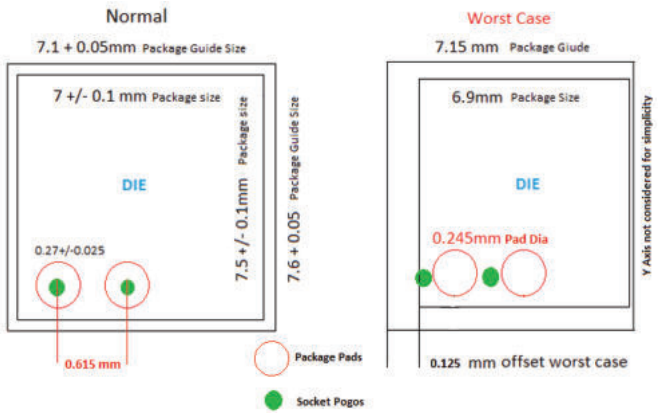


Fig.1. Play between Socket Package Guide and Package.

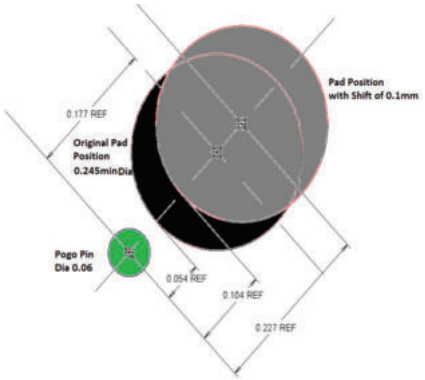


Fig 2. Contact Simulations between the Device Pad and Pogos.

IV. Suggested Improvements

Contact simulation was done on different possible permutations and combinations of the Package Dimensions and socket Dimensions and the numbers which would mitigate this risk was recommended to the packaging team.

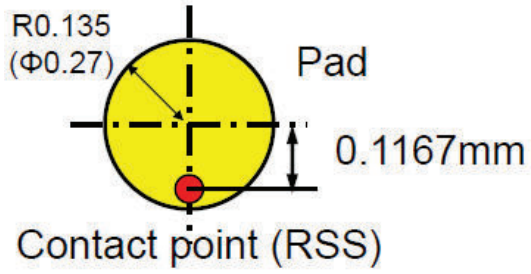


Fig. 3. Contact Simulations for Recommended Package Tolerance

The Packaging team agreed to revise the dimesions to the following

- Dimension Tolerances to 0.05mm from 0.1mm
- Pad Diameter to 0.280±0.2mm from 0.270±0.25mm
- Pad Shift Tolerance to 0.140mm from 0.100mm.

The revised pad shift tolerance is on the higher side when compared to the previous dimension of 0.1mm. With these revised dimensions the contact simulations and the RSS Analysis were done and found that the complications never eased while considering the worst-case Package dimensions & worst Socket package Guide Dimensions. But the packaging team never agreed to tighten the pad shift tolerance because of practical limitations and paraphs the cost.

This forced us to look into the actual production spread of the Pad shift of similar products from the same manufacturer which was never more than 0.005mm versus the on-paper value of 0.140mm. This gave a sigh of relief to the package design team and was confidence that the pad shift tolerance wouldn't create any issues with the contact. But still as it's not a scientific solution as there is a chance that the Process shifts further to the on-paper value of 140mm which is still within the manufacturing limits. Therefore we pressed on with revising the package dimensions.

V. Recommendations and results

Results from more CAD simulations were used as recommendations to the Packaging team and the Socket Vendor to Enhance manufacturability and improve yield. As sockets have their manufacturing limitations and tolerances and are designed to fit-in the Package there was little or no room for improvement on the socket side.

VII. Results and Conclusions

Proposals highlighting the Risks of manufacturability were given to the Packaging team along with further contact simulations and RSS Analysis. The packaging team analyzed the data and agreed to the risk and the package was changed to BGA with a bigger ball diameter than the existing LGA.

Since the package type was changed, now we had room on the socket side to choose a crown tip with a larger diameter rather than the already selected Pointed tip for LGA which would give us more contact area. The contact analysis was done for a combination of the new package dimensions with the crown tips and simulations showed contact at worst case improved a would make contact as the simulations revealed.

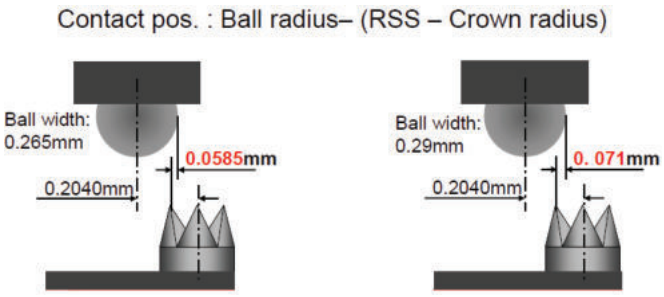


Fig. 3. Contact Simulations for revised

It would have been better to have increased diameter with a lesser Position shift tolerance which is possible, but due to increased cost of manufacturability for a tighter tolerance package a decision was made to go ahead with this revised package, which is a tradeoff between the increased manufacturing cost and slightly poor contact.

For a New Product introduction, it is the ultimate responsibility of the Test engineering Team to provide not only a stable Test Program and Workable HW, but also to investigate every bits and pieces of the Test Package, foresee any hidden risk and take actions to mitigate the same. This approach would pave way to have a robust test Package, which will serve its purpose for the full life cycle of the Product, without any major upgrades or modification to test Hardware.

2. SHMOO ANALYSIS TOOL (SAT) - AUTOMATION TOOL

Authors: Amba Kumari - Test Lead and Gopinath Raju - Technical Lead

With the increasing test pattern count and shrinking project time-lines, we need to automate process for easy/efficient execution of projects. This tool has been developed targeting same.

SAT tool supports conversion and analysis of shmoo data (for SMT8) collected using TCCT tool. Shmoo data available in the DLOG file is analyzed and converted to PNG with the files being segregated in different folders accordingly to the shmoo category decided by the tool.

1. ALL_PASS: Shmoo response passing across all voltage/frequency condition.
2. GROSS_FAIL: Shmoo response failing across all voltage/frequency \ conditions.
3. FAIL_SHMOO: Shmoo response failing at the required voltage/ frequency.
4. SHMOO_HOLES: Shmoo response with cluster of FAIL surrounded by PASS.
5. CEILING_SHMOO (Both high and low frequency): Any shmoo which is passing @ required voltage/frequency and series of lower frequency fails from shmoo start frequency point across voltage conditions or series of higher frequency fails till shmoo end frequency point acros voltage conditions.
6. WALL_SHMOO (Both LV and HV Wall): Shmoo response which passes @ required voltage/frequency, failures observed across frequency for a series of voltage step (either towards the lower or higher voltage side).
7. LINEAR_SHMOO: Shmoo response which passes @ required voltage/frequency, and has a failing linear pattern with enough margins above the required voltage/frequency.
8. MARGINAL_SHMOO: Linear shmoo response which is passing @ required voltage/frequency but does not have enough margins above the required voltage/frequency.
9. OTHERS: Shmoo response which is passing @ the required voltage/frequency and which either have more than one category mentioned above or does not meet any of the listed classifications.

The script generates below reports:

1. Summary report in below format.

Pattern_Name	Dev#_Split_SiteID		
	Temp1	Temp2	Temp3
Pattern1	Linear	Linear	Gross_Fail
Pattern2	Linear	Shmoo_Holes	All_Pass

2. Detailed report in below format.

SiteID	Dev	Temp	Split	Pattern_Name	All Pass	Gross Fail	Shmoo Holes	Celling Shmoo	Wall Shmoo	Marginal Shmoo	Others	Linear Shmoo
2	F1	25	FFF	Pattern1	No	No	Yes	Yes	No	No	Yes	No
2	F1	25	FFF	Pattern1	No	No	No	No	No	No	Yes	Yes

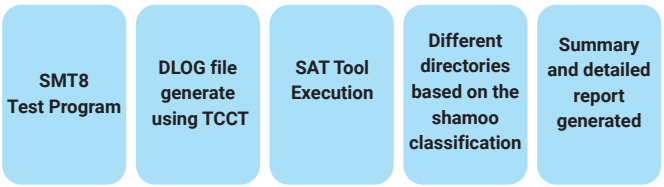
Site ID: device placed on which site while data collection (site1, site2, etc.)

Dev#: device number inputted while collecting data.

Temp1, Temp2, Temp3: Temperatures @ which data was collected \ (-40C, 25C, 110C).

Split: Type of the device (TT/FF/SS).

Process Flow:



Execution Time:

DLOG file containing 1000 shmoo response was analyzed and it was observed 90% of analysis time savings.

Manual Analysis	SAT
~3hours	~20min

3. COST EFFECTIVE VALIDATION FOR EARLY TEST-TO-DESIGN FEEDBACK

Author: Abhilash Jattimane - Sr. Test Engineer

Abstract:

As there is always a competitive scenario in the Semicon industry to release products with similar features, there is also a trend in the design community to reuse IP's from existing designs to gain faster time to market.

Though the Design is taped out/released to Fabrication with limited design simulation; it does put a special onus on the Validation team to evaluate the Design w.r.t it's Specification across PVT and also meet the Target Yield & Test Cost per Unit

As always, if conventional approach is used for Silicon validation with extensive ATE/bench testing at multiple temperatures and Lots, it can potentially overkill the schedule and Time-to-Market.

The technique described in this article is one of a case-study which demonstrates how ATE validation criteria with VT Guardbanding (GB) was best utilized by this tool development for early detection of yield issues thereby assisting the Design community with further corrective actions in Design (if any).

Approach:

Guardbanding is a methodology devised to minimize test insertions across desired production temperatures.

Taking into account the test cost and test time involved in estimating the yield or understanding product behavior through multiple temperature insertions across multiple wafers, guardbanding helps in reducing test insertions thereby reducing test cost.

Once guardbands are derived from sample characterization data, yield estimation is possible by exercising GB's on room temperature testing alone. With this approach it is possible to have economical and swift estimation of the yield, facilitating test engineers in conveying appropriate feedback to chip designers wherever design improvements are to be planned in subsequent revision of silicon.

Interval estimates are used rather than point estimates to calculate the temperature offsets from characterization data as will be demonstrated further. Temperature offsets are then used to calculate Room Temperature Guardbanded limits from the existing data sheet specifications guaranteed across voltages and temperatures.

Step 1: Characterization and analysis across 3 temperatures (-40°C, 25°C, and 115°C) on sample quantity (say 50 devices).

Step 2: Calculating individual drift per device at hot and cold temperatures relative to room temperature across all devices.

Step 3: Calculate average drift across 50 devices. Mean of drifts from cold to room temperature and mean of drifts from hot to room temperature across all 50 devices is calculated.

Step 4: Standard deviation calculated from individual delta's relative to room temperature across 50 devices.

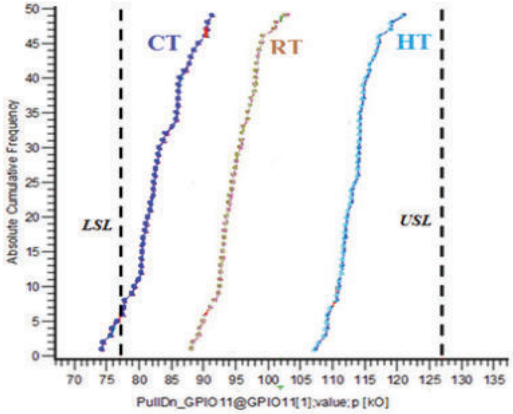
Step 5: Temperature Drifts (DCR, DHR) are calculated with 80% confidence interval (Z = 0.84) with n devices (50)

Step 6: DEL and DEH are calculated as shown below,

Step 7: From the Data sheet limits (LSL, USL) and drift parameters (DEL, DEH) calculated from char data, Guard bands are derived as per below equation.

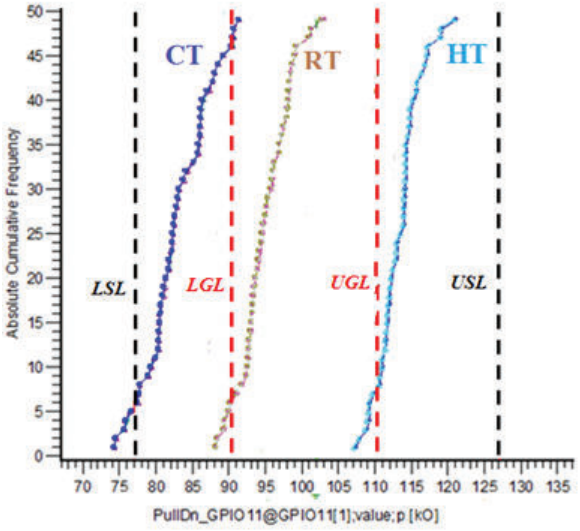
LGL= LSL + DEL.

UGL= USL - DEH.



- There are about 5 devices at cold temperature (CT) having measurements below LSL.
- These out-of-spec devices are only caught during 2nd temperature insertion at cold temperature after room temperature testing.
- Also, good devices from these two temperature insertions are to be tested at hot temperature (3rd temperature insertion) before considering the device as Bin1device.

With guardbanded test limits, highlighted by red dotted lines (LGL, UGL) as in below CDF, it is possible to reduce test insertions by deriving the test limits such that the probable failures at hot temperature and/or cold temperature can be identified by just testing at room temperature.



In Summary,

- Instead of testing devices at multiple test insertions with broad data sheet limits, it is beneficial to use Guardbanded test limits for testing the devices only at one temperature thereby minimizing test insertions and test cost.

Advantages of Guardbanding

- For guaranteeing the data sheet requirements of a product and to understand the product behavior followed by release to market, any new design has to undergo hot, room and cold temperature testing. As indicated in table below, it would take ~ 45 days for ATE testing on 1 Lot across 3 temperatures. With guardbanding approach with single temperature insertion we would ***save ~ 30 days.***

	Test time	
	Sec	Days
Effective Test time per device	30	0.000347222
Test time per wafer (1800 die/wafer)	54000	0.625
Test time per LOT (25 Wafers /LOT)	1350000	15.625
Test time for 3 test insertions.	4050000	46.875
Test time saved in days with Guardbanding approach		31.25

Limitations of Guardband

- Test parameters assumed to follow Gaussian distribution across PVT. Hence design improvements cannot be factored for non-Gaussian parameters if any.
- Though GB's helps in reducing test insertions, it cannot be 100% guaranteed that all the outliers at cold/hot temp will be binned out by testing at Room temp. There is always a trade-off between test time and binning of marginal failures.
- Guardbanding is only effective for parametric measurements and will not be applicable for functional test cases.
- Prior to Guardbanding, process sensitive parameters have to be cherry picked/handheld.

Conclusion

- As it is evident that most chip designers re-use IP's from previous IC designs and are more dependent on post-silicon validation results due to limited simulation data, the Guardbanding technique along with Preliminary Production data (again Guardbanded) can be used to swiftly identify the yield issues related design bugs or specification drifts and thereby the whole ecosystem from Design-Fabrication-Test quality and Time to Market is improved for achieving near to Zero DPPM.

4. OP AMP TEST HARDWARE DESIGN FOR COST AND PERFORMANCE

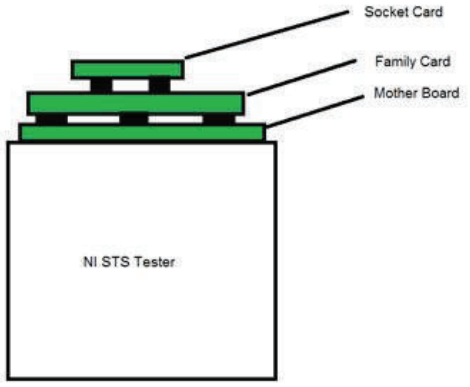
Authors : Pavithra Joshi - Test Engineer, Shashank B Radhakrishnan - Test Lead

Abstract

This Article describes the method for developing low cost test hardware for multiple Op amps and Comparators using Single Family Card / multiple Socket Card approach

1. Introduction (Requirements)

Op amps and Comparators need accurate testing to qualify them for use in satellites and other vehicles, the present solution is for a client who needed to test Op Amps, Comparators, regulators and ADC/DACs to design an ATE board with each DUT having various packages, developing individual hardware for testing each DUT is a costly affair. To optimize this an innovative approach was to design a family card to house the test circuitry for multiple designs and then interface that with a socket card housing the different packages. This would reduce the cost significantly of design, fab and components as there would be no duplication of circuitry across the family of devices.



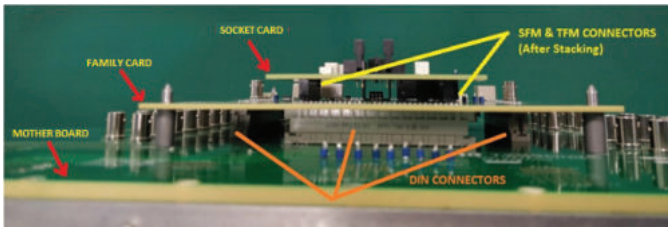
It was observed that along with cost reduction there were multiple advantages in going for Family Card-Socket card approach like risk limitation since major circuitry is only on one board. Reduction in design time as small socket boards can be done in parallel once pin outs are finalized for Socket Card mating (on the Family Card). For High Frequency testing like Slew Rate and Gain Bandwidth tests, the Input to the DUTs can be provided directly on the socket card avoiding stubs caused due to DC test support circuitry and thereby improving the performance.

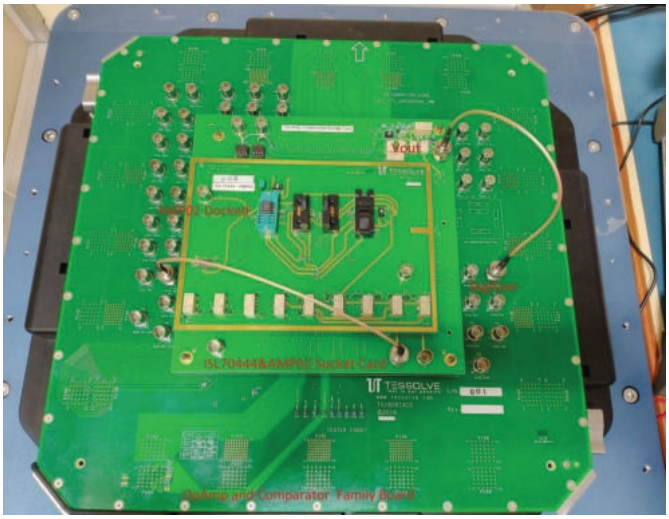
DUT list below to give picture on test requirements

Family	Package style needed	Channels	Slew Rate	GBW	Input Bias Current	Input Voltage Offset
Op Amp1	DIP 14,FP 14	4	0.15 V/µs	500kHz	750pA	80uV
Op-Amp2	FP-14,DIP-8,LCC-20	2	2.4 V/µs	5MHz	15nA	50µV
Op Amp3	CFP 14	4	60V/µs	10 MHz	650 nA	400µV
Op-Amp4	CFP-10	2	85V/µs	160 MHz	4.7uA	0.2mV
Op Amp5	DIP 14, FP 14	4	4 V/µs	4.25MHz	80nA	250µV
Op-Amp6	DIP-8, SOIC-16	1	6 V/µs	-	4nA	40µV
Op Amp7	CFP 10	1	4100 V/µs	200MHz	2.7µA	200µV

Part No	Package type	Channels	Input Voltage Offset	Input Current Offset	Response Time	Output Leakage
Comparator 1	DIP-14, FP-14, LCC-20	4	±2.0 mV / ±5.0 mV	±25 nA	1.3us	0.5 uA
Comparator 2	DIP-8, FP-10	1	7 mV (Max.)	±4 uA	7ns	-
Comparator 3	CAN-8, FP-10, DIP-8	1	±3 mV	±10 nA	165ns	-1 nA to 10 nA

Actual photo of implementation of 3 layer stackup





Three Layer Stackup Top view

1. Servo loop selection

To test the DC parameters of the Op amps and Comparators we need to implement a servo loop, below options were looked into and the optimal solution was finalized

1.a Simple Op amp Measurement servo loop by James Bryant

Simulations were done using TINA basic version as per circuits suggested in the paper, observed close to typical results as per the data sheet for DUT. But during practical implementation the oscillations were un-controllable and the results were inconsistent

1.b Intersil Recommendation for Opamp servo loop

This approach was implemented in TINA and observed close to typical results as per data sheet for DUT, during practical implementation faced oscillations related to compensation capacitors and were fixed using trial and error. The circuit was realized for Opamp-1, Opamp-5 and Opamp-7 op amps to cater for 3 ranges in Input bias current and offset voltages. Hence Intersil method was finalized for Servo loop in case of Op amps

2. Analog Devices Recommendation for Comparator servo loop

The approach mentioned for Op Amp was not stable for the comparator, so the single Op Amp servo loop (Positive feedback approach) was tried based on the recommendation from Analog Devices document.

The recommended circuits were simulated on TINA with the same servo loop components chosen for Op Amp testing and observed close to typical results as per data sheet for DUT.

The Family Card was decided to have both Positive and Negative Feedback circuits as fail safe.

3. Bench Validation

- The simulated circuits were validated on bench before starting with the PCB design to make sure all the criticalities were taken care.
- The components for the servo loop were finalized after multiple bench validation and the same has been taken to the PCB design. The bench results were almost matching with the simulation data. The placement of servo loop components was also decided from the bench validation
- It was observed that the compensation capacitors and resistors need to be varied for different device family and hence a bank of pads was provided for these components in the PCB design and controlled using relays.

4. Challenges and issues faced

- CMRR Marginality faced for few devices, which was solved by using very low tolerance resistors
- Slew rate reduction was observed due to Cabling from Pogo to tester hardware, DUT output swing was adjusted accordingly along with along with hardware changes to achiev e the targeted 1700V/uS.
- 10nS Response time measurement was difficult to achieve, this was achieved by using high speed comparator logic with ps response time.

5. Conclusion

- With the three layer approach the following advantages are seen
- Cost reduction by 40% compared to multiple mother board designs.
- Limited Risk since only 1 board (Family Card) has major components and circuits.
- Reduction in Turnaround time since only small Socket boards are needed along with Family card and Mother Board.

6. Reference

- https://www.analog.com/en/analog-dialogue/articles/simple-op-amp-measurements.html
- https://www.renesas.com/tw/zh/www/doc/application-note/an551.pdf

5. HIGH VOLTAGE (1.2KV) PCB DESIGN

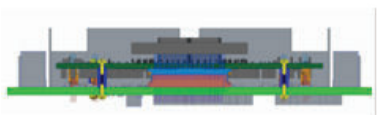
Author : Selva raj Sr. PCB Design Engineer

Scope of this project

This paper elaborates Guidelines and Considerations followed for designing a PCB carrying High Voltage (1.2KV) signals. The design is for a Universal Mother board on ETS 364 platform designed in Mentor Graphics PADS EDA tool. Unlike a normal PCB design, High Voltage designs have lot of constraints like Conductor Spacing, Dielectric Material selection, Guarding etc. This paper discusses all those constraints in detail and how they are dealt in this High Voltage ATE Board. Finally Leakage was tested at a High voltage of 600V. It was less than 20nA at open socket condition and the leakage value measured with the DUT in place was close to the design spec

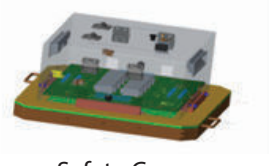
Board Setup

The DUT is placed on a Daughter card that sits on top of this Universal Mother board. The entire setup, Mother board + Daughter card, is covered with a Safety cover to isolate user from High Voltage exposure during Hand test. The Safety cover is designed by Tessolve Mechanical Engineering team.



Mother Board

Daughter Card



Safety Cover

Board details

This board was designed with ETS 364 platform and 34 layers stack up with 9 signal layers (0.5 oz cu) and 13 power layers (1 and 2 oz cu). High voltage power layers used 2 oz (For Force high) and 0.5oz (Sense high) copper with thicker core. Board thickness was 4.74980 +/- 0.254mm and size was SQ 416.56 mm.

Steps taken to control the Current leakage during high voltage testing:

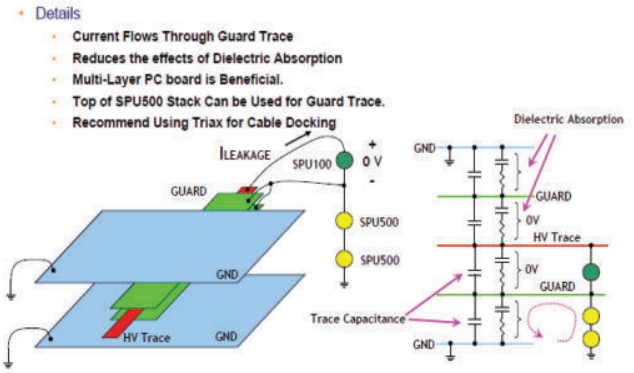
a. Conductor Spacing

Trace width and spacing is followed as per the IPC 2221 standard for High Voltage Design and Clearance. Also, care is taken to select tester channels for High Voltage signals in order to meet all high voltage design criteria and resources in tester.

b. Layer stackup

High Voltage traces were routed using Guard trace method between the High Voltage Signal and the Ground to reduce the Dielectric Absorption. With this as a reference and considering the Force Low, Sense High and Low traces, we came up with a Layer stackup as below for this design. Comparative tracking index (CTI) was taken into consideration to withstand such a high voltage.

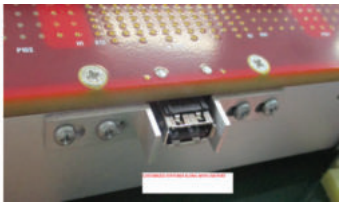
The layer above the High voltage signal (Force high) is HV guard for which potential is same as Sense high. The layer below High voltage signal has Sense high and HV guard



c. Nature of challenges during high voltage protection and mechanical rigidity setup

a) USB setup for high voltage protection:

This board was designed to use in three different environmental such as production test, characterization test and Hand test environmental. So We designed an interlock feature mechanism which can communicate to high voltage instrument to adopt for different 3 environmental. Polycorbide Safety cover was designed along with USB connector in order to make a communication for high voltage setup during Hand test. One more USB foot print was created and placed in tester side at pogo region. This USB pad had a hard gold plating for half area and remaining half area was used for soft gold plating and customized stiffener was used for both production and characterization test. During production test, we will use one stiffener along with interlock feature mechanism which will sit on the hard gold plating on the USB pad contact and enable the high voltage instrument through USB cable (Refer below picture). During characterization test, we will use another customized stiffener and USB connector will be soldered manually on the soft gold plating area of USB pad contact which can be used to enable the interlock mechanism through USB cable.



b) FEA thumb rule

Handler will pick the device to be tested from tray and will be put in Socket and hold it for few minutes. So, handler also will apply some plunge force on the entire mechanism (super imposed). So mechanical rigidity was confirmed to withstand over all plunge force applied by handler based on the data available and Finite Element Analysis (FEA) thumb rule.

6.DESIGN CHALLENGES FOR A QUAD SITE I-FLEX TO 16 SITES ETS800 PROBE CONVERSION

Authors: Venu Gorantla-Sr. Test Lead and Somashekar - Sr. Manager

Abstract

This System ASIC is a basic chip for airbag applications. It is a Mixed signal Automotive chip being converted from a 4-site IFLEX to a ETS800 16 site solution. The die has 164 unique signals with 256 probes including all the senses. Some signals have multiple probes per the maximum current requirements. Challenge was to design a customized universal PIB for two families of devices to reduce the cycle time & cost. Designed the card for the maximum test coverage variant and the unused pins on the other variants were left floating on the probe head.

Challenges :

Resource allocation

Needed to share tester resources within site to the maximum possible extent due to high number of signals per site (256 pins) and due to the high site count of 16. Almost 90% of signals having shared resources within the site and made sure that no resources were shared across sites to have parallel test efficiency among sites. This resulted in greater density of on-board components that had to fit on the probe card PCB.

1xRelay count	Probe Card+PIB	392
	Probe Card	300
	PIB	92

16xRelay count	Probe Card+PIB	6272
	Probe Card	4800
	PIB	1472

Probe head design Solution

• Interchangeable Probe head design solution was implemented for each variant of the common probe card and PIB. PCB pad landing is given input to the probe head design of the sub variants of the device eliminating to re-design Probe card PCB for each variant.

• Effective kelvin method was taken care of with special sense-routing techniques.

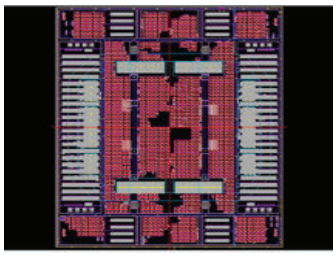
• Per pin current carrying capabilities based on probe head vendor ratings were reviewed and decided on multiple probe pins per pad. For high current signals, shapes were designed for the probe head PCB.

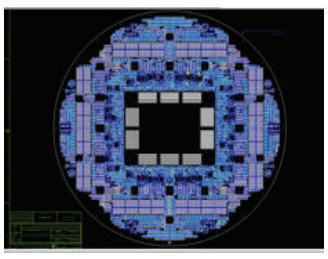
• ETS800 sector-grounds were maintained for the ground sensing in probe head close to the DUT pad.

• Trace widths or planes were custom designed in Probe head PCB based on the device design requirements.

Probe Card and PIB Design Solution

Snapshot of the PIB and Probe card placement:





• Calculating the available real estate on the PCB board with approximate keep out area is very crucial to study the feasibility of required components.

• Component selection: SSR relay selection based on the need and requirements were done with smallest footprints available in the market.

• Placement of components on both tester side as well as wafer side of the board were reviewed and selected for low current paths to make sure that the relay operating temperature range did not exceed the required current conduction.

• Relay control bits handled by the tester with available 64 bits and extended 128 bits per sector. Combined multiple (up to 24) relays with same control bits and used special logic to operate in the NC/NO conditions with same control bit.

• Customized universal PIB across two family of devices

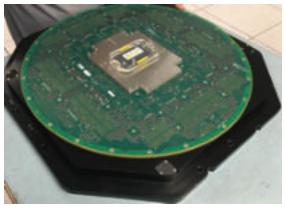
• Tester via / mating connector pogos were covered 100%, maintained trace widths, trace length resolution and verified the same.

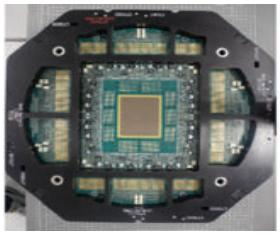
• Identical routing maintained across sites.

• Generic PIB with custom connections across devices were incorporated in the design to place as close to the tester pogo as possible.

• Final layer count = 56 layers!!!

Actual pictures of the Probe card top and bottom sides:





Conclusion

Through innovative design ideas and a disciplined approach, created a 56-layer customized universal PIB and a common probe card that provided enormous cost savings to the customer and also provided the capability that future designs can reuse the PIB. Only Probe cards need to be designed thus reducing lead time, effort & cost.

Extensive reviews during the hardware design for each sector on ETS800 helped for smooth bring up @ the wafer probe without any hardware-specific issues.

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A Hero Electronix Venture

Thank You !

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