TESSOLVE
Delivering Excellence in Semiconductor Engineering

A HERO ELECTRONIX VENTURE

FIRST BIN

A newsletter for the semiconductor engineering community

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Contents

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Tessolve Semiconductor Pvt. Ltd.
Plot # 31, Electronic City,
Phase 2, Bangalore 560 100,
Karnataka, India.
Tel: +91 80 4181 2626
www.tessolve.com
Your kind enquiries / feedback solicited at,
sales@tessolve.com / news@tessolve.com

FROM THE PRESIDENT'S DESK

Srinivas Chinamilli

Dear Customer,

I hope the New Year is going good so far for you!

Thanks for your support. We are well on our way to concluding our fiscal year with record revenues and achieving 30% growth this year.

To further strengthen our Analog design offerings, we acquired Analog Semi, a company specializing Analog circuit design and layout. Analog Semi is a team of 50+ engineers led by a very capable management team who are veterans in the industry. We are happy to have them as part of Tessolve family!

We are seeing good traction in our ESD/Latchup and Burnin reliability services. Being the only independent Reliability lab in India, we are happy to enable semiconductor companies to extend the productization capabilities beyond electrical test and characterization to product reliability qualification.

In our continuing efforts to participate in developing cutting edge technologies, we signed a partnership agreement with Institute of Microelectronics, Singapore. Our initial collaboration will involve developing improved test methodologies for advanced packages such as 3D IC packages.

I am happy to announce that we have been added as the National Instruments Gold Alliance partner. This is a good recognition of our outstanding solutions in LabVIEW, TestStand PXI and STS tester based initiatives. This further boosts our capability to offer fully integrated and turnkey PXI based solutions seamlessly.

We have also invested in Advantest Smartscale Mixed Signal tester which further boosts our capabilities for SOC testing.

We have started Tessolve China office in Shanghai. This will enable us to provide better support to companies with operations in China.

Let me take this opportunity to congratulate our employees who have received recognitions and accolades.

Firstly, let me congratulate Raja Manickam, our Founder and CEO for receiving the IESA Sarabhai Award for outstanding contributions by an individual to Indian Semiconductor Industry. A well-deserved award for furthering the semiconductor ecosystem in India!

Let me also congratulate Gowri Shankar, C Srinivasan, Siva Pavan, Jagadishkumar Chandrasekaran on their papers "Adaptive RF-DIB for ATE and Bench Reducing NRE-cost and Cycle Time" and "Novel DIB Layout Solution to Minimize Load Capacitance in pico-Amps Measurement", and N Vijay on his paper "Choosing the right PCB Stackup technology for your Teradyne Ultraflex Test Boards", which were selected at TUG (Teradyne Users Group) conference.

We look forward to continuing to provide value add engineering solutions to you and further enhancing our partnership with you.

Best Regards,
Srinivas Chinamilli
Co-Founder & President

TESSOLVE SHOWCASE

1. Improving the product quality using robust outlier screening technique

Arun Goud Poshala - Sr. Test Engineer

Introduction

To deliver zero defect product quality there are numerous tests to screen out the defective failure parts in both wafer and package level testing. In this article, we discuss on one such screening technique which intended to improve the product quality.

The Effective Outlier screening technique uses the parametric test results such as IDDQ (quiescent currents), CPR (Ring Oscillator recommendation) etc.

Description

On a conventional Leakage measurement tests or any parametric test, the test pass/fail result is judged by the defined limits say Lower spec limit(LSL) and upper spec limit(USL). In this technique, we use the calculated ratio on given parametric test results. For e.g. active leakage measured by off leakage measured. On known good part, this ratio is uniformly distributed. On few specific outlier devices, the ratio might not remain same. The device might have higher off leakage currents and lower active currents or same on and off leakage currents. Such devices considered to be failures/Outlier. These devices are not caught on conventional standard leakage tests because these devices are well within the limits. With the outlier screening technique, we could potentially catch these failures during the production screening eventually improve the product quality.

Device	Test	LSL (mA)	USL (mA)	Measure (mA)	Remarks
1	Active VDD CX	1	20	16.5	
	OFF_VDD_CX	1	10	5.5	
2	Active VDD CX	1	20	8.5	Outlier
	OFF_VDD_CX	1	10	8.5	
3	Active VDD CX	1	20	6.5	Outlier
	OFF_VDD_CX	1	10	9.5	

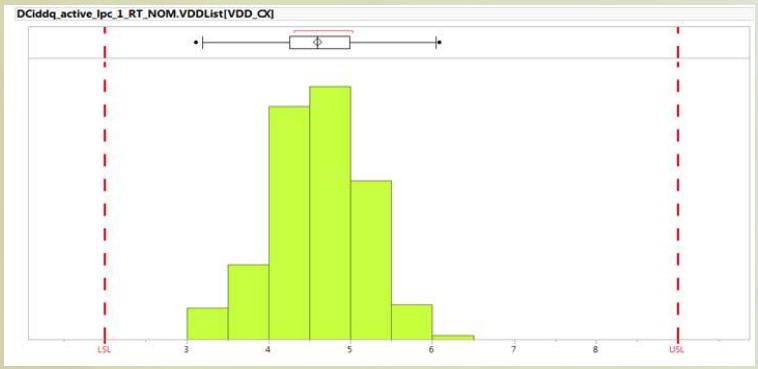


Figure 1 : Standard Leakage test with defined spec limits

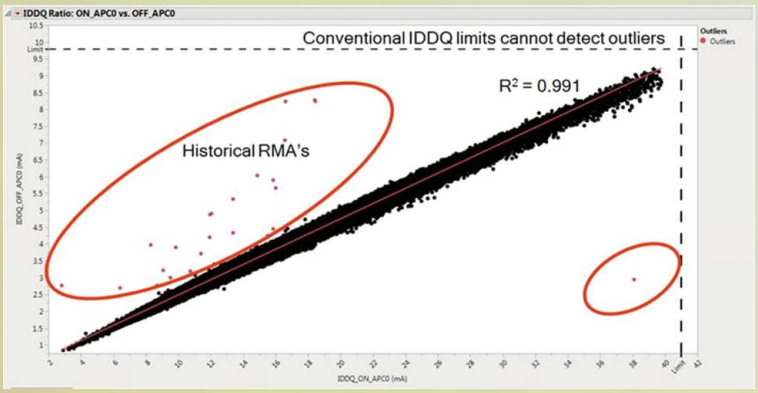
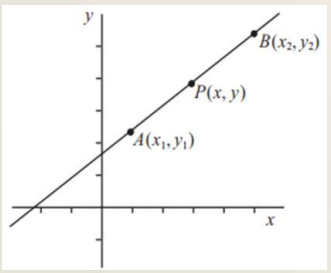


Figure 2 : Convention method of detecting outlying IDDQ Limits

Mathematics involved in outlier screening technique

On a given volume parametric test data derive the ratio of the tests of interest. Now the equation of a straight line is derived through two given points. When we do know two points on the line, and so we can use them to work out the gradient. We just use the formula m = (y2 – y1)/(x2 – x1) and drive the equation of the straight line i.e. y=mx+c.



Draw the straight-line equations on both lower and upper corners- Please refer Figure 3. Each device's parametric test result is checked if it lies within this limits or no. If the results failed it is considered as outlier.

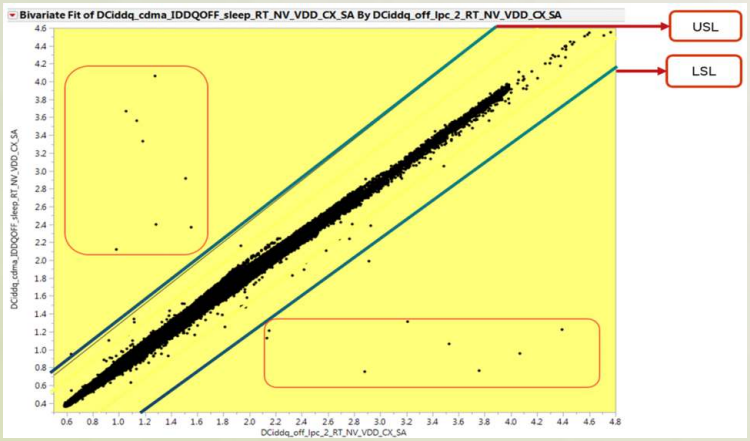


Figure 3 : Parametric test outlier screening technique

Advantages

- This screening technique proved to catch the customer returns.
- Cost effective test screening technique, this test doesn't any DFT test pattern.

2. Server Product – Test Binning Techniques

P.R. Sudhakar - Staff Engineer and R. Rajmohan - Sr. Test Engineer 2

Cloud computing is growing at a torrid pace. Cloud computing is expected to account for more than 50% of the datacenter server revenue by 2020. This growth is driving profound shifts in datacenter infrastructure. Data center operators like Google, Microsoft and Facebook have been seeking a competitive alternative that would give them servers with optimized performance for new class of cloud datacenter infrastructure while driving prices lower and boosting innovation. With the increasing demand in processing, the number of processor-cores in server chips keeps increasing with high memory.

With Multi cores CPU and more memory inside Server products, devices failing for few/single core or few MB of memory need not be branded as a completely bad device. These chips can still be salvaged and down-binned as a good part with a slightly limited feature-set. A test-time question comes up here – if a core or a memory bank fail, further down the program there might be tests which exercise these failing cores/memories again - why should we test this failed hardware as the test program proceeds? Can this be avoided? The amount of test-time involved in testing thisunit (which has a bad core or failed memory) for subsequent tests needs to be reduced, thereby overall testtime (hence the test cost) of the server chip can be reduced. A test challenge arises here to record and pass the information of failing cores/memories to subsequent tests, so that these failed cores/memories (reported by the earlier tests) can be weeded out dynamically in the test program – test-time can be saved on the fly.

Partial Good (PG) technique is a solution to the above problem statement. This works by reading pass/fail data for cores under test, Use data from Partial Good Test Array to disable failing cores (from the information of previous tests) -> execute the current test -> Update the Partial Good Test Array with the results based on the current test ->datalog the test results per core -> down-bin based on the number of passing cores and memory.

Since the amount of vector memory is more and for containing the FT (Final Test) yield loss at WS (Wafer Sort), different insertions are used. Test-time can be saved a lot if Information of failing/passing cores is passed to the next level of insertion (ex. WS1 to WS2 or WS to FT testing). Data Feed Forward helps in uploading the Pass/Fail core information of the first insertion to tools like Optimal+ (O+) and in the subsequent insertion it can be downloaded. Every Partial Good Test Flow works by downloading Partial Good Array data from previous insertions (Data Feed Forward), convert Optimal+ Feed Forward data to local Partial Good Test Array, execute the tests in the flow (excluding the failed cores). Each PG test-suite will execute the test and update the test array in real time. At the end of the flow execution, devices are binned out based on test results and Upload Partial Good Test Array to O+ for future insertions

Tessolve Engineering Challenges Contest [TECC]

1. 1ps Jitter Clock Generation for 93K LB

Vinayaka L G – Test Manager

Abstract

This article will describe the generation of High Speed clock frequency with jitter as low as 1ps. The key approach used to have the clean clock frequency is:

- By using Si5338 IC which is an I2C programmable, quad clock generator which generates output of 0.16 to 710 MHz (Low phase jitter of 0.7 – 1.5 ps RMS type).

Considerations and challenges

Frequency with low jitter is one of the critical parameters in testing and most important factor of consideration for test engineers.

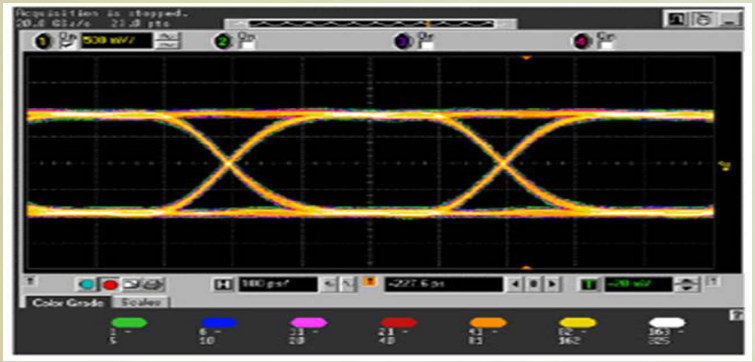


Figure 1: Waveform without Jitter

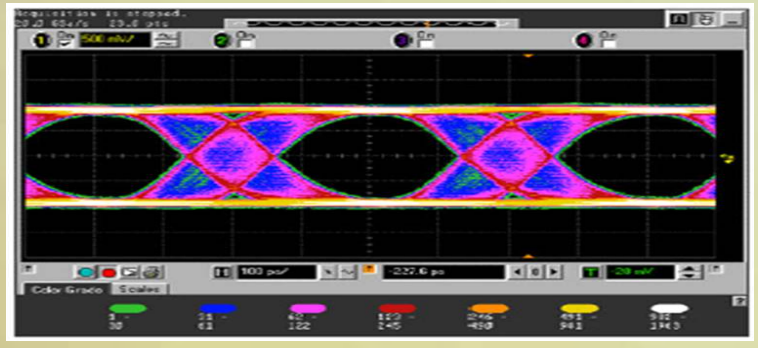


Figure 2: Waveform with jitter

Higher jitter causes timing variations of a set of signals from their ideal value and degrades signal quality. To achieve such low clock signal jitter, we used an external clock module, as the cards PS1600 (80pSec) and best module from Advantest PS9G card (18pSec) was not able to meet the need of 1pSec.

Additional challenge was to integrate the s/w, as programming s/w from Silabs was supported only in Windows OS and our ATE uses Linux platform.

Approach and Solution

To address these challenges/issues, we undertook below approaches and solutions:

- Since the clock generator chip was programmable through I2C communication so we decided to program the chip through I2C from the tester
- Si5338 Evaluation Board (EVB) chip is programmed directly through the "ClockBuilder Desktop" a GUI S/W from Silabs.
- Now with Usb power from computer and I2c data from tester, we were able to successfully program the module and get output frequency.

By taking reference from the Layout file of the EVB, we designed Daughter Card.

Figure 3: Daughter Card Top view

Figure 4: Daughter Card Bottom view

Jitter Measurement

- Using the inbuilt Jitter/Noise Analyzer Wizard, we did single ended jitter measurements on all clock out channels.
- This wizard also provides an option to calibrate the probe being used.
- Jitter values were recorded after 1M transitions had taken place.

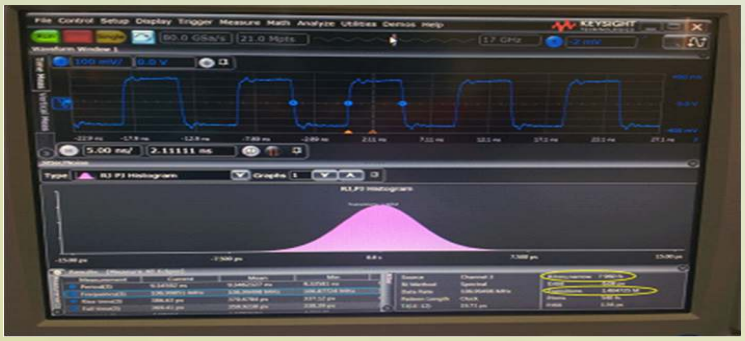


Figure 5: Jitter/Noise Measurement after daughter card installation

Improvisation

- Right now through GUI based software we are getting 359 hex bytes and converted them to serial (Excel macro 359*29 = 10411) data on 2 pins and store that into Sequential memory of tester.
- This can be done automated if we use D2S framework.

Conclusion

With the help of customized daughter card design & ported HEX code from GUI based software to 93K bin, we can generate <1pSec jitter free clock and successfully energized the module from Linux platform.

Figure 6: Daughter Card after final installation to ATE HW

2. Turret Contactor - A Challenging Library Part

Madhavan N - PCB Design Engineer, Loganathan P - Sr. PCB Design Engineer

Introduction

Tessolve library team has gone through many critical parts but this part "TIEM-(MSOP)10-0.50G0SP1.60C-FSS" (Turret contactor) is one of the peculiar among them. This part took lot of time to interpret to narrow down it as a footprint.

Nature of Challenges

Initial library creation request came for the Turret contactor with single image file attached (Figure 1) and a reference board file (Figure 2)which was used by customer in previous design.

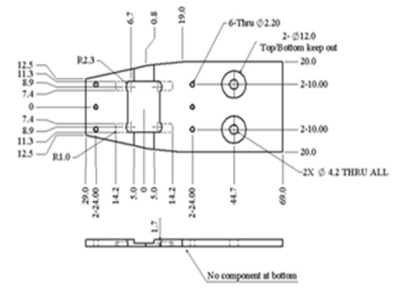


Figure 1: Turret connector Image

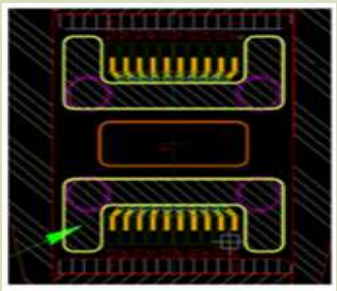


Figure 2: Initial Footprint received

While proceeding with library creation noticed that the cut-out used in the board file was different from the image file. From the side view it was found that the required footprint is entirely different from provided board file. After series of discussions with customer got a clear view that there will be 3-types of board cut going to be present in footprint (Figure 3).

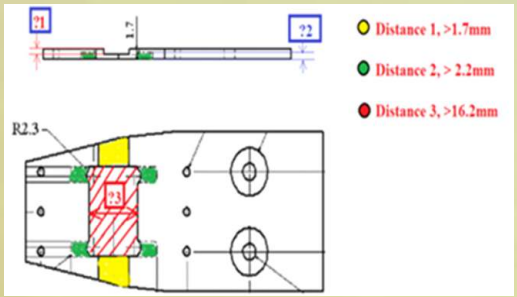


Figure 3: Different board cuttings

- Centre thru board cut-out (Marked in RED)
- Depth Board cut from TOP (Marked in YELLOW)
- Depth Board cut from BOTTOM (Marked in GREEN)

With above approach created the footprint with full details so that the Designer & FAB vendor can get a clear idea of the cut-outs. After a series of discussion with designer, the required design was clear and gave green signal for the footprint which was created (Figure 4).

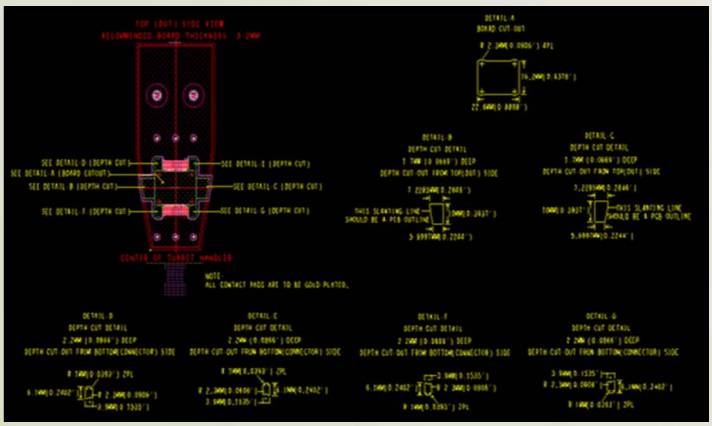


Figure 4: Final Footprint

Finally, the board was designed well with reference to the finalized footprint and later received the pictures of the board (Figure 5) from customer with good note.

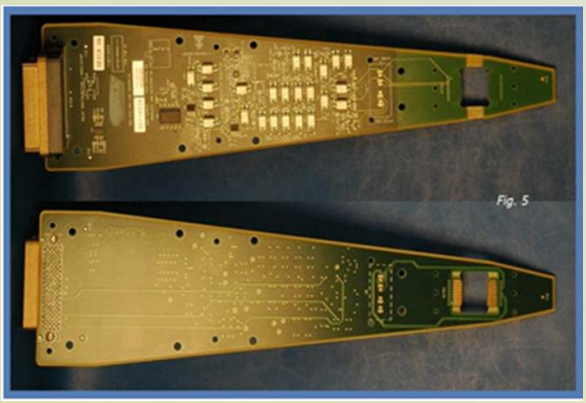


Figure 5: Final HW after assembly

3. Sine wave generation for Phase measurement test on 93K

Santhosh Kumar M – Test Engineer & Aravind Lijoy – Sr. Staff Engineer

Objective

Phase measurement block of the DUT senses the phase of input sine wave with respect to every instance on Reset input signal's falling edge and converts the phase difference to digital value on 'Adcout' pad. To check this phase conversion capability, the phase ranges from -45mRad to 45mRad is needed to be measured in 453 measurements on a sine input of 80uS period. To achieve this smallest resolution, reset input signal need to be adjusted through digital stepping.

Key Challenges

1. Down converting/cyclizing the patterns to achieve the smallest resolution on reset input signal.
2. Measuring the trigger to signal delay using digital capture and compensating the same through the pattern
3. Aligning the input waveform phase instances with respect to the Reset input signal falling edges.

Specifications of Analog Source (HF-AWG)

Si. #	Specification	Value
1	Sampling rate	8 ksps to 200 Msps
2	Resolution	16 bit
3	FMax. sine wave	25 MHz @ 100 Msps[1)]
4	Output range(AC+DC)	1.5 V < AC+DC < 1.5 V @ 50 Ω to GND
5	DC offset range	±1.25 V @ 50 Ω to GND, 15bit resolution
6	Output impedance	50 Ω nominal
7	Filter	Through (32MHz), 1.5 MHz, 15 MHz
8	Trigger to Signal Delay	5uS+/- 10nS
9	Absolute DC accuracy	±0.4 % of setting ±8 mV ±0.2% of DC Offset @ > 10 kΩ load

Test Setup

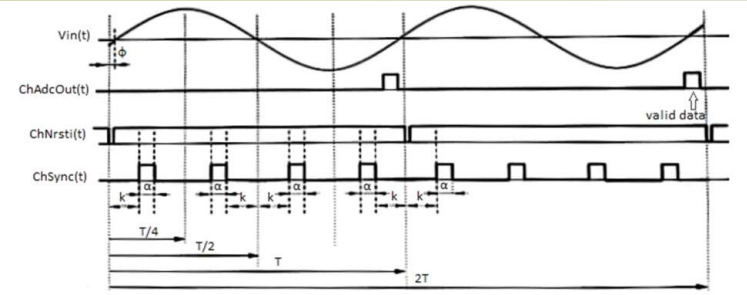


Figure 1: Test Setup for Phase Measurement

I. Pattern Cyclization

The pattern provided by customer is cyclized at 40nS. Hence the patterns need to be down cyclized as per below calculations to adjust the reset input signal.

Measurement Range: -45 mRad to 45mRad (90 mRad)

Number of measurements: 453

Phase resolution for each measurement: 198.67 µRad (90 mRad/453 steps)

Convert above calculations with respect to time:

Input sine wave frequency: 12.5 KHz (80µS)

Radians for 1 cycle of sine: 2π Rads

For 1Rad, time elapses: 12.72 µS (80 µS/2π rads)

For 198.67uRad, the time needs to be elapsed: 2.528 nS (: 12.72 µS *198.67 uRad)

The nearest period which is a divisor of 40nS is 2.5nS. Hence down converted the pattern with 2.5nS period. The test pattern is executed with this cycle period i.e. at 400MHz.

II. Compensating the delays

According to the Advantest technical documentation, the trigger to signal delay for HF AWG is 5µSec ±10nS. This delay we need to compensate through the pattern by triggering the AWG early, which is equal to the delay. This delay might vary from tester to tester and board to board. To avoid this uncertainty, we have provided a back-up option through DNI resistors as shown below.

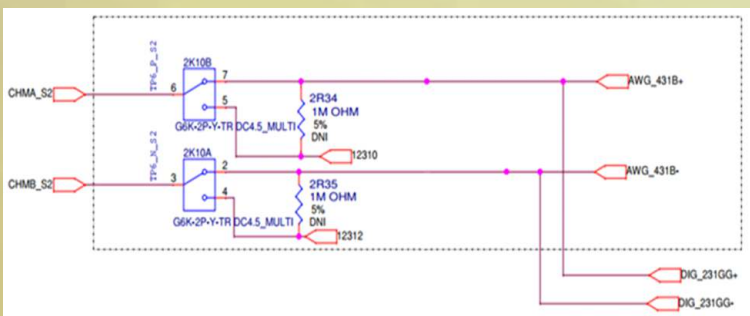


Figure 2: Phase Measurement Block

Before executing the test, AWG is triggered and the response is digitally captured on the digital channels 12310 and 12312 as shown. By multiplying the number of cycles delay AWG has taken to outsource the wave form with the period (2.5nS in this case) will become the actual trigger to signal delay. Hence in the real execution of the test, the AWG will be triggered the same number of cycles early in the pattern.

After several observations, we understood that, the uncertainty is always within the ±10nS as promised by Advantest. Hence fixed the same triggering point instead of measuring every time.

III. Alignment of Waveform

a) Measuring the positive phase (0 mRad to 45 mRad)

Compensating the trigger to signal delay aligns the starting point of the Sine (0' phase point) to the falling edge of the reset input signal. The phase of the waveform is shifted by 196µrad for each measurement, by moving the Reset input signals edge by 1cycle (i.e.2.5nS) for every 160µS (for every two periods of sine wave). The converted phase value is digitally captured through AdcOut pad. In this way by incremental digital stepping, the positive phase from 0 to 45mRad can be measured.

b) Measuring the Negative phase (-45mRad to 0 mRad)

To measure the negative phase, the reset input signal must be moved in backward direction, which is same as (2π-45mRad) phase point. Hence the trigger point needs to be set at a position such that, the -45mRad phase instance would align with the falling edge of reset input signal. This is achieved by moving trigger point to the exact location in the pattern, retrieved by back calculation as below.

Tester period: 2.5 nS

Sine Input period: 80 µS

A complete sine input can be aligned to 32000 (80 µS/2.5 nS) digital cycles. Hence to achieve -45mRad, Reset input signal needs to happen nearly 230 cycles early from '0' phase location.

Hence digital steps/cycles required for:

Trigger to Sig delay: 5 µS/2.5 nS = 2000

-45mRad point: 31770

That is, Reset input signal should go low, after (31770 +2000) cycles from AWG triggered, so that required phase point will be aligned to reset input signal's falling edge.

Conclusion

By following the above 3 methods, we achieved the aligned and able to measure the required phase from Sine.

TESSOLVE

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Tessolve Semiconductor Pvt. Ltd.
Plot # 31, Electronic City,
Phase 2, Bangalore 560 100,
Karnataka, India
Tel: +91 80 4181 2626
Fax: +91 80 4120 2626

Tessolve Semiconductor Pvt. Ltd.
65, 35th Main, 100ft Ring Road,
BTM Layout 2nd Stage,
Bangalore 560 060, India
Karnataka, India
Tel: +91 80 6699 5800
Off: +91 80 6699 5873

Tessolve Semiconductor Pvt. Ltd.,
Excellence - 5th Floor,
104, Race course road,
Coimbatore - 641018,
Tamilnadu, India
Tel: +91 422-2221199
Fax: +91 422-2490573

Tessolve Semiconductor Pvt. Ltd.,
OCAC Tower, Suite # 215,
Gajapati Nagar,
Bhubaneswar - 751013
Odisha, India
Tel : +91-674-6592999

TessolveSemiconductor Pvt. Ltd.
S-3 & S-4, 2nd Floor, Land Mark Building
Sampath Vinayaka Temple Road
Visakhapatnam - 530003
Andhra Pradesh, India
Tel : +91 91001 64949
+91 91002 74949

Tessolve Engineering Services Pte Ltd.,
Blk 20, Woodlands Link, #06/20
Singapore 738733
Tel : +65 6297-9613

Tessolve Semiconductor Sdn. Bhd.
Koridor Utara Malaysia
Plot 36, Hilir Sungai Keluang 2,
Kaw. Perusahaan Bayan Lepas Fasa 4,
11900 Bayan Lepas, Pulau Pinang
Malaysia
Office: +604 637 0672
Mobile: +6012 528 9996

TessolveDTS Inc.,
14567 Big Basin Way Unit A3,
Saratoga, CA 95070
Tel : +1 408-865-0873
Fax : +1 408-865-0896

TessolveDTS Inc.,
1702 N. Collins Boulevard, Suite 161,
Richardson, TX 75080
Tel : +1 972-290-0172
Fax: +1 972-437-9348

Tessolve Semiconductor GmbH.,
Wöhlerstraße 29
30163 Hannover,
Germany
Email : info_gmbh@tessolve.com

For enquiries or feedback Contact:
sales@tessolve.com / news@tessolve.com
www.tessolve.com