TESSOLVE
Delivering Excellence in Semiconductor Engineering

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FIRST BIN

a newsletter for the semiconductor engineering community

Contents

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FROM THE PRESIDENT'S DESK

Srinivas Chinamilli

Dear Customer,

At the outset, let me thank you for your support in the last 6 months. We have continued to grow in spite of tough business conditions in the first half of the year. We have just crossed 1000 employee mark!

We are continuing to invest in expanding our engineering capabilities to better serve you.

You probably would have heard by now that Hero Electronix has taken a majority stake in Tessolve. We are happy to be associated with Hero organization, which is well known for its business ethics and leadership. There is no change in Tessolve organization structure and we are fully committed to continuing to provide world-class engineering solutions.

We have further strengthened our embedded systems design capability by acquiring Indian arm of TES-DST holdings, Germany. TES brings with it expertise in designing various embedded system products especially in the multimedia space.

With this acquisition, we have a 60+ member team of highly talented engineers in embedded hardware and software engineers.

We have also started a design center in Bhubaneswar with a group of highly talented engineers in the Design Verification space.

I am also happy to inform you that we have been selected as NI Alliance partner. We have been very successful in developing test solutions on their newly launched NI STS tester platform and we are delighted that NI has chosen us as their specialty test partner. We have installed two STS platforms with capabilities in mixed signal and RF test on our test floor in Bangalore.

I would like to take this opportunity to congratulate Justin Jacob, Harish Bodappatti, Manikandan Panchapakesan and Lokesh Babu P for their paper presentation on "Fault verification of Safety Centric Automotive Mixed signal chip" at CDNLive India 2016 and being awarded as Best Paper award. I would also like to congratulate V.M. Kameshvaran and D. Vijayakumar for their paper presentation on "Intelligent data transfer between Design, fab and assembly using IPC-2581" at CDNLive 2016,

I look forward to working with all of to forge even tighter partnerships in the months to come.

TESSOLVE SHOWCASE

1. Carbon Nanotubes as Field-effect Transistors

Sree Harsha Parimi - Design Engineer

Abstract

In the present day scenario of VLSI industry there are many issues cropping up while integrating more and more transistors like short channel effect, power dissipation, scaling of transistors etc. This paper enumerates on how these problems can be overcome with the use of Carbon Nano Tube (CNT) in the place of silicon in future MOSFETs. It also throws light on some potential problems and possible solutions associated with the technology. The CNT is emerging as a viable replacement to the MOSFET.

Introduction

As the MOS device dimensions such as channel length approach to the sub-nanometer regime, direct tunneling between source (S) and drain (D) and severe short channel effects present a fundamental challenge in continued scaling of silicon devices. As researches concluded that transistor smaller than 7nm will experience quantum tunneling through their logic gates.

Tremendous research efforts have diligently been undertaken by various academic and industrial research groups to integrate new semiconductors instead of conventional silicon and germanium as the channel material in MOSFET, to enable (i) more efficient transport of charge carriers that are having higher mobility and (ii) improved electrostatics at nanoscale. CNT technology seems promising with

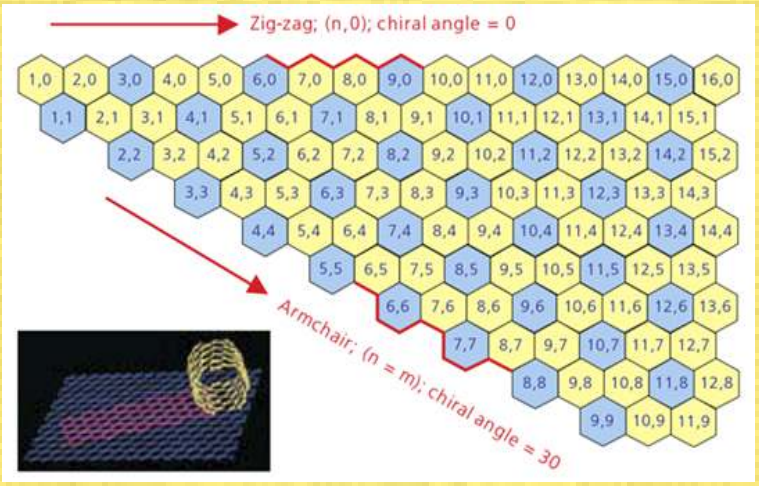


Figure 1: 2D Graphene Sheet
(courtesy: Richard Jansen, Philip Wallis, Material Matters 2009, 4.1, 23)

respect to above mentioned aspects due to the unique mechanical and electronic properties. Semi-conducting carbon nanotube can be used as the channel in Carbon Nanotube Field Effect Transistor (CNTFET). One of the major advancements of CNTFETs over MOSFETs is that the channel of the former devices is formed by CNTs instead of silicon, which enables a higher drive current density, due to larger current carrier mobility in CNTs compared to bulk silicon

Figure 2: Single walled and multi walled nanotubes
(courtesy: http://cnanotubes.blogspot.in/)

CNTFET Advantages

- **Speed:** The carbon nanotubes have a ballistic transport mechanism. As a result the charge carriers do not collide, reducing the resistance to almost negligible. The result is a capability to achieve speeds of Terahertz or more, compared to today's processors that operate at 3 gigahertz.
- **Power:** The leakage associated with CNTFET is 70% less, as compared to the conventional MOSFET. This means that the power being wasted while the transistor is off is greatly reduced.
- **Cost:** The scaling of MOSFET devices increases the fabrication cost. In 2006, the cost of a fabrication line was $5billion and now it has gone beyond $10billion. This cost can be reduced if fabricating units are set up for CNTFET.
- **Power and Delay Analysis:** The Average power, delay and Power delay product shown in Table 1.

	MOSFET (32 nm)	*Stanford UniversityCNTFET(32nm)*
Average Power	6.7035 µW	232.2 nW
Delay	52.811 ps	18.27 ps
Power Delay Product	0.354 fJ	4.242 E -18 f

Table 1: Average power, delay and power delay product

The designs are simulated with operating voltage of 0.9V. The analysis shows that the Stanford 32nm CNTFET model design is more efficient than the 32nm MOSFET design.

Problems to Solve

- **Chirality:** At times it is difficult to control the rolling of graphite sheet which will determine whether the nanotube is metallic or semiconducting. Due to this device characteristics might change.
- **Difficulties in mass production:** Although CNTs have unique properties such as stiffness, strength and tenacity compared to other materials especially to silicon, there is currently no technology for their mass production. To overcome the fabrication difficulties, several methods have been studied such as direct growth, solution dropping, and various transfer printing techniques.
- **Proper Simulation Tools:** Currently there is no accurate model to use for simulation of circuits using CNTFETs.

Recommendation

Though CNTFETs pose some initial problems on the grounds of mass production and control mechanisms, the technology on the whole, seems definitely promising to the future of VLSI, as its advantages are immense such as high drive current, large trans-conductance, high temperature resilience and strong covalent bonds. As we are using ballistic transport mechanism the chance of electron scattering is very less and due to this, resistance will reduce and delay of the transistor will also reduce. Since it operates in lower voltages, power consumption is also less compared to MOSFET. To control whether a nanotube is metallic or semiconducting problem can be solved by placing coaxial material on it. So, CNTFETs have a promising role as the FETs of the future.

TESSOLVE ENGINEERING CHALLENGE - CASE STUDIES

1. Solder Pad Land Pattern (SPL) – Auto Creation

Selvaraj S - PCB Design Engineer

Scope of work

This document describes the Solder Pad Land Pattern (SPL) automatic creation in Mentor PADS with its X, Y co-ordinates input (either text format or AutoCAD dxf/dwg).

Nature of Challenges

Mentor PADS EDA tool don't have any provision to create the Solder Pad Land Pattern (SPL) library foot print automatically with its pin no. and X, Y co-ordinates. As per customer input we need to place each pins manually especially for staggered pattern due to EDA tool's restriction. If more than 1000 pins are to be placed manually, it would take around 12 hours for SPL pattern creation.

Problem Description

There is high possibility of critical human errors in manual placement such as typo in pin numbering or pin location swapping which can lead to board scrap or re-spin, causing a waste of money.

Execution of Script for Text inputs

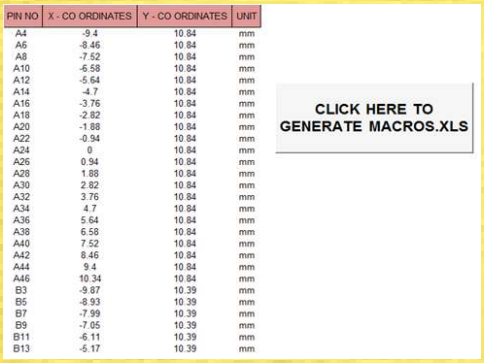


Figure 3

- Once the inputs in either Excel or text format is received, those inputs shall be fed into the Mentor PADS SPL auto placement

script.xls which was developed specially for SPL placement.

- The auto placement code shall be generated by clicking the generate macros button as in Figure 3.
- This script uses Visual Basic and is converted into macro (*.mcr) format which is recognized by Mentor PADS EDA tool.
- Then this generated script shall be loaded into Mentor PADS. Once the RUN button is pressed, the EDA tool will start placing the pins immediately. SPL pattern with about 1000 pins will be created within few seconds without any errors as in Figure 4.

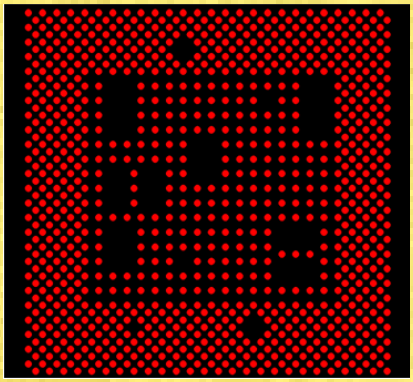


Figure 4: SPL pattern created by using developed script

- In order to place one pin, 8 lines of VB code is required. If we need to place around 1000 pins then there will be 8000 lines of VB coding in this script. These codes will be read by Mentor Pads EDA tool and pins will be placed within few seconds.

Execution of Script for AutoCAD inputs

- The figure 5 shows the SPL pattern input we receive from customer

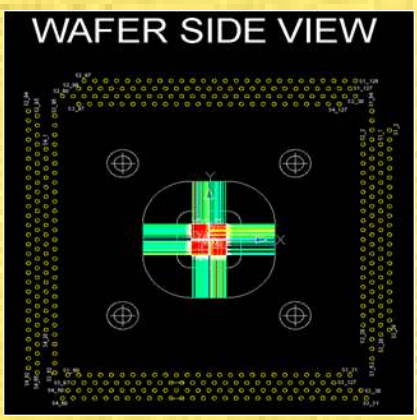


Figure 5: SPL pattern received from customer in AutoCAD format

- If the input is received in AutoCAD format, then the X, Y co-ordinates and pin no. from given diagram or dxf shall be generated by a lisp program as shown in Figure 6.

A1	-1.331118	1.080000
A4	-1.331118	1.000000
A15	-1.136118	0.800000
A12	-1.136118	0.880000
A23	-1.136118	0.640000
A18	-1.136118	0.720000
A14	-1.266118	0.800000
A11	-1.266118	0.880000
A10	-1.331118	0.920000
A13	-1.331118	0.840000
A22	-1.266118	0.640000
A19	-1.266118	0.720000
A20	-1.331118	0.680000
A29	-1.331118	0.600000
A16	-1.331118	0.760000
A17	-1.201118	0.760000
A21	-1.201118	0.680000
A28	-1.201118	0.600000
A5	-1.266118	0.960000
A9	-1.136118	0.960000
A40	-1.136118	0.400000
A36	-1.136118	0.480000
A52	-1.136118	0.160000
A48	-1.136118	0.240000

Figure 6: X, Y Co-ordinates generated from AutoCAD by a lisp program developed

- Then the all circles will be converted into block and pin numbers and will be assigned by using specially developed lisp. Then we will get the Pin no's, X and Y co-ordinates.
- The generated reports shall be imported in Mentor PADS SPL auto placement script.xls and the *.mcr file will be output which can be loaded in Mentor PADS. As said above then SPL pattern will be created within few seconds.

Advantages of this script

- This script is very useful in maintaining quality consistently as it causes 0 defects in SPL pattern creation.
- This script shall reduce the SPL pattern creation time by about 90% thus improving cycle time.

Conclusion

This kind of script development is useful in making an error free product for the customer and also reduces the turn-around time.

Time taken for creating each SPL pattern based on the pin counts (automatic) = 2 man hours

Time for creating each SPL pattern based on the pin counts (Manually) = 14 Man Hours

Time saved by adopting the automatic method over manual method = 12 hrs.

2. Multiple Frequency Measurements on Multiple Pins in a Single Test

Vidyut Yagnik - Sr. Manager, Harihara Reddy N S - Test Lead & Venugopal Vadde - Test Engineer

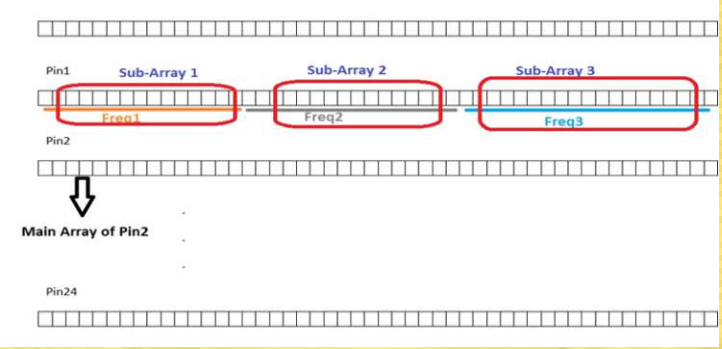
In this article, we touch upon the methodology developed for measurement of multiple ring oscillator frequencies routed on multiple pins inside the same test pattern. This device is an IO standard cell library test chip for 28nm design. Characterization of this device has to be carried out for each individual on-chip module.

This design had more than 2500 ring oscillator tests and for each ring oscillator test frequency measurement has to be done. These ring oscillator frequencies (1.56MHz, 2.4MHz, 3.6MHz, 8MHz, 12MHz, 16MHz, 20MHz, etc.) are routed to 24 top levels IO pins of the device.

Adding and capturing these measurements for all ring oscillators is the main challenge involved on ATE. Missing even one cycle of a particular ring oscillator test will result in a wrong frequency measurement for the remaining ring oscillator test frequencies on the ATE. To measure all ring oscillator frequencies accurately below are the steps followed and error-preventionmeasures taken during the execution of this project.

Tester Setup

The designer provided a list of tests for frequency measurements with



time stamp info and ring oscillator name. Since the frequency values to be measured are small, patterns were created with more sampling period for accurate measurements.

For all 24 pins in the particular test, 24 different capture variables were added. All the 24 capture variables have to be captured into 24 different arrays through ATE test method coding.

Based on the time stamp, a look-up-table (LUT) was created, which would provide the starting and ending cycle numbers for any particular RO-test/Frequencymeasurement-test of a particular pin. Based on the cycle number info given in the LUT, this codecreated sub arrays for each pin.

Frequency measurement using FFT technique and Tabei-Ueda interpolation algorithm

- Each captured sub array of the pin and sampling period (tester cycle period) will be given as input to the function.
- Based on the captured sub-array and sampling period it does the FFT processing and calculates the frequency spectrum.
- Also spectrum will be processed with Hanning window in order to improve the spectrum fundamental component and reduce spectral leakage.
- After calculating the frequency spectrum, DC-Component of the spectrum will be made "0".
- Max frequency bin index(kmax) will be determined from the resulting spectrum, as well as its immediate neighbor with bin index((kneighbor) which has next higher strength in magnitude after the Max bin.
- Tabei-Ueda interpolation algorithm is applied on Max bin index and it's neighboring index, to get the direction and magnitude of the real frequency offset value(Delta "K") from the Max bin index (kmax).

$$\Delta k = \frac{1 - 2\left[\frac{V(k_{neighbor})}{V(k_{\max})}\right]}{1 + \left[\frac{V(k_{neighbor})}{V(k_{\max})}\right]}$$

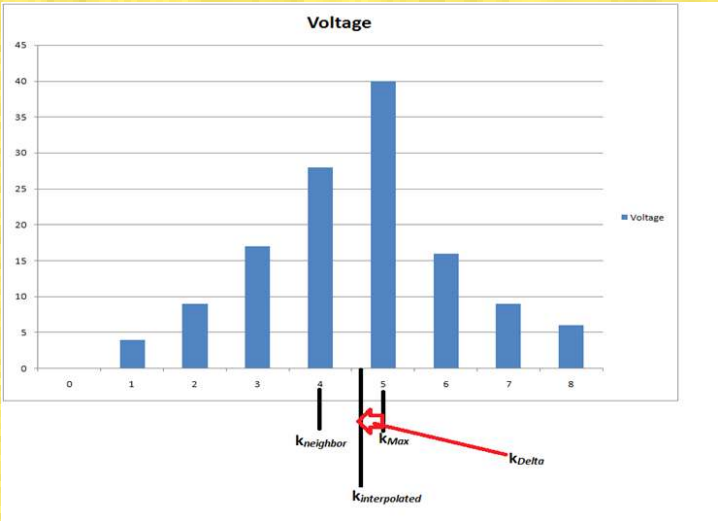
- Depending on the sign and magnitude of *Delta K*, value of the interpolated bin index is calculated using this formula below.

$$k_{interpolation} = k_{max} + \Delta k$$

- Then from the bin index Kinterpolation, Frequency is calculated using the following formula

Fmeasured = Kinterpolation/(Tester cycle Period * size of sub-array)

- Tabei – Ueda interpolation algorithm increases the accuracy of frequency measurement by interpolation. This will be more accurate than just reporting the Fundamental frequency component from the spectrum, which has bin index kmax in this case.



Since the test is over sampled with higher frequency, Nyquist criteria is followed to get the accurate values. Resultant frequency measurements will be compared with upper and lower limits provided in the LUT, pass/fail status of the particular RO test will be decided and reported into a log file along with frequency readings. The above process will be repeated for each sub-array of all the 24 pins and results will be logged into the report file.

Advantages & Limitations

Advantages

No additional ATE speed licenses required for performing this test. No limitation on the number of measurements for a test, since number of pins and capture variables are already taken care of in the test method coding.

Limitations

Nyquist criteria must be satisfied. For better results it is recommended to over sample the vector with a sampling frequency that is at least 4 to 5 times the target frequency to be measured. Since it is over sampled multiple times, capture RAM size will limit the number of capture values that can be stored for post-processing. But for all practical low frequency measurements the available memory should suffice.

3. Test Time Reduction Strategies for MBIST

Neha Ranjan- Test Engineer

Embedded memories are an essential part of any System on a Chip (SoC).The requirement arises not only to validate the digital logic against manufacturing defects but also to do robust testing of large memory blocks post manufacturing. MBIST (Memory built-in self-test) provides an effective solution for testing of such large memories. MBIST is a self-test logic that generates effective set of March Algorithms through inbuilt clock, data and address generator and read/write controller to detect possibly all faults that could be present inside a typical RAM cell whether it is stuck at 0/1 or slow to rise, slow to fall transition faults or coupling faults.

The main focus of this article is to emphasize on the test-time optimization done on Advantest 93K ATE platform for MBIST testing. With the below mentioned strategies we were able to reduce test-time from ~ **30 sec** to **4.2 sec**.

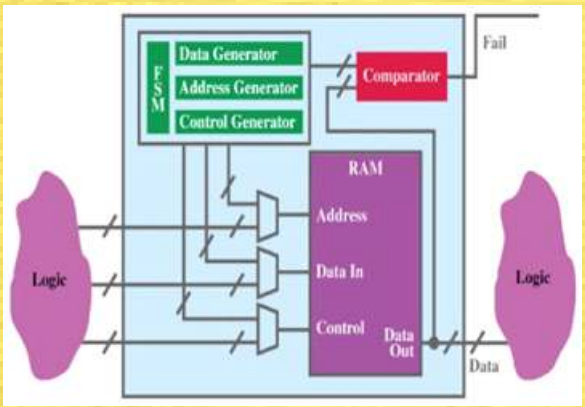


Figure 7: BIST Architecture

Clock Grouping

When 2 ports in the same multiport specification have vastly different periods, then unnecessary overhead is added to each test suite that uses that specification. In a typical project, we see as much as 4.5ms overhead per test suite affected. By clubbing the ports with similar frequencies together, we are able to significantly reduce the overhead test-time.

Avoid fract statement rounding error

Fract statement can be used with the period statement within the timing set.

Period: fract (<numerator>,<denominator>,<global var>)

PS1600 hardware makes use of fract() statement in timing file to accurately program the master clock in ATE to obtain the required frequency. Should pass integer arguments in the fract statement (MULT, Freq_Hz_t1, E6) to avoid the time taken by tester in rounding off the decimal places.

Port Order: Port with shortest tester period should be at the top of the port list in timing specification.

Toggle clocks using break waveforms: Clocks can be toggled using break waveforms and a single toggle in the clock bins. Replace the RPTV instruction or multiple vectors for clocks with single vector

Merge vectors as much as possible: Implementation of core merge patterns in spite of single core/single controller based vectors will significantly reduce test-time.

Optimize Repeat values within vectors: Usually ATE patterns will have multiple repeat instructions. We can minimize some of them. Reduce loop counts in initialization vectors for the pll lock duration and reduce loop counts in stil vectors for BIST done wait time. We optimized initialization vectors and test-time was reduced by 300 ms.

Remove go-id checks: Go-id checks help to localize failures to specific controllers, memories, bit cells, etc. They're required for diagnostic purposes, but can be removed during production testing.