TESSOLVE

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FIRST BIN

a newsletter for the semiconductor engineering community

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FROM THE PRESIDENT'S DESK

Srinivas Chinamilli

Dear Customer,

At the outset, let me wish you all Health, Happiness and Prosperity in the New Year!

It has been 6 months since the last newsletter. We have been very busy in this period. We have doubled our test floor space to accommodate more ATE equipment, handlers, SLT handlers etc. to address increasing customer demand for testing more products out of our Bangalore facility. This required a major upgrade to our facilities including chilled water plant, compressed air and other electrical infrastructure. Kudos to our operations team! They have worked very hard to make this happen in a record time.

Characterization lab is also coming up well. Most of the equipment have been received and the rest will be in house by mid of February. With this, Tessolve will be able to offer access to state of the art bench equipment to you to address your characterization requirements. You will be able to either rent equipment from us or have Tessolve engineers execute on your projects to fulfill your analog, high speed digital and RF characterization requirements.

Our HR team has been busy as well in aggressively hiring engineers. Our employee count has crossed 700. Our Test Engineering and PCB Design teams have delivered end to end solutions for several complex devices including baseband processors, microcontrollers, application processors, high precision analog and high voltage power management products. To further strengthen our production release and sustaining activities in Taiwan and China, we have established a partnership with a local Taiwanese company. Our VLSI design team has grown steadily to over 50 engineers offering solutions in DFT, design verification and physical design.

Tessolve also has been very active in offering mentoring program (as part of IESA and TIE initiative) to start-ups in the IOT (Internet of Things) space. Thanks to our Systems Design team for their efforts in offering valuable solutions to the participating startups.

I also congratulate our employees, Siva Vijayaraghavan for winning at the All-India PCB Design Contest 2014 conducted by IPC India at Bangalore, and Vijay David for successfully presenting a paper titled 'Robust PCB Library development, maintenance and parts search' at CDNLive Cadence User Conference 2014 conducted by Cadence at Bangalore.

We are continuing to invest in growing our talent pool and our equipment infrastructure to be able to serve you better and handle your increasing engineering needs.We look forward to engaging with you a lot more and strive even harder to provide value add services for you in 2015.

TESSOLVE SHOWCASE

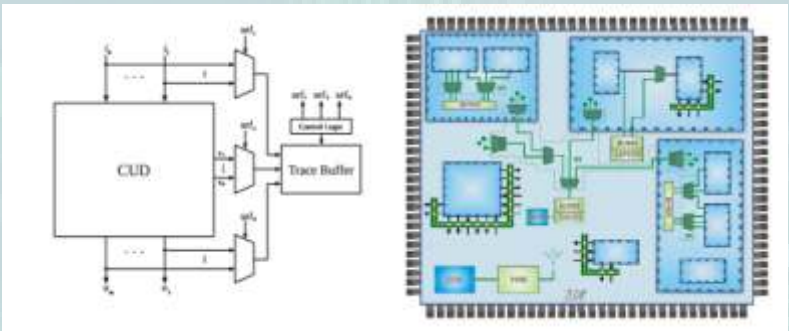
Debug Time Reduction in Next Generation SOC

Swetha Priya Aenikapati, Sr. Design Engineer, VLSI Design

As semiconductor manufacturing technology shrinks down to 14nm, micro architectural designs on a single SOC are becoming large & dense. Consequently test escapes into pre & post silicon verification stages are posing more challenges due to lack of internal node visibility. Eventually these test escapes are detected at system level, thereby adding to the cost of silicon. These systems typically contain at least 10 programmable processor cores packed into various slices with dedicated peripheral functions. This interface implements the standard communication protocols and hardware accelerators for configurable processing tasks with DDR4 and with other micro-architectural designs. As time to market is crucial, routing out bugs at such complexities require more number of vectors and run time. A couple of scenarios like non real time observation technique, Silicon debugging time and visibility were faced which brought out the inability of DFT.

Thus DFD (Design for Debug) is adopted as a solution to record & monitor the continuous real time signal information on a chip. DFD provides high degree of visibility to the internal nodes in-situ. However, limited resources like memory, pin count and low level abstraction threw challenges on internal observation of signals as integration levels are unfamiliar to designers. To overcome this tradeoff between hardware resource efficiency and number of signals, the following solutions were found to be good.

- Usage of DFD structures on top of DFT structures.
- Usage of mux-observation point and trace buffers in DFD insertion.



Block diagram of DFD structure on top of DFT structure

Figure shows huge multiplexer tree structure that picks up trace data and sends to trace buffers to capture data from selected signals to aid the debug process. The entire debug control system is automated with the help of mini taps at every unit which in turn is operated by master wrapper protocols with proper trigger control logic on trace buffers. This provides enhanced features like at-speed signal capture capability while tracking bugs at pre silicon and post silicon stages. This reduces the cost of system level test performance providing temporal and spatial bug information for failures in silicon at very high signal frequency greater than 64MHz without necessity of external logic analyzer and halt for debug data acquisition.

SOC Level Power Gratification in VDSM Technology

Umamaheswari Ganesan, Design Engineer, VLSI Design

Today semiconductor industry is emphasizing on the die size reduction and less metal layer technology process option to improve cross margins. The evaluation of VDSM technology faces new challenges as layout dimensions continue to shrink whereas the number of functions expected from SOC continues to grow. The uniform power distribution throughout the chip area is the key to have lower IR drop in the design. We need to provide reasonable number of horizontal and vertical power stripes with appropriate width as per the design.

Power Planning

It is the process of defining the power and the GND-net of the design specifying their structures which distributes power in the entire design. The key goals are listed below.

- Increase routing resource in design.
- Increase robustness of power grid network.
- Reduce cross talk noise.
- Improve IR drop.

In every SOC, metal layers are distributed in power and signal routes, metal densities are computed such that the power grid would support aggregate power and IR drop constraints. It creates conduction path between power supply and each component.

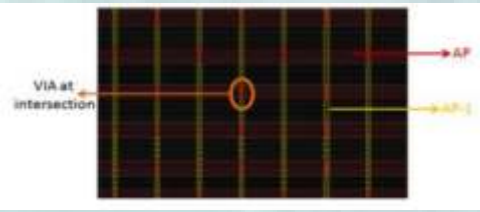
Power Grid Methodologies

Power grid is built with metal layers that used to supply power to whole SOC design. Based on technology option there are one or two upper metal layers with low resistivity. The upper most Aluminum layer (AP) has the least resistance and is mostly used for power grid designs such as

- Power Mesh.
- Power Ring.
- Power Rail.

Power Mesh

It is one or two repeated sets of pairs in horizontal and vertical segments that supply power to the core. The mesh can consist of a single net or a pattern of two or more nets that repeat at regular intervals across the design.



Conventional Mesh type Power grid Methodology

Power Ring

Core Ring

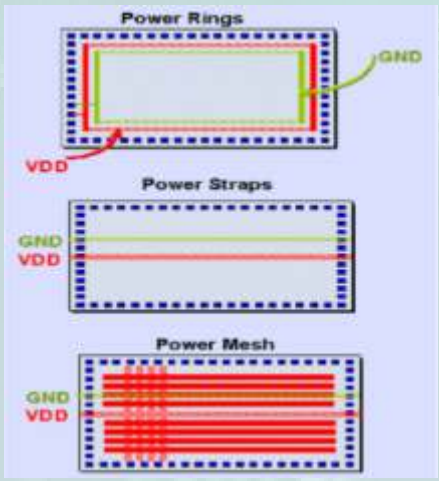
The ring that enclose the core with one or more sets of power and GND rings and provide external power from the pad ring to core structure. The top and bottom sides and any other horizontal segments of a core ring are located on a horizontal metal layer while left, right and other vertical segments on vertical layer via holes connect to the ring sides.

Macro Ring

A ring that enclose one or more macros with power and GND rings providing that macros with power. This ring does not always have 4 sides and they often have wire extension from one or more sides that connect to nearby power and GND wires of the same net.

Power Rail

Power and GND wires that supply power to the standard cells are placed in standard cell rows. Power rails draw power from rings and mesh to which they are connected. This is a single layer.



Structure of Gratification Methods

From all the above power grid methodologies, we can limit the maximum level of IR drop within the block and SOC level.

Achieving High Accuracy in Linearity Measurement

Thangaraj Aruchamy, Test Engineer, Test Engineering

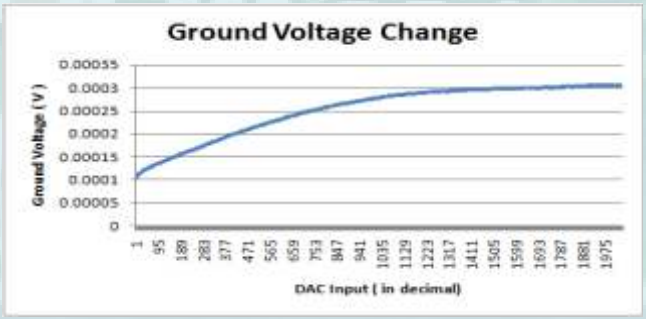
The transfer characteristics of Digital to Analog Converters (DAC) are defined by two key parameters

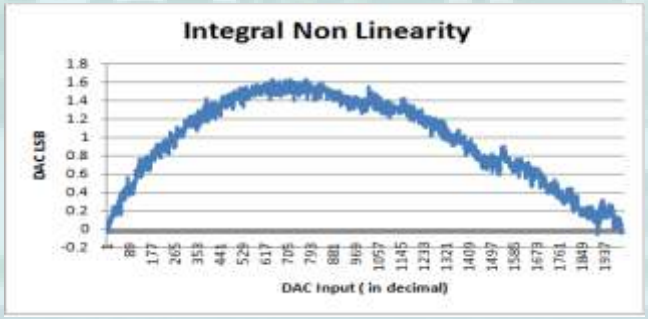
- Integral Non Linearity (INL)
- Differential Non Linearity (DNL)

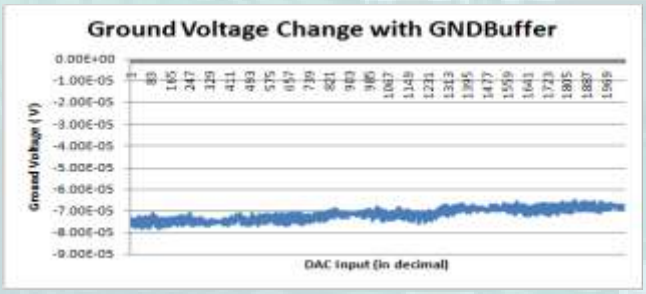
INL is used to measure the accuracy of DAC output voltage when compared to the ideal characteristics. DNL is the maximum deviation of an actual analog output from the ideal step value for successive input codes. In an ideal DAC one least significant bit change will produce $Vref/2^N$ change in DAC output. Linearity is a key parameter in applications like "Test & Measurement" which require DAC output voltage to be highly accurate corresponding to input digital code. Measurement of INL and DNL error is called linearity measurement.

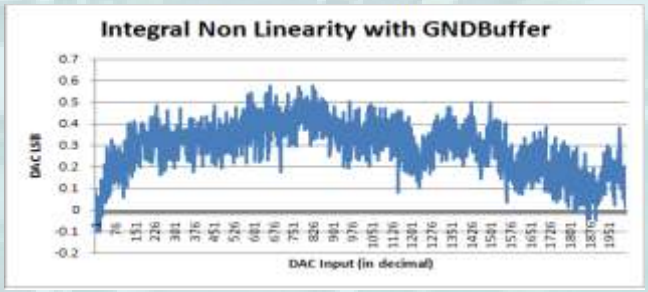
Board design for linearity measurement becomes challenging if the DAC resolution increases or the pin count reduces or multiple channels are present in a chip. If there are more channels the current drawn from reference and power supply will increase. Multiple channels sharing the single reference or the power supply and reference sharing a single GND will create IR drop in reference or GND traces. The IR drop varies with code changes since reference current is code dependent.

Reduction in LSB size demands more accurate voltage measuring instrument to measure the change in DAC output voltage. High accuracy instruments are slow









and expensive. Low accuracy instruments require on-board circuitry like high resolution pedestal DACs, PGAs, buffers, noise reduction circuits and filters. On-board components such as OPAMPS, switches and relays should be selected based on the offset error, gain error, CMRR, PSRR, on-resistance and capacitance. These have to be calibrated to obtain high accuracy. PCB routing and ground isolation also need to be done with great care. In addition parameters like drift in reference voltage, GND shift and contact resistance of the socket also need to be considered for improving linearity measurement.

Drift in reference voltage

The reference generation circuit should have low temperature drift, low line and load regulations, good long term stability and low noise. Any drift in reference will increase the INL value. Hence, drift in reference should be less than half LSB. Reference traces should be protected with guard traces. This will avoid noise affecting reference signal to change. Kelvin connection should be used to avoid IR drops.

GND shift & Socket contact resistance

The GND shift depends on code change and is avoided by using star connection and GND buffer. As shown in the figure above, GND voltage is increasing with respect to code and INL is reaching 1.6 LSB for 1 LSB DAC. Drift in GND directly causes drift in reference voltage. Socket contact resistance should be low.

TESSOLVE TEST CHALLENGE – CASE STUDIES

High Current Load Board Design – Consideration & Challenges

Selvaraj.S, PCB Design Engineer, PCB Division

In one of our turn-key projects related to power measurement units, there were multiple challenges like current can go up to 160 A, load board needs to be compatible for wafer as well as package level testing, needless to say cost needs to be low too. Special power slots known as Voltage Supply Modules (VSM) were used in TERADYNE ULTRA PA tester platform for this kind of high current application. Two different VSM slots were used in this project where each slot can support 81 A Max. The wafer and socket testing circuits had different types of restrictions in different areas, so placement was done by considering all the regions which resulted in the board being successfully deployed in both types of testing.

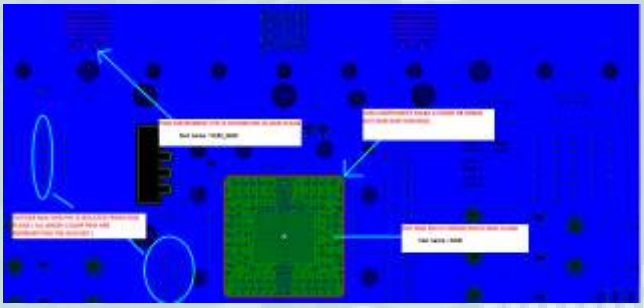
Risk factors in the design execution

- Two separate Power plane layers were used for core power (VDD Power domain). Each layer had 2 ounce copper to carry 160 A current.
- There are special requirements and tester mandatory lists like Force return should be connected to the plane which connects only to the DUT ground and all on board components/other instrument grounds should be isolated.
- The high current plane layer is sandwiched between the two different types of digital GND. One side had common digital GND and another had VSM GND. The Force return should use the VSM GND only.
- So we used 2.7 mil thickness of dielectric core between power to VSM and 7 mil prepreg was used between power plane and common digital GND. So Force return would go through separate VSM GND only due to less core thickness. Please refer the below stack up in the fab print.
- One IPC short was found during the IPCD 356 bare board net list matching against the Gerber which is a valid one viz. an intentional short which is caused due to VSM_GND and GND pin short.

Enhancements of VSM_GND in the current design

- VSM GND slot must have a separate GND path and VSM force should not return through common digital GND in the outside BGA. Special type of foot print was created and used in this design to short between DUT GND and VSM GND since it had a different net name.
- This foot print does not have any physical component, but it will connect the BGA GND pins and VSM GND pins alone in that particular VSM GND plane layers only. All other common digital GND layers will have enabled all the GND pins including BGA and on board component's GND pins except VSM GND pins.
- When such a high current return through the common GND, IR loss will be very high so separate return GND is required to make a return path.
- We cannot disconnect a few pins connecting from plane layer due to lack of tool possibility. So KPO Plane restriction is placed on the particular pins alone.
- Usually we place the KPO restriction on all GND pins and vias in outside BGA area, in order to make all on board components' GND pins and other GND pins disconnected in that particular VSM GND plane layers except BGA GND pins.
- But in this design we created a virtual GND short foot print to make a short between DUT GND pins and VSM GND. So this method is useful to reduce the cycle time for placing the KPO in all pins to disconnect the particular pins connecting from plane and can avoid the manual work too.

Virtual GND short component used to make a short between DUT GND and VSM GND, also used to isolate the GND pins outside BGA.



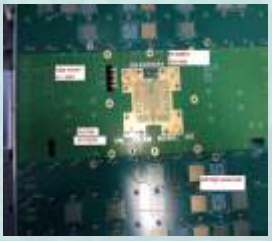
Voltage Supply Module:

This is special type of ground instrument which works at 6V/80A rating. Special requirements for this power supply is that the Force low should be connected to the plane which connects only to the DUT GND and all on board components/other instrument GND should be isolated.

Force high and Sense high are supposed to be shorted near the C load array. We have used 241 capacitors of 0.1uf, 31 capacitors of 22uf magnetically coupled to provide the required decoupling. In order to achieve the plane impedance for multiple GND layers with high current application we have used a number of low ESR capacitors to have high capacitance.

Critical signals:

- PCIE signals totally 55 RF PORTS were used for this device testing.
- TSC, Touch Screen, loop back - both transmitter and receiver are looped back to BGA itself.
- XG_PLL RF SIGNALS.



Conclusion

This design had lots of challenges like placing the components, critical signals routing, power and GND plane design, making the board work for both wafer and package level testing etc. The expertise gained from this design gives us confidence to handle upcoming projects at ease. This method will also be useful while designing floating instrument for high current applications.

High Speed USB Testing in Teradyne Test System

Karthik Chellappa, Test Lead, Test Engineering

Here we discuss how to test a high speed USB2.0 on Teradyne test platform. The tests include both edge search and digital capture tests for TEST0NACK/ OTG host transfer and test packet in which at least 32000 samples are to be captured using the digital capture Instrument in Octal mode timing.High speed USB testing is conducted at 480MHz. Only 4 pins are allowed to operate up to 800MHz in Octal mode timing. The captured 32 bit word has to be post processed to extract the two bit information using DSP compute block. The test time for this test is expected to be higher when we go with linear search method by sweeping the r2 edge from minimum to maximum in few pico seconds interval and get the best edge to proceed for the digital capture test. This uses the r2 edge which has the maximum width in the edge search algorithm. Here we describe the Interpolation method in which the edge can be estimated so that the overall test time for the test can be optimized. The method could be extensively used where the non-deterministic characteristics occurs within the clock period.

USB Edge Search Routine

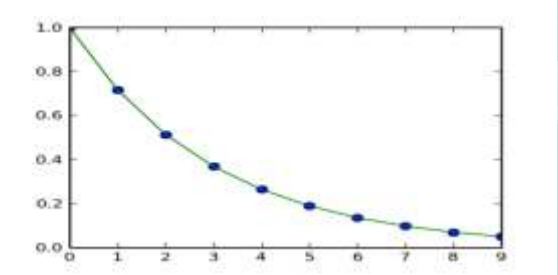
The USB Edge search routine will do two levels of search algorithm sweeping the r2 edge from minimum to maximum inside one clock period to find the window within the range. The second loop will do a similar search within the window to find the flat region within the window found using the coarse search. Edge search algorithm is executed for all the three tests.

- OTG Host transfer.
- TEST0NAK.
- TEST PACKET test and will help to find the edge to be used for the DSIO routine.

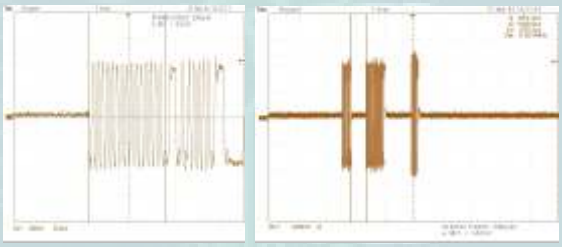
The test uses linear search algorithm which takes more time to sweep the entire range and as we also have an outer loop for two steps varying the VOD, the edge search routine suffers severe test time consumption before proceeding to the DSIO test.

Interpolation

Interpolation method using the Spline method or linear interpolation will help to estimate or approximate the range to be chosen for the edge search algorithm rather than sweeping the entire range



- Once the edge is identified based on the interpolation method and the variation/non-deterministic situation happens in the device in case of USB can be approximated to get reduction in the test time.
- Based on the verification using the spec search/shmoo method in finding the window for 5 to 10 parts will ensure the margin that is available in the edge placement.
- The sync pulse verification which has 127 samples of 10 toggling in the USB_DP will ensure the communication/handshake happening between the tester/USB PHY.
- The inter packet gap between the test packets will be ignored and only the useful information will be compared against the packet sent.
- If the error is zero for all 2bit samples (127 in the case of the TEST0NACK and the OTG transfer) and 32567 for the TESTPACKET will ensure the USB high speed tests are OK.



The test technique will be useful to quickly react to the non-deterministic behavior of the device within a clock period and will definitely help to save considerable amount of test time in the production environment.

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