TESSOLVE
test is our passion

VOLUME: 1 ISSUE: 1 JAN-2013

First Bin

a biannual newsletter for the test community

I. TESSPOD – Low Cost Test Solutions for Semiconductors

Necessity is the Mother of Inventions is a time-tested maxim, which holds true in the semiconductor test engineering industry wherein the challenges for test engineers are ever increasing. Tessolve has just the right answer to meet these challenges: The TESSPOD 28XX family of automated testers. TESSPOD ATE is configurable and extensible by seamlessly integrating third party instruments with proprietary instruments. TESSPOD is modular, re-configurable, open architecture, lower cost in multiple ways and ensures faster time to a lower cost test solution. *TESSPOD enables rather than constrains test strategies required.*

Featured above is a CMOS image sensor test solution built on the TESSPOD hardware and software platform by Tessolve.

Powerful software features, leveraging commercially off the shelf PXI and other bus instrumentation, device-specific configuration along with Tessolve's engineering team enables the customer to achieve a lower test cost, faster, through standard or application specific solutions.

TESSPOD Features

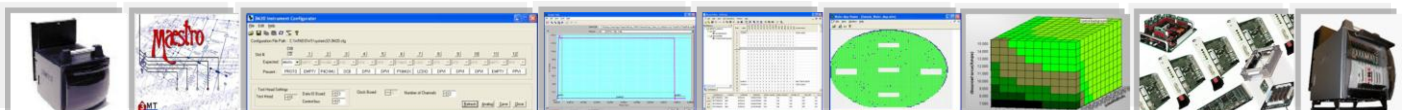
- 20 interchangeable slots for instruments.
- Broad range of DC, Digital I/O, AWG, Digitizer, DMM, etc.
- TTL I/O, RS232, USB, GPIB compatible Prober / Handler interfaces.
- Up to 168 pins via SIB from 3L instrumentation slots to DIB.
- Up to 16 ports for High Frequency / High Voltage / High Current.
- Up to 160 pins (32 ch instrument).
- Up to 80 user control bits.
- Software with support up to 128 test sites.
- Windows based Maestro software offering a wide range of software feature set and tools to support efficient programming, data collection and analysis.
- Microsoft Visual Studio based C / C++ programming environment.
- Seamless generation of 3D Shmoo, Line Shmoo, and Scatter Shmoo plots.
- Waveform capable Voltage & Current instruments with source and measure voltages up to 2500V and pulsed currents up to 100A.
- Scalable AWGs with sample rates up to 200 Msps.
- Scalable Digitizers with Sample rates up to 5 Gsps.
- 7 ½ digit high-accuracy DMMs.
- Digital I/O up to 100 MHz with PPMU.

Typical Applications

Analog SiP Devices | ASICs | Audio / Video converters | Automotive Power Devices | Battery Charger / Management Devices | Charge Pumped Drivers | CMOS Image Sensors | DC-DC Boost / Buck Converters | Defibrillator Devices | Digital SMPS Controllers | Power IGBTs / BJTs | MEMS devices | Laser Detectors | LED / Lamp / Panel Display Drivers | Linear / LDO / Switching Regulators | Power MOSFETs | MOSFET Drivers | Op Amps | PWM Switches / Controllers | Thyristers |

TESSPOD 2820 is designed adequately to deliver low cost Analog, Mixed Signal, and Digital test solutions for various test requirements including,

- Engineering and characterization test.
- Production test with prober or handler.
- Debug for failure analysis.



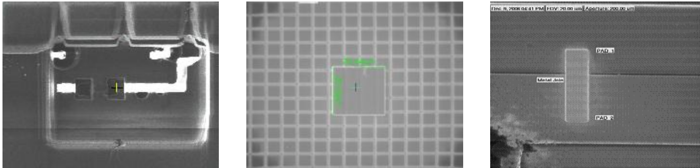
II. Failure Analysis

D Jaypal, Manager - FA Lab, Tessolve

A. Circuit Edit using Micrion 9800FC F.I.B. system

Features

- Metal cut
- Probe pad construction for probing
- Metal join using tungsten / molybdenum
- Via formation



Achievements

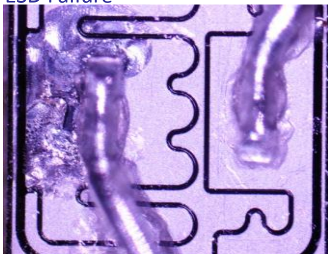
- 24 metals cuts on single device
- Longest metal deposition using tungsten (2400 µm)
- Smallest probe pad size of 0.5 µm x 0.5 µm up to 50 µm x 50 µm
- 20 probe pad construction on single device

B. Decapsulation using Nisene automatic / manual decapsulation

Features

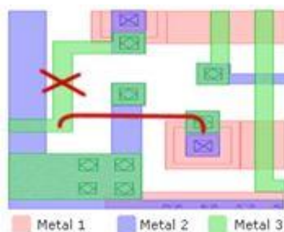
- Decapsulation of all packages using wet etch chemical process
- Selective area etching using precision drill bit for coarse removal

ESD Failure



1 mm x 1 mm

Circuit Edit

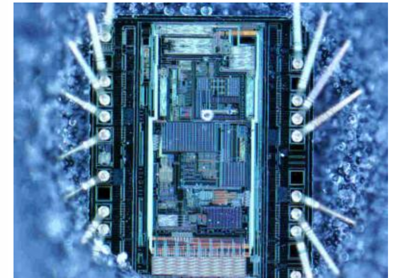


- Customized chemical etch for fine removal
- Programmable built-in 100 process recipes

C. Optical Imaging using Nikon LV150

Features

- Optical Magnification up to 1000x
- Digital zoom up to 1500x
- DIC mode
- Measurement software

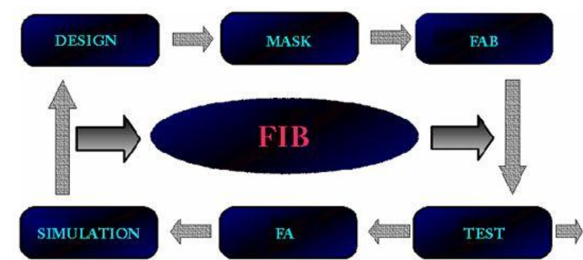


D. Hot Spot Detection using Liquid Crystal

Features

- K18R Liquid Crystal
- Clearing Temperature 29 °C
- Detect hot spot between 1 mw to 2 mw

E. Role of FIB in Circuit Edit



III. Tessolve Test Challenge - Case Studies

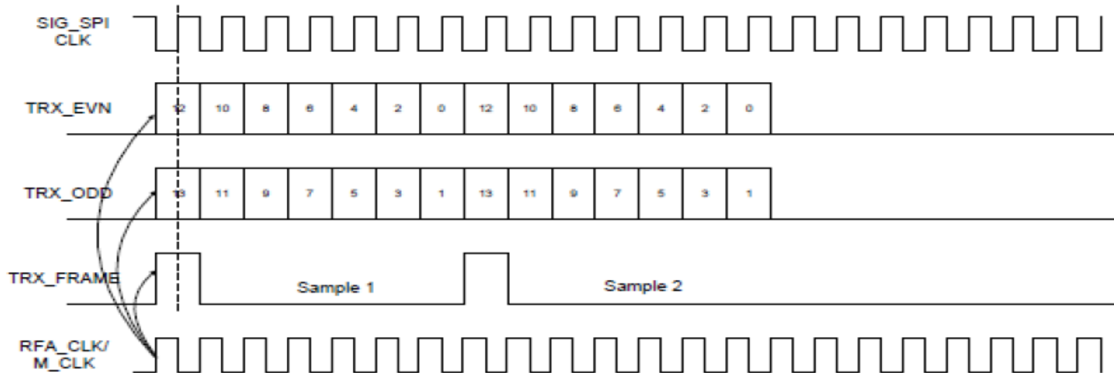
A. Test Time Reduction for RF Transceiver

Karthik Chellappa, Senior Test Engineer, Tessolve

We had two challenges for an RF transceiver data acquisition and reconstruction related testing requirement.

1. Test time reduction for the RF transceiver.
2. Reconstruction of 14 bit word from TRX_DATA_ODD & TRX_DATA_EVEN pins. ⅄

⅄ Let's look at the second challenge first. Data from the RF module is received from TRX_DATA_EVEN & TRX_DATA_ODD pins using 2 bit parallel DSSC. TRX Frame goes high once every 7 clock cycles as shown in this figure thereby indicating the MSB of the sample. The challenge lies in reconstruction of the 2 bit parallel capture being shifted, multiplied and summed up to obtain one valid sample data. The captured waveform is then rearranged by left shifting the MSB bit and performing multiplication of 2^n for the successive bits to get 1 sample. ❑



❑ We created a ramp signal with elements, 2^{12}, 2^{10}, 2^8, 2^6, 2^4, 2^2, and 2^0. Incoming data needs to be multiplied by this 7 element ramp signal. Now let us discuss the first challenge. Multiplication with ramp wave required a FOR loop which has to ☆

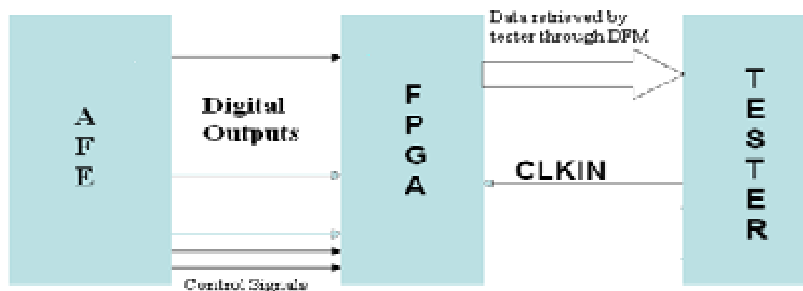
☆ process almost 55000 samples. We used convolution for test time reduction. The conventional method had a test time of 0.3 s whereas the new convolution based method took 0.04 s thereby saving considerable test time.

B. Digital capture using Advantest - T6372

Arun Siva, Test Engineer, Tessolve

Advantest-T6372 basically is an application specific tester which does not have instruments that ⌖

⌖ can support digital waveform sourcing and capture. We had an Analog Front End device with built-in ADC blocks to be tested in Advantest T6372 platform. ❍



❍ T6372 has an option to store the failed vectors while executing the pattern. We used the Digital Fail Memory (DFM) to capture the required digital data for ADC tests. The required a high level of synchronization between some of its control signals, clock and capture signals. The major limitation was that the depth of DFM was only 256 words per digital pin. But tests like linearity of ADC

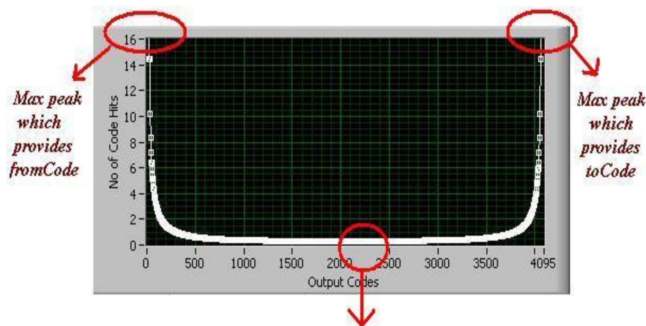
require large capture memory of at least 32 kB. Digital outputs from the device is continuous which cannot be captured using 256 bytes. So in order to overcome this memory depth issue we brought in a FPGA which can be programmed to act as a memory. Even though the test time will be high while retrieving the data to tester memory, as we pass only an array of 256 words from FPGA to tester in one shot, this is the best and safe working option we implemented.

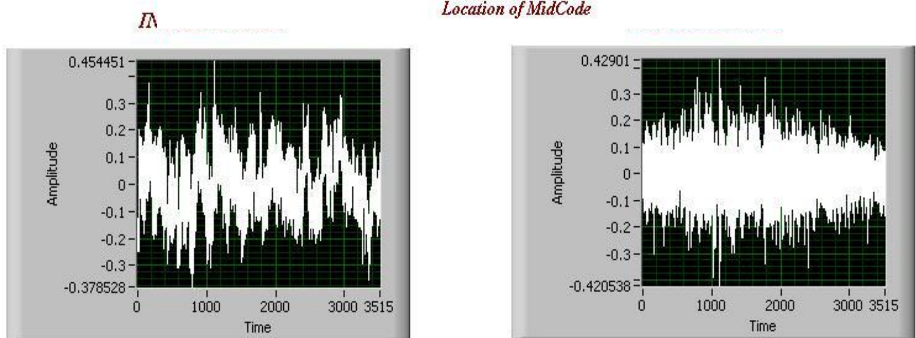
C. INL / DNL measurement using Sinusoidal technique

Y S Naveen, Test Lead, Tessolve

We had a challenge to do the static linearity measurements viz. INL / DNL using Sinusoidal techniques due to the need for more dynamic response and better characterization. We used "Cumulative Histogram” method along with “linear regression formula” and "Normal Histogram" method using Idealized histogram technique to calculate the INL / DNL. Sine wave spends more time near the upper and lower peaks than at the center. As a result, we would expect to get more code hits at the upper and lower codes than at the center of the ADC transfer curve. As we get more code hits near the peaks of the sine wave than at the center, the sinusoidal histogram of a perfect ADC exhibits a “bathtub” shape, as shown in the plot below.

We have verified our results with the data sheet specifications and it was matching very well on all aspects.





INL/DNL values obtained are as follows :

Parameter Name	Lower_Limit	Read_Value	Upper_Limit
minINL	-3.0000	-0.3780	5.0000
maxINL	-5.0000	0.4540	3.0000
minDNL	-0.7500	-0.4210	0.7500
maxDNL	-0.7500	0.4290	0.7500

Editorial Team

Advisory committee
Srinivas Chinamilli
TNK Sundararajan
D Rajakumar

Editor
S Parthiban

Operations support
Thirumalesh Babu

Publishing support
E K Senthil

For any enquiry or comments please send email to
sales@tessolve.com

Printed and published on behalf of
Tessolve Services Private Limited,
Electronic City Phase-2,
Bangalore – 560 100,
Karnataka, India.
www.tessolve.com