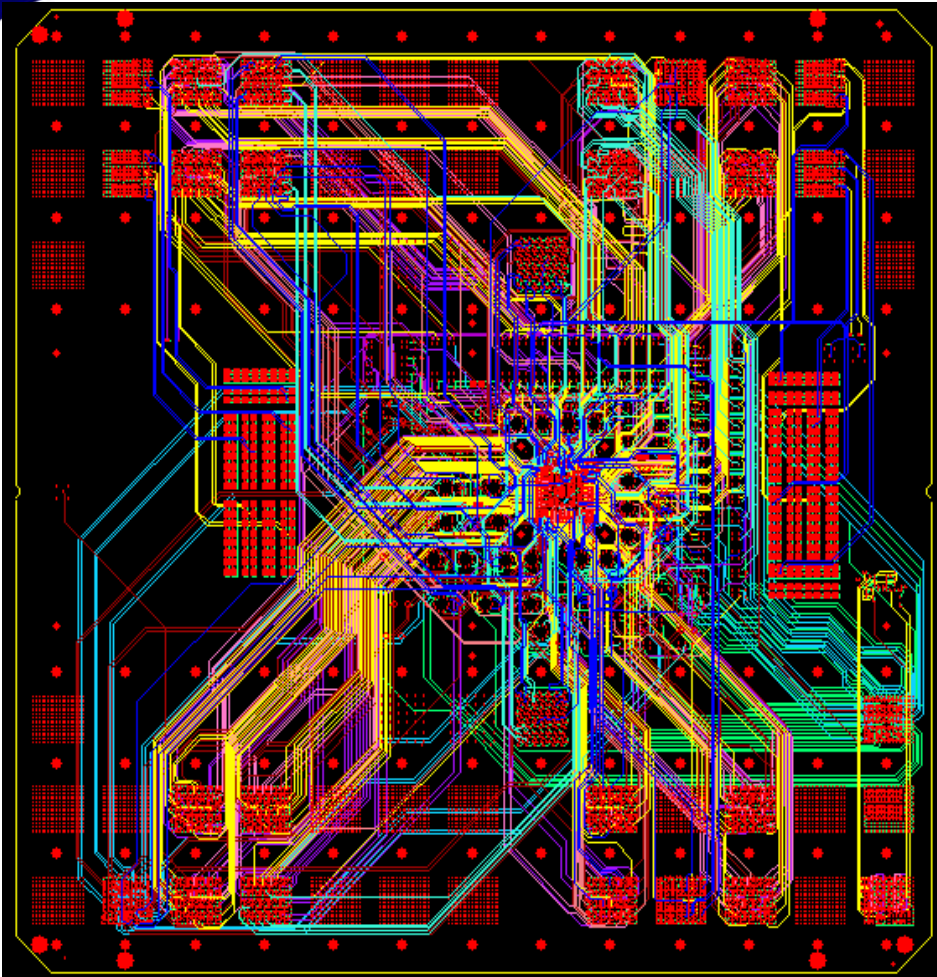


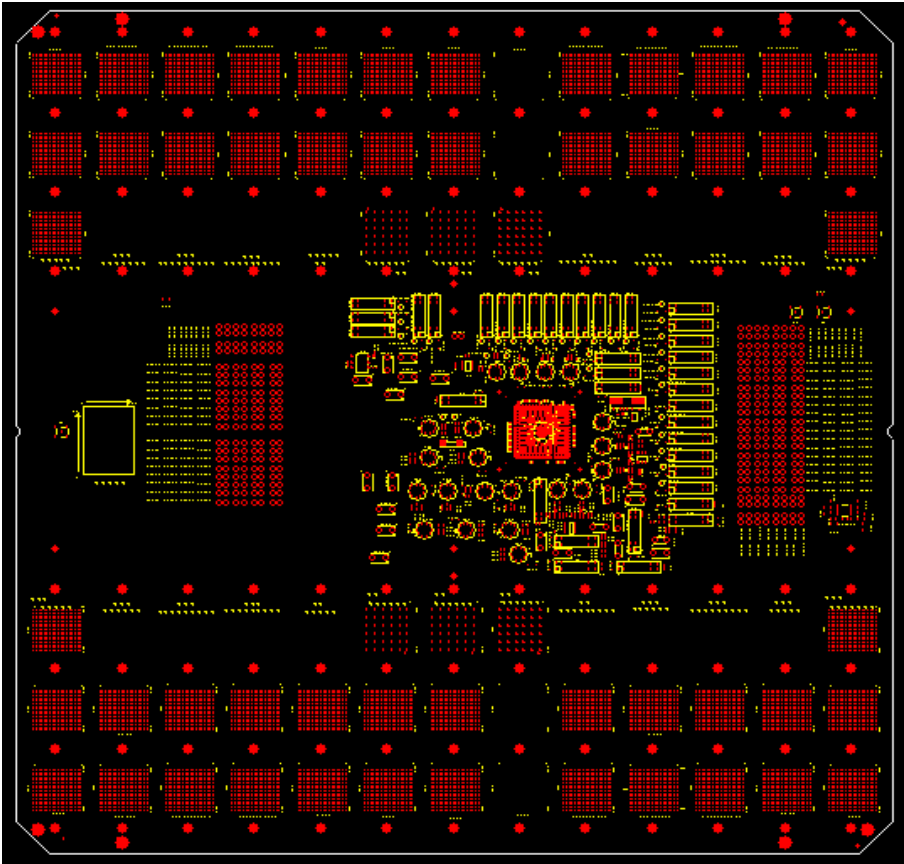
ULTRA FLEX-CASE STUDY

Ultraflex Design



- 812 pins, 0.8mm pitch BGA
- 669 Components
- 226mil board thickness
- 1120 nets
- 34 layers
- Composite material
 - FR4 material
 - Roger material

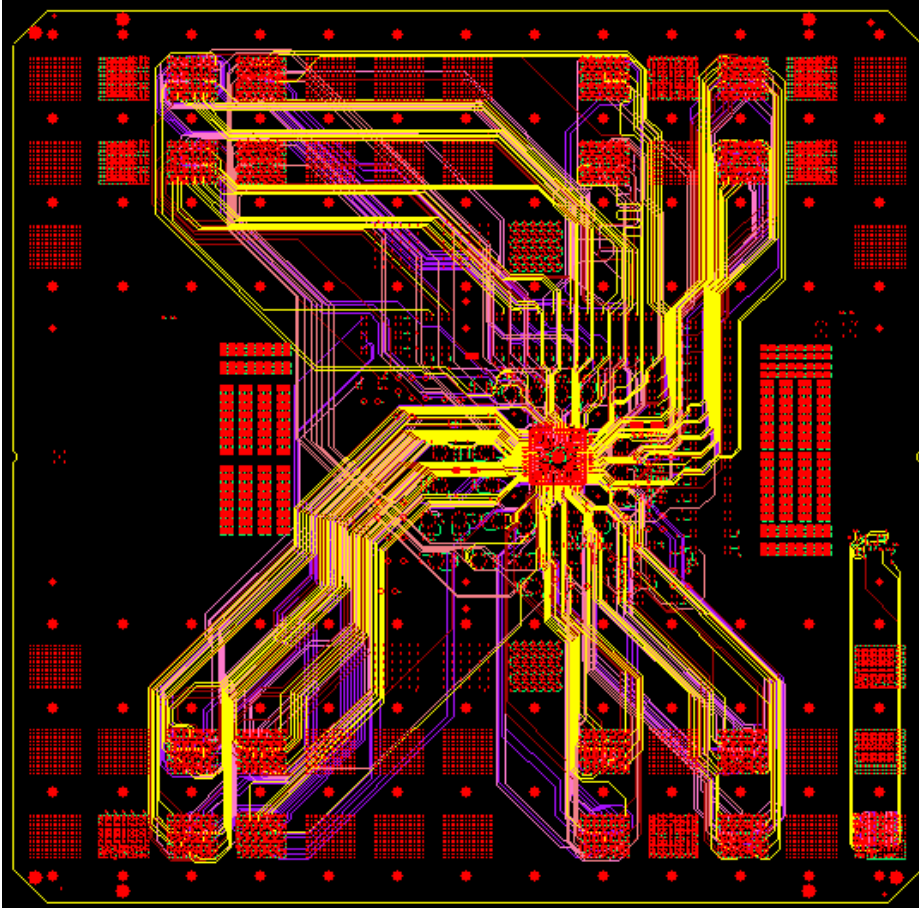
Ultraflex Design



Instrument used

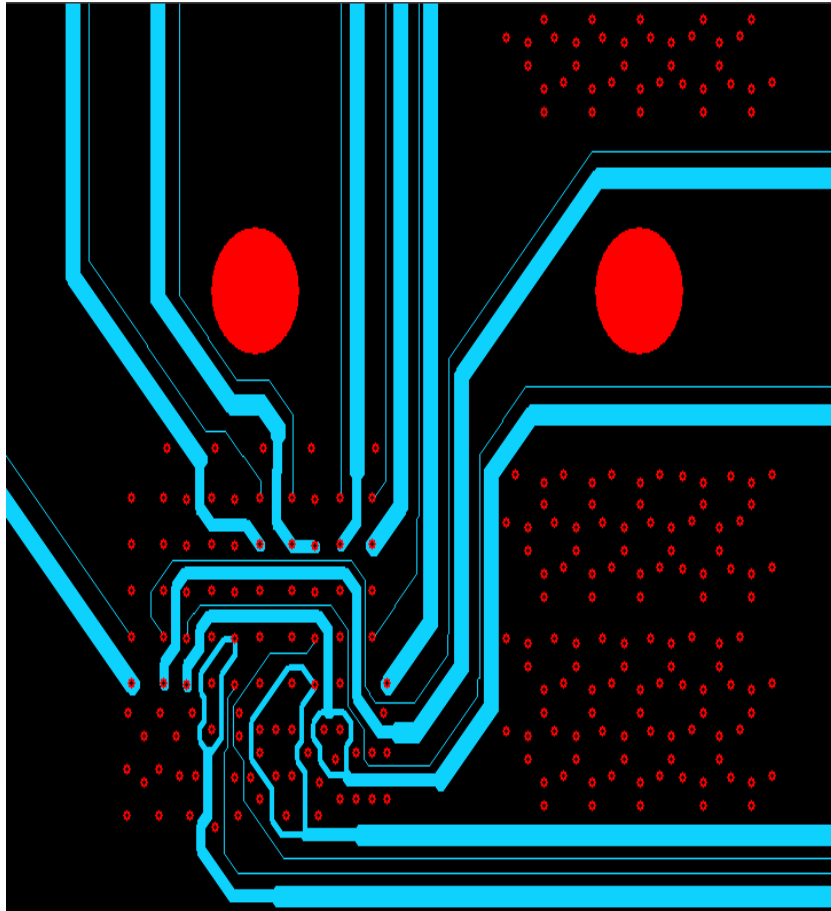
- HSD 1000 - 8
- DC30 - 1
- BBAC - 2
- HEXVS - 2
- SB6G - 3
- SUPPORT BOARD - 1

HSD 1000 - 8



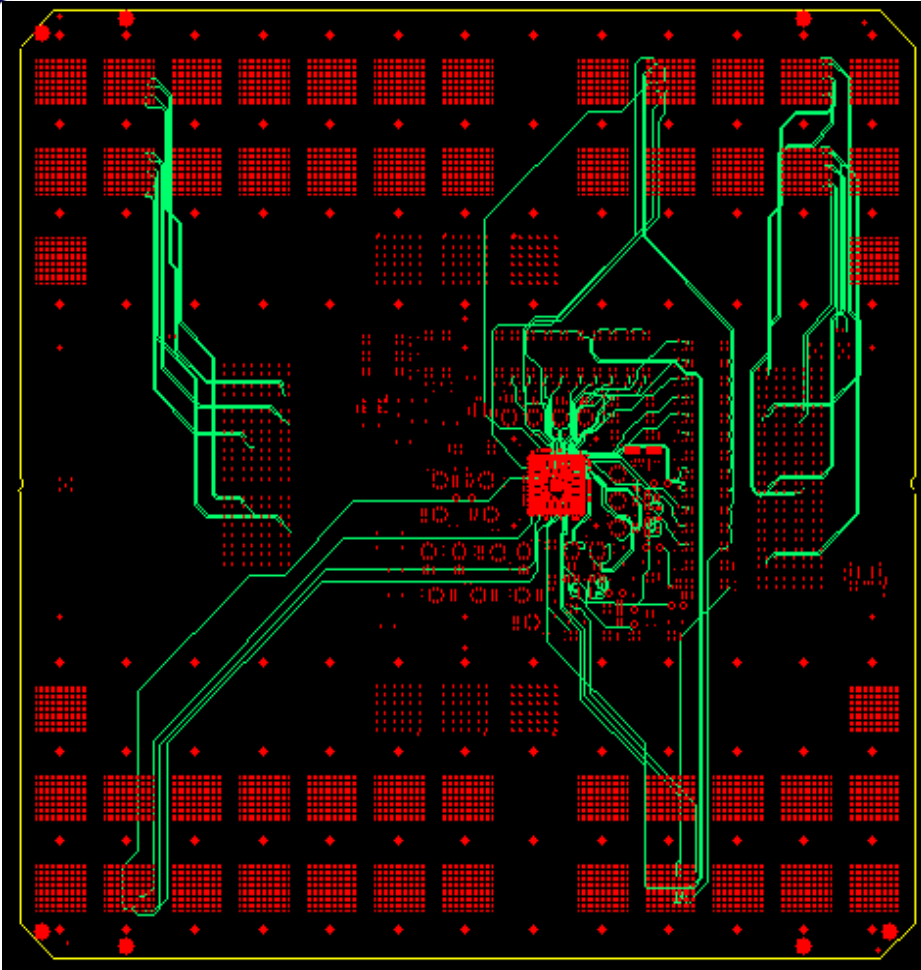
- HSD signal frequency - 200 MHz.
- Data rate - 1000 MBPS.
- There are 8 group of signals. All the signals in a group should go to a single HSD slot.
- 2 GPIO clock signals are routed to single slot with 5X spacing from other signals.
- All HSD signals are routed as 50 Ohm impedance controlled traces.

DC30 - 1



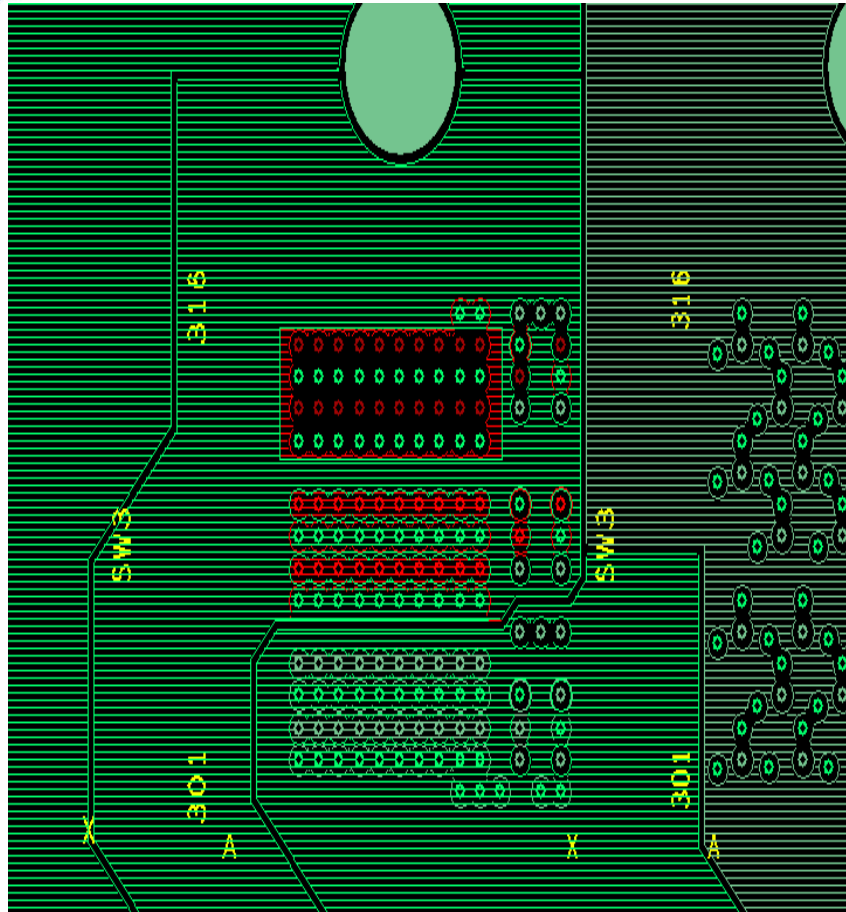
- Voltage range - +/-30V
- Routed the force and sense as kelvin connection with constant spacing between force and sense traces.
- Trace width used:
Force-50mil
Sense-6mil

BBAC - 2



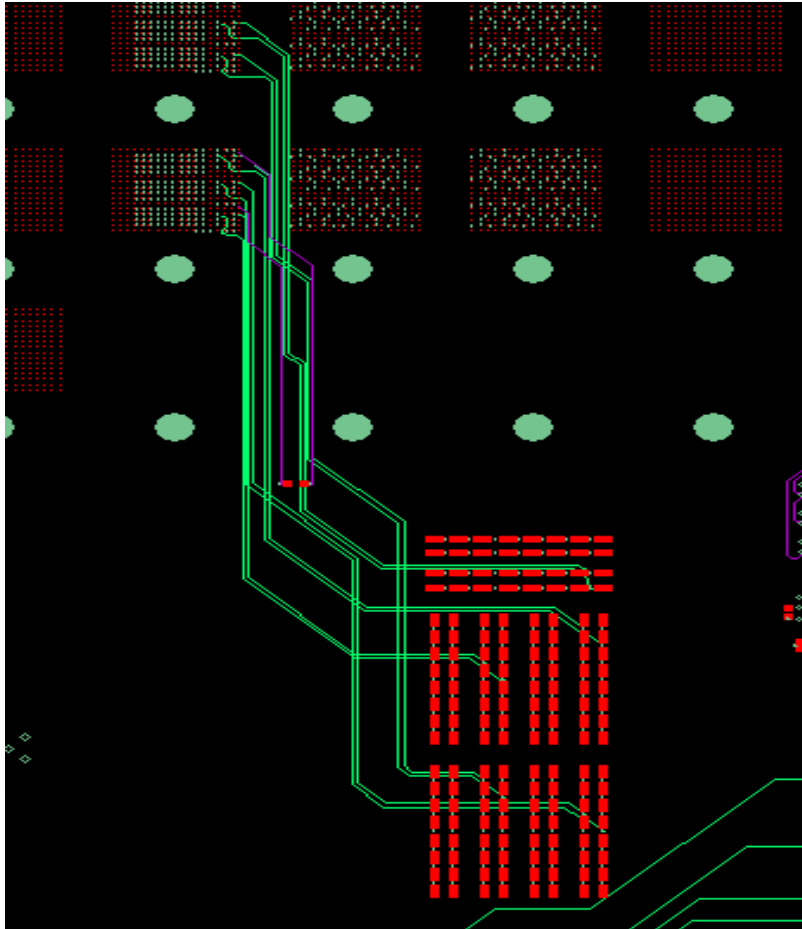
- These signals are routed in separate analog signal layer.
- Routed as a differential pair.

HEXVS - 2



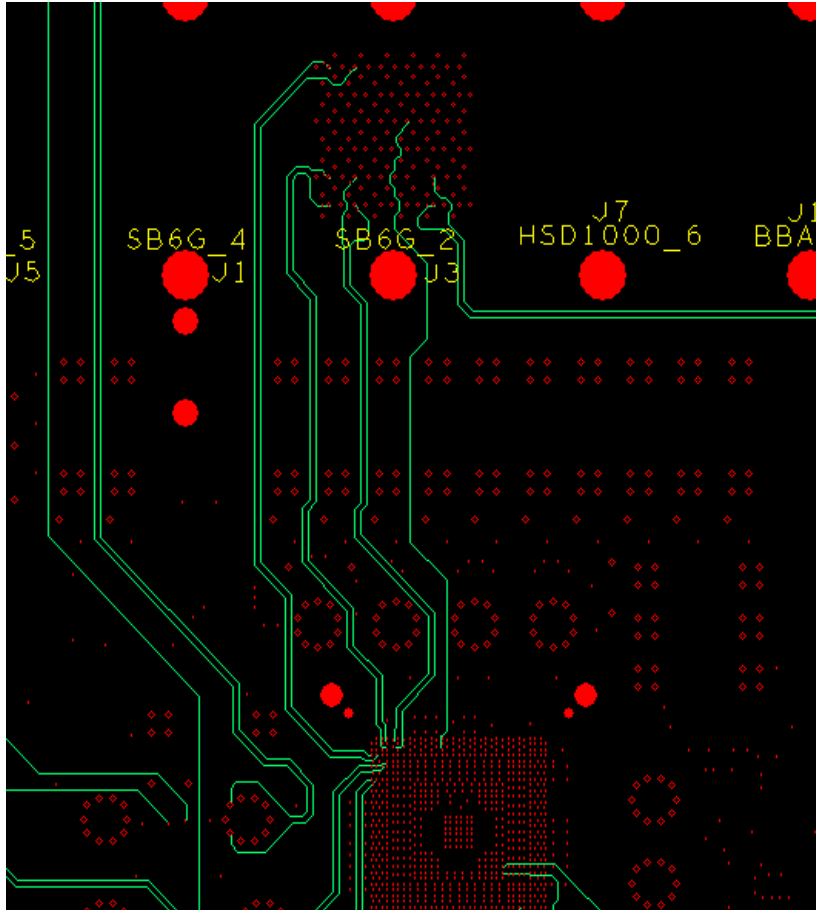
- Current Rating-15A
- We have used planes for HEXVS supplies.
- Each HEXVS power plane has a return plane in the adjacent layer.
- The Returns for other HEXVS supplies should not all be connected at the instrument.

HEXVS - 2



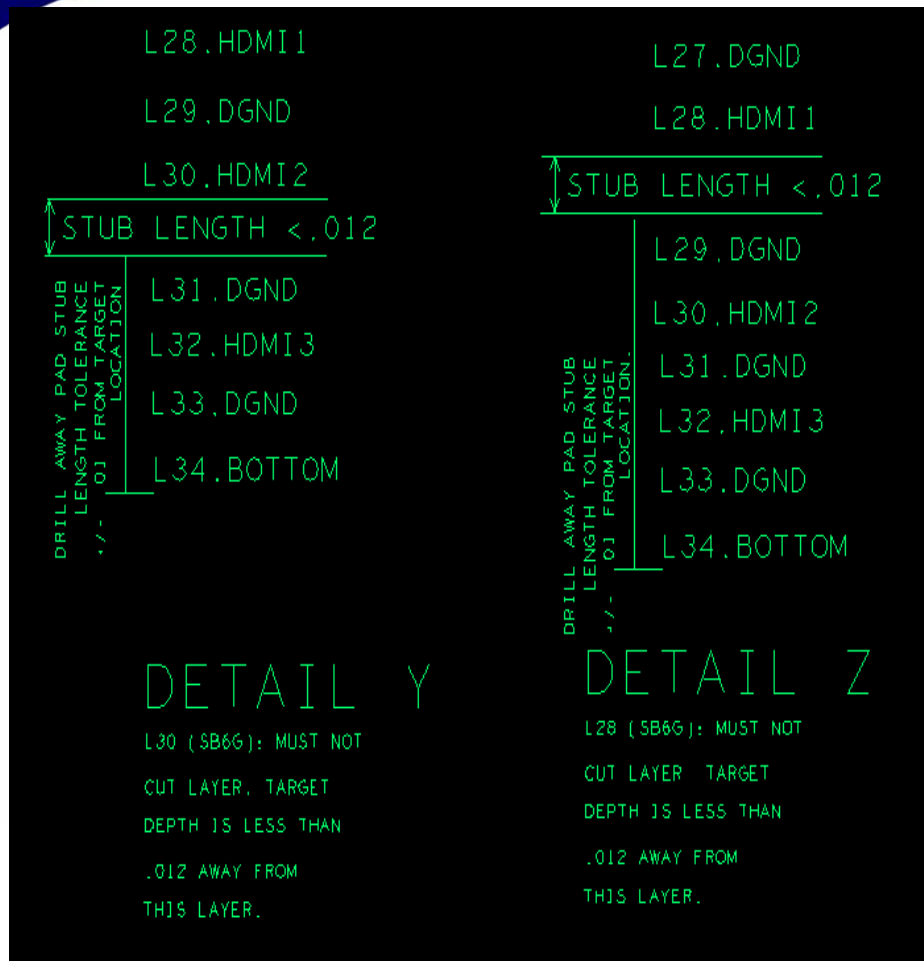
- 16 By-pass capacitors used for each power supply
- Used ceramic capacitors with low ESR and ESL
- The By-pass capacitors are placed near the DUT.
- The force and sense are routed from tester slot to these capacitors.

SB6G Slot

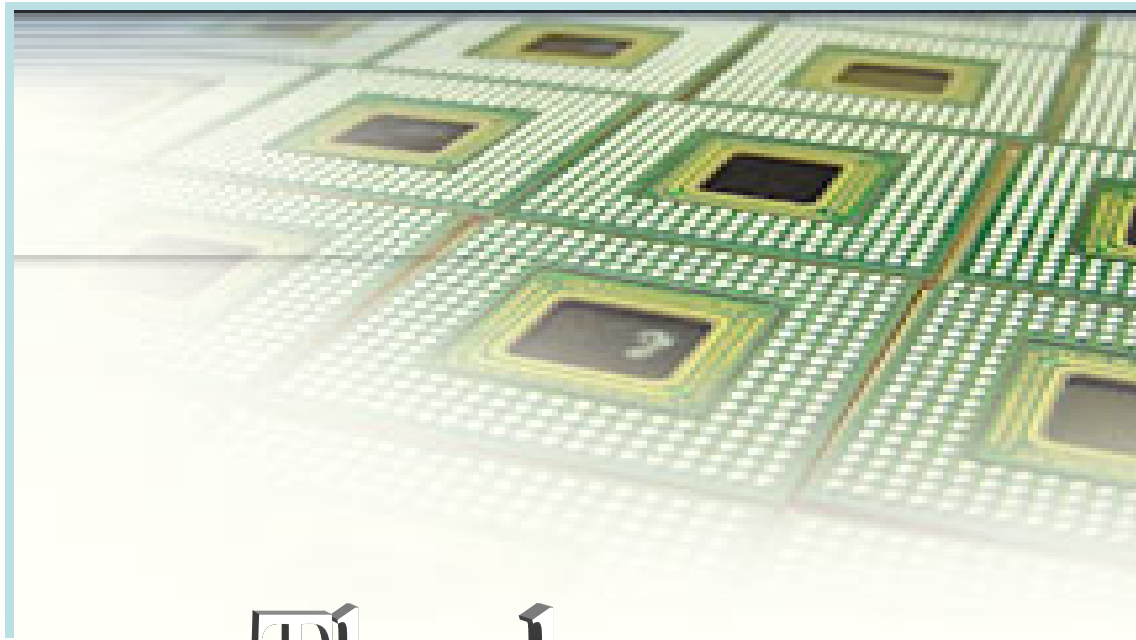


- 6Gbps Max data rate
- 13 high frequency diff pairs
- The neck down length of positive and negative signals in the DUT area are matched exactly
- Added speedy dots for all signals to maximize band width of via to trace transition
- Backdrilling
- Via filling

BACK DRILLING



- For High speed signals, length should be minimized. So we removed the unnecessary stub length in high speed signal vias.
- The high speed signals in DUT are routed in layers closest to the DUT.
- The high speed signals in Tester side are routed in layers closest to the tester side.



Thank you